

N-channel 60 V, 0.019 Ω typ., 8 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - production data

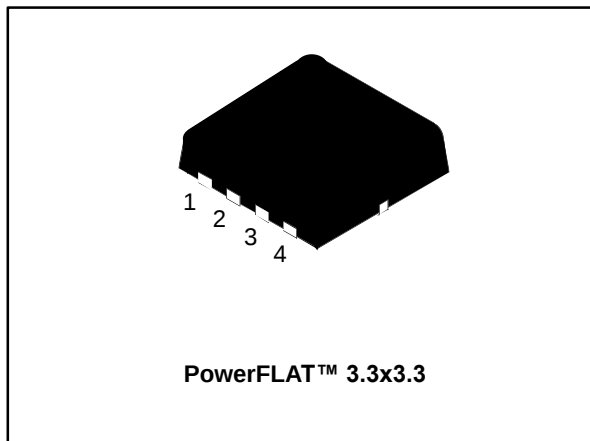


Figure 1: Internal schematic diagram

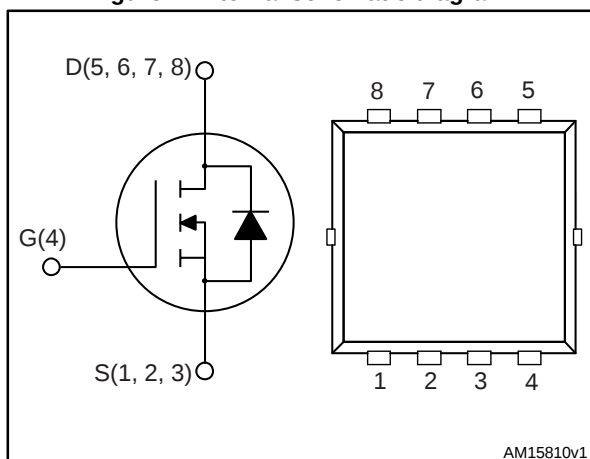


Table 1: Device summary

Order code	Marking	Package	Packing
STL8N6F7	8N6F7	PowerFLAT™ 3.3x3.3	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL8N6F7	60 V	0.023 Ω	8 A

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	36	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	22	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	144	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	8	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	32	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	60	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	3	W
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:(1) This value is rated according to R_{thj-c} .

(2) Pulse width limited by safe operating area.

(3) This value is rated according to $R_{thj-pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	42.8	$^{\circ}\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case max.	2.1	$^{\circ}\text{C/W}$

Notes:(1) When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ sec}$.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	60			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V V _{DS} = 60 V			1	μA
I _{GSS}	Gate-body leakage current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 4 A		0.019	0.023	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 30 V, f = 1 MHz, V _{GS} = 0 V	-	420	-	pF
C _{oss}	Output capacitance		-	215	-	pF
C _{rss}	Reverse transfer capacitance		-	16	-	pF
Q _g	Total gate charge	V _{DD} = 30 V, I _D = 8 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	8	-	nC
Q _{gs}	Gate-source charge		-	2.3	-	nC
Q _{gd}	Gate-drain charge		-	2.1	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 30 V, I _D = 4 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times")	-	7.85	-	ns
t _r	Rise time		-	3.25	-	ns
t _{d(off)}	Turn-off delay time		-	12.1	-	ns
t _f	Fall time		-	3.95	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 8 A, V _{GS} = 0 V	-		1.2	V
t _{rr}	Reverse recovery time	I _D = 8 A, di/dt = 100 A/μs V _{DD} = 48 V (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	17.1		ns
Q _{rr}	Reverse recovery charge		-	6.67		nC
I _{RRM}	Reverse recovery current		-	0.8		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

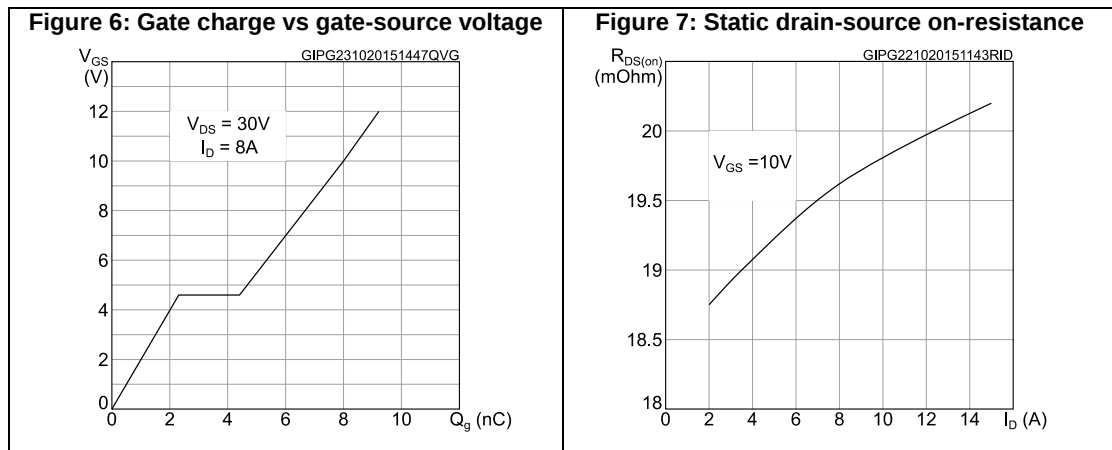
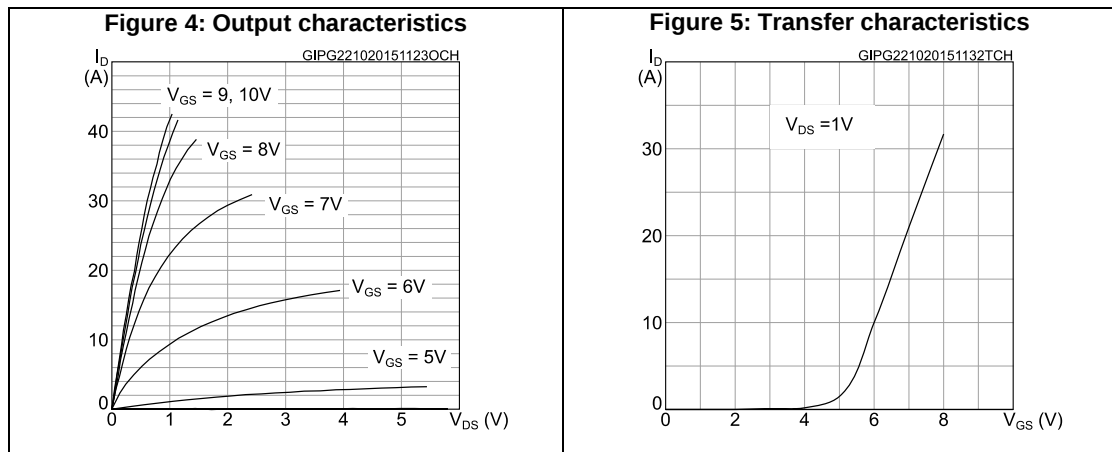
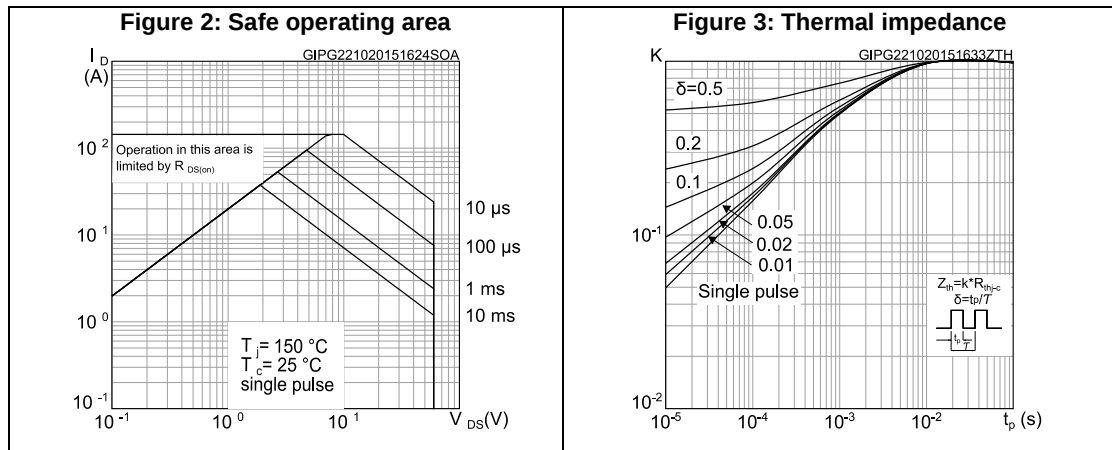


Figure 8: Capacitance variations

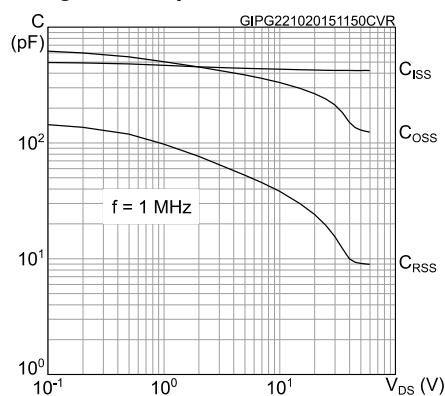


Figure 9: Normalized gate threshold voltage vs temperature

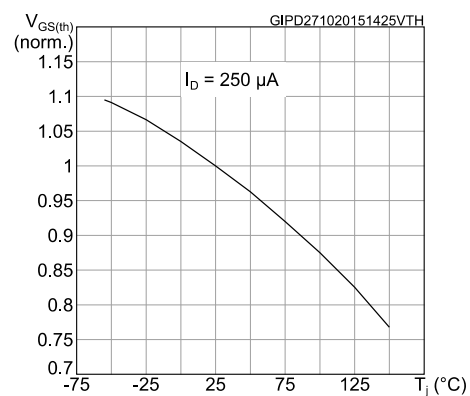


Figure 10: Normalized on-resistance vs temperature

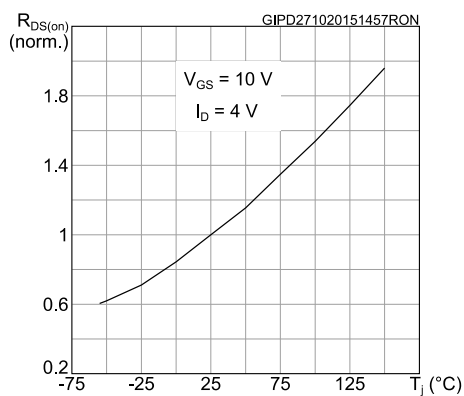


Figure 11: Normalized V(BR)DSS vs temperature

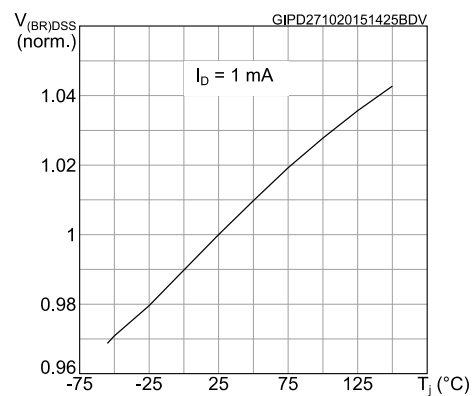
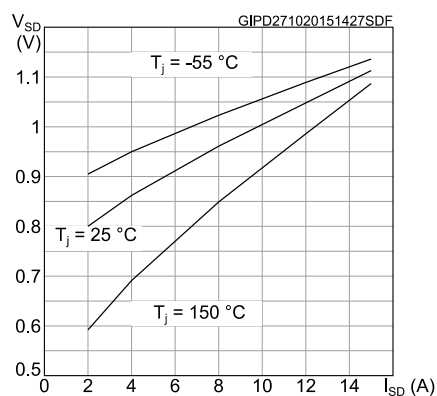
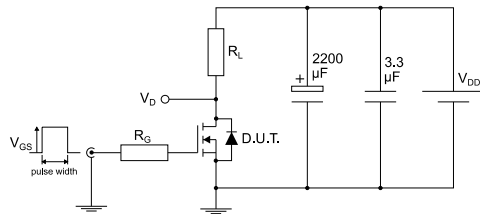


Figure 12: Source-drain diode forward characteristics



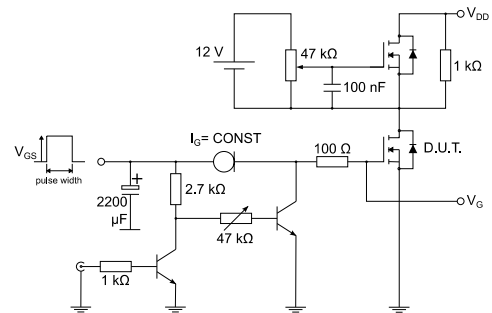
3 Test circuits

Figure 13: Test circuit for resistive load switching times



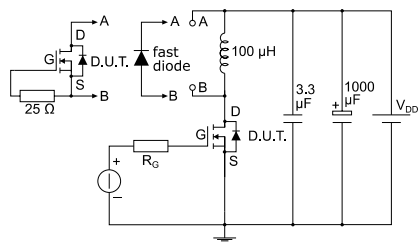
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Figure 14: Test circuit for gate charge behavior



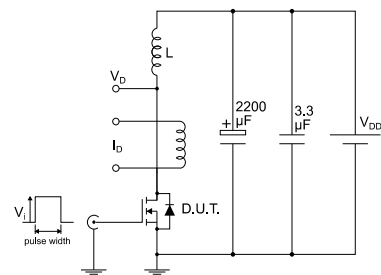
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Figure 15: Test circuit for inductive load switching and diode recovery times



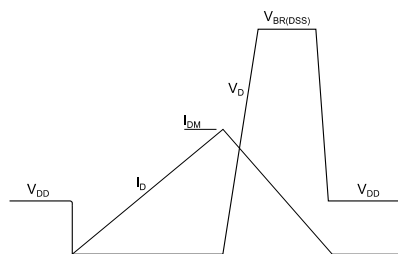
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Figure 16: Unclamped inductive load test circuit



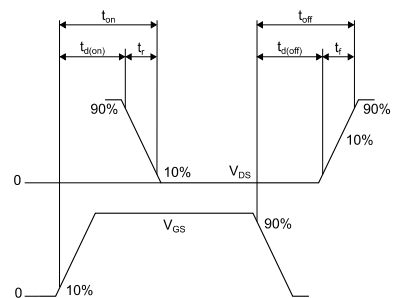
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT 3.3x3.3 package information

Figure 19: PowerFLAT™ 3.3x3.3 package outline

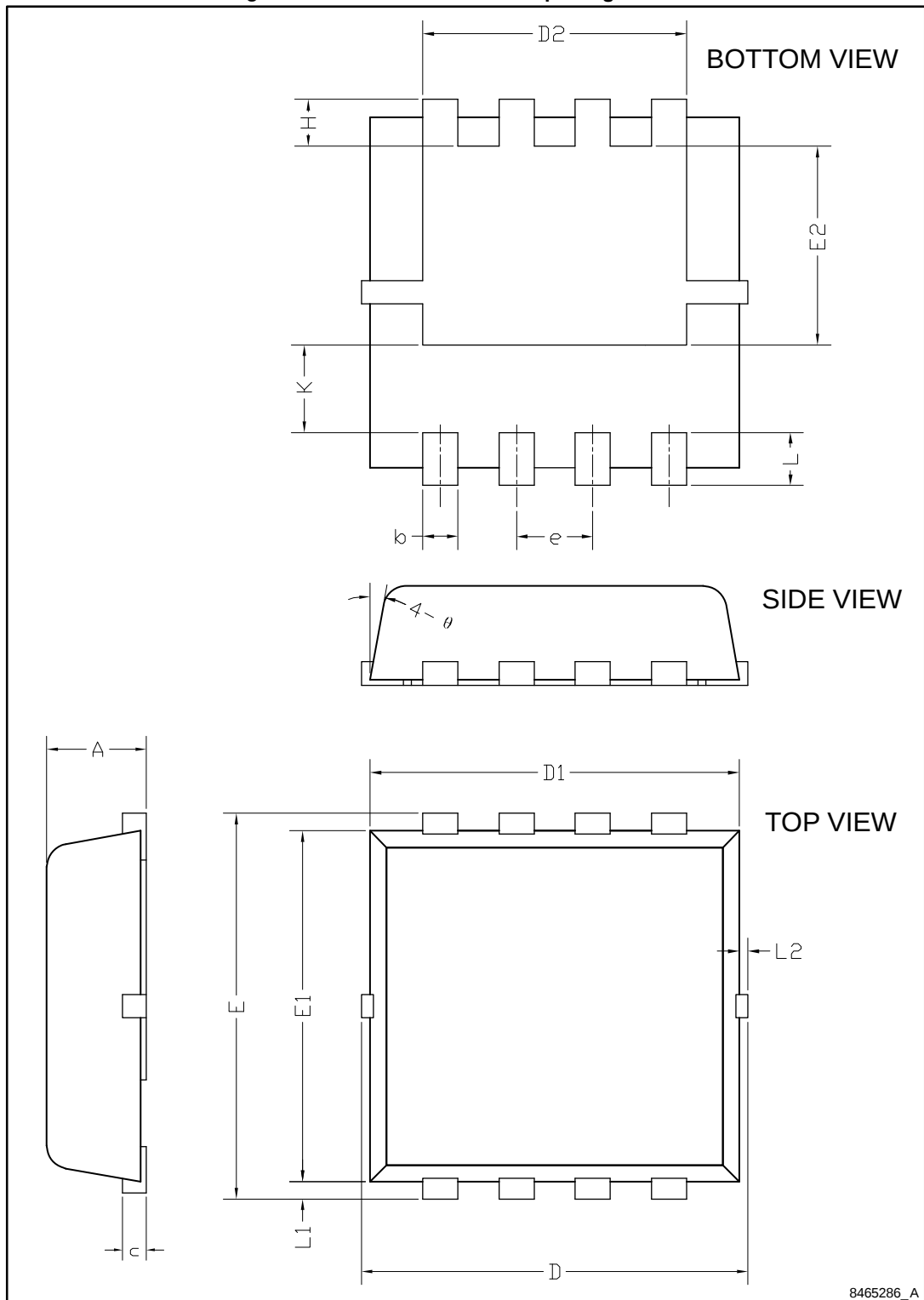
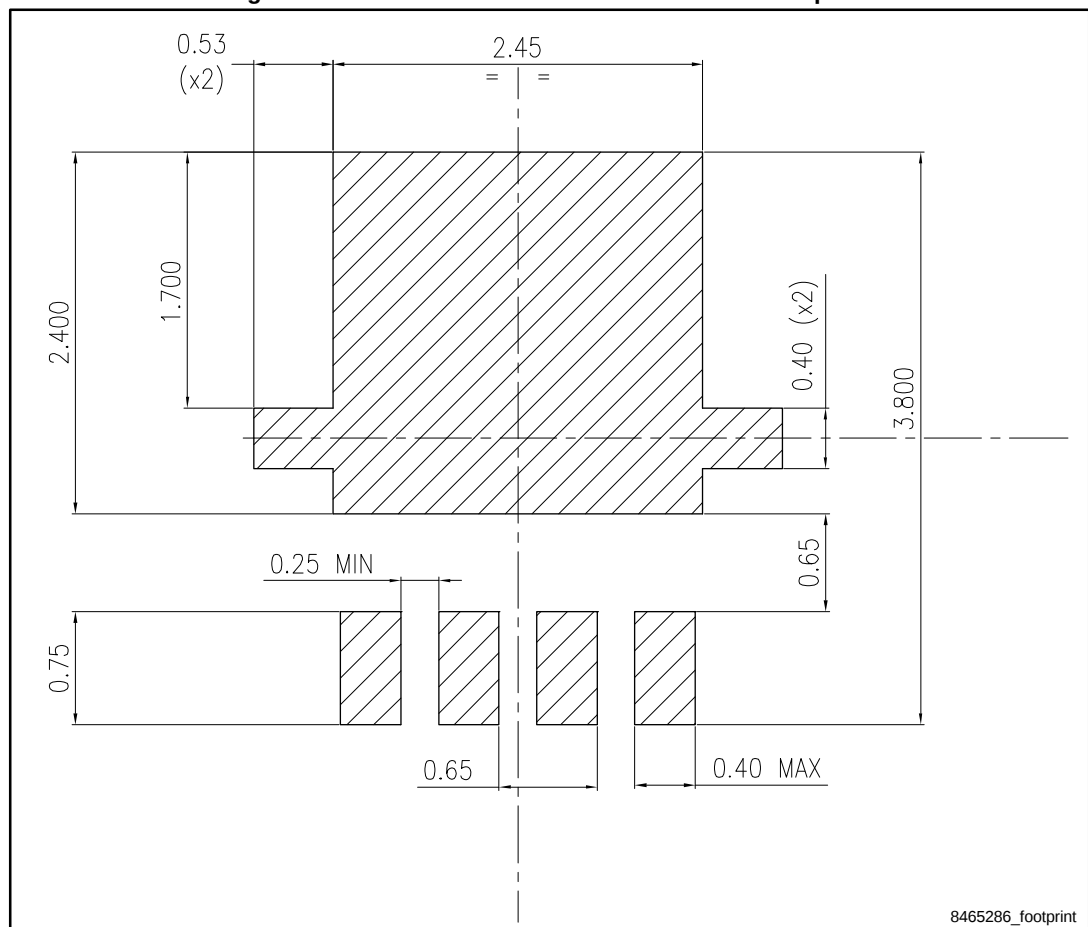


Table 8: PowerFLAT™ 3.3x3.3 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 20: PowerFLAT™ 3.3x3.3 recommended footprint



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
20-Aug-2015	1	First release.
22-Oct-2015	2	Updated title and features in cover page. Updated Table 4: "On /off states" , Table 5: "Dynamic" , Table 6: "Switching times" and Table 7: "Source-drain diode" . Added Section 3.1: "Electrical characteristics (curves)" . Document status promoted from preliminary di production data.

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