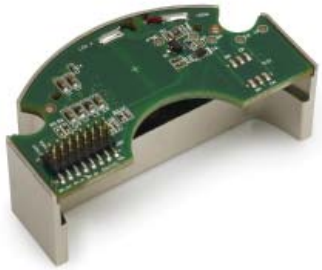
AEAT-9000-1GSH1 (Basic Option)

Ultra-precision 17-Bit Absolute Single Turn Encoder

Data Sheet



Description

Avago Technologies' AEAT-9000 series are high resolution single turn optical absolute encoders. The 17-bit AEAT-9000 encoder code disc consists of 13 pairs of differential absolute tracks and 2 pairs of sinusoidal tracks to perform 4 bits interpolation. In addition, the encoder incorporates photo detectors for electrical alignment on the radial and tilt. AEAT-9000 also comes with 2 channel incremental output with the basic of 2048 counts per rotation.

The AEAT-9000 is a modular absolute encoder that consists of a read head module and a high-precision code disc [(HEDG-9000-H13 & HEDG-9000-H14) which is ordered separately]. The modular design allows for better flexibility to system designers to easily design-in the encoder feedback system.

Note: Avago Technologies encoders are not recommended for use in safety critical applications, e.g., ABS braking systems, power steering, life support systems and critical care medical equipment. Avago's products and software are not specifically designed, manufactured or authorized for sale as parts, components or assemblies for the planning, construction, maintenance or direct operation of a nuclear facility or for use in medical devices or applications. Customer is solely responsible, and waives all rights to make claims against Avago or its suppliers, for all loss, damage, expense or liability in connection with such use. Please contact sales representative if more clarification is needed.

Features

- 17-bit absolute single turn output (131072 absolute positions over 360°)
- 2048 CPR A/B channel incremental digital output
- Interface output is SSI (2wire SSI / 3wire SSI) with RS485 line transceiver or single ended option
- On-chip interpolation and code correction compensate for mounting tolerance
- Selectable direction for Up/Down position counter
- Electrical alignment output for tilt and locate
- Built-in monitor track for monitoring of LED light level
- Error output for LED degradation
- -40 to 115° C operating temperature

Applications

Typical applications include:

- Rotary applications up to 17 bits/360° absolute position
- Integration into servo motors
- Industrial and maritime valve control
- High precision test and measurement machines
- Industrial and factory automation equipments
- Textile, woodworking & packaging machineries
- Nacelle & blades control in wind turbine

ESD WARNING: *HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.*

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-40	85	℃
Operating Temperature	T_A	-40	115	℃
Supply Voltage	V_{DD}	-0.3	6	V
Voltages at all input and output pins	Vin & Vout	-0.3	V_{DD}+0.3	V

Note: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables "Recommended Operating Conditions and Characteristics" provide conditions for actual device operation.

Recommended Operating Conditions

Description	Symbol	Min.	Typical	Max.	Units	Notes
Temperature	T_A	-40	25	115	℃	
Supply Voltage	V_{DD}	4.5	5	5.5	V	Ripple < 100 mVpp
Input-H-Level Threshold	V_{ih}	2.0		V_{DD}	V	Input-H-Level threshold
Input-L-Level Threshold	V_{il}	0		0.8	V	Input-L-Level threshold

Electrical Characteristics Table (VDD = 4.5 to 5.5 V, TA = -40 to +115° C)

Electrical characteristics over recommended operating conditions. Typical values at 25° C

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Currents						
Total Current	I_{Total}	LED current @10 mA typ		94		mA
Digital Inputs						
Pull Up Current	I_{pu}	Room Temperature	-106	-60	-35	µA
Pull down Current	I_{pd}	Room Temperature	-108	-56	-31	µA
Digital Outputs						
Ouput-H-Level	V_{oh}	I_{oh} = 2 mA	V_{DD}- 0.5V		V_{DD}	V
Output-L-Level	V_{ol}	I_{ol} = -2mA	0		0.5	V
SSI Serial Interface						
SCL Clock Frequency (3wire SSI)	f_{clock}				10	MHz
SCL clock Frequency (2wire SSI)	fclock				1.5	MHz
Duty Cycle f_{clock}	T_{clock},LH	f_{clock} = 10 MHz	0.4		0.6	
Gray Code Monotony Error (1)		fclock = 5 MHz, RPM = 100		1		Error step
SPI Serial Interface						
SPI_Clock	t clock			100		kHZ
Incremental A/B (2048cpr)						
Cycle error		5.0 V @ Nominal	-8		+8	Deg
Phase error btw A/B		5.0 V @ Nominal	-15	5	+15	Deg
Duty error		5.0 V @ Nominal	-23	4	+28	Deg

Note: Code monotony error is dependent on customer installation and the bearing and shaft eccentricity being used.

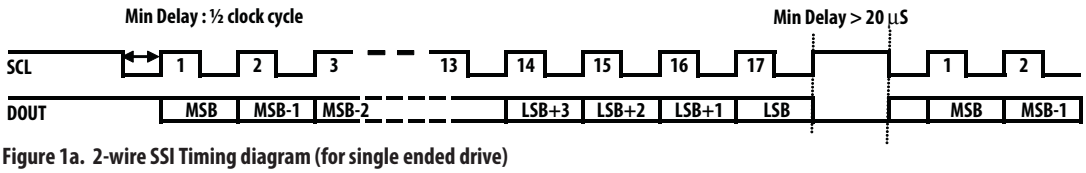


Figure 1a. 2-wire SSI Timing diagram (for single ended drive)

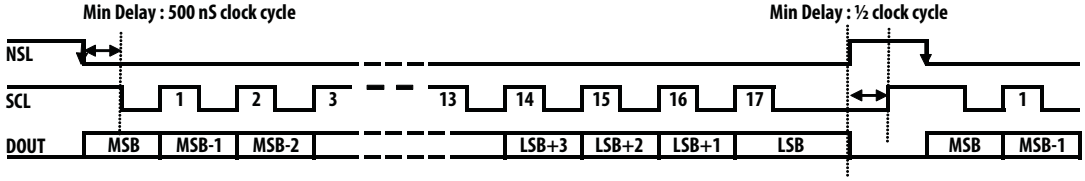


Figure 1b. 3-wire SSI Timing diagram (for single ended drive)

Theory of Operation

1. The AEAT-9000 encoder consists of 13 differential absolute track signals. 12 tracks generated from code wheel and track number 13 is generating from the analogue sine of the incremental track.
2. 8 photo sensors are used for analog Sine+, Sine-, Cosine+, Cosine- signal generation with 90° phase shift. The analog signals are calibrated to correct the offset and gain via SPI interface. The offset and gain values will be preloaded into internal memory. After signal conditioning, the encoder performs on chip interpolation to generate an additional 4bit absolute output (D-1~D-4) and synchronizes with the 13 absolute track to make up a 17 bits absolute encoder. The analog signals are true differential signals with a frequency response of 500 kHz, enabling output position data to be read at high speed.
3. An additional sensor is used for radial alignment. Sensor Locate will output at LocTest pin and is enabled using SPI interface during alignment mode.
4. Besides that, the inner and outer tracks are used for tilt angle measurement, by generation of pulses via TiltOut pin. The TiltOut pulse width will be used to determine the tilt angle.
5. A Zero_RST pin is used to allow the encoder to set zero position at any position. The encoder stores this preset value into the internal memory and indicates the new position information with reference to the preset value every time data is read out. The Zero reset function is enabled when Zero_RST pin is pulled to ground.

Alignment Mode

Align the code dics to the read head by positioning the mid-point location of the code disc hub about 17.5 mm away from center point of the mounting hole as shown below. SPI will command to switch to alignment mode.

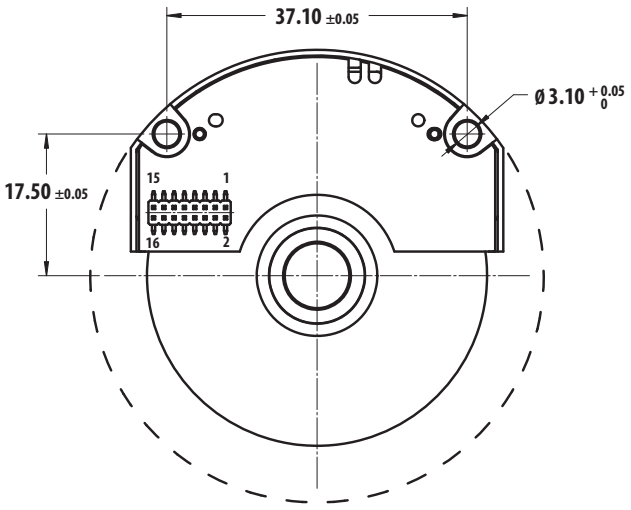


Figure 2. Alignment between read heard and the codewheel.

1. Write address 0x11 with 1010 1011 to unlock the register.
2. Write address 0x10 with 0001 0001 to turn on alignment mode.

address	Command+add	Data
0x11	01+001 0001	1010 1011
0x10	01+001 0000	0001 0001

The D1 signal will be output to LocTest pin and at nominal location, the signal pattern is as shown in below figure 3 and 4. The amplitude of the signal will depend on the total stack-up TIR of the code wheel.

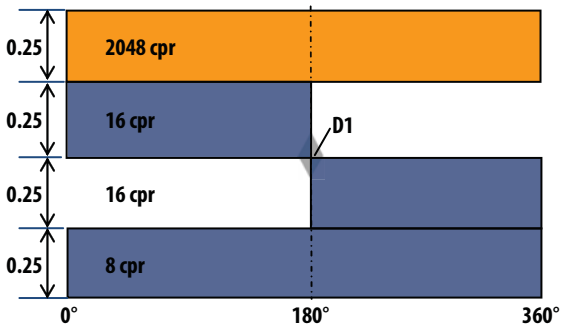


Figure 3. Code disk track 7 alignment to D1 photo detector

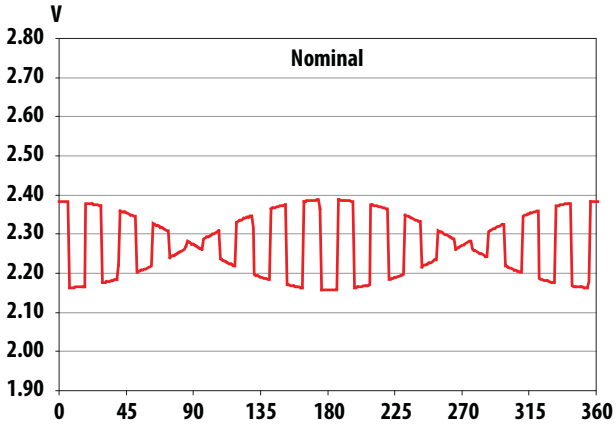


Figure 4. Output of D1 with code wheel eccentricity of 10 μm

D1 is used to align the code disk to the encoder chip in radial axes. For the sensor tilt alignment, the TiltOut signal is monitored. An output pulse is generated via TiltOut pin as shown below in Figure 5. At nominal position the t/T will be at the ratio of 0.0078 at any motor spinning speed.

After alignment is done, an SPI command is sent to set the same address (0x10) with 0000 0001 or a power cycle is performed to set back the register to the default value of 0000 0001.

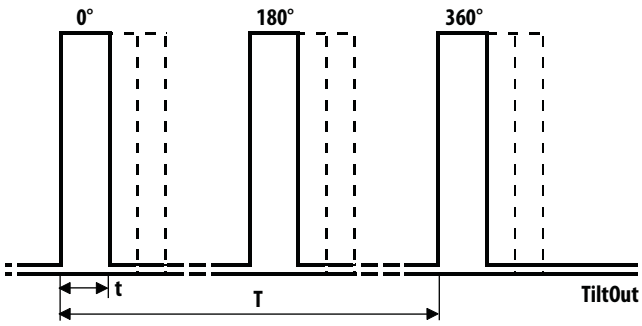


Figure 5. TiltOut signal in alignment mode.

LED regulation

The LED regulation control unit keeps the LED power perceived by the PDA constant regardless of temperature or aging effects. It also acts to stabilize the amplitudes of the Sine/Cosine signals.

If the power control exceeds the operating range the LERR pin will be pulled to logic High.

The LED power control is generated from the analog tracks, i.e. the Sine/Cosine photo sensors. At high RPM speeds, the LED power control will compensate for signal amplitudes attenuation, and it can drive up to 50 mA maximum current.

Sine/Cosine Signal Calibration

Due to amplifier mismatch and mechanical misalignment the signals do have gain and offset errors. Once the alignment is done, the encoder will need to be switched to calibration mode, which to correct the single-ended sine and cosine to 2.5 V offset and 1 Vpp amplitude. The signal calibration is done with LED regulation turned off.

The sine/cosine signal will driven out through an op-amp where the Vpp will be 0.5Vpp amplitude for a single ended sin/cosine with 2.5 V offset.

Calibration is done at Avago in factory prior to ship out, so user can skip this process.

Interpolator for Sine & Cosine Channels

The interpolator on the Sine/Cosine analog signal generates the digital signal of D-1 to D-4 by a flash A/D conversion; the interpolation value will be synchronized with the 13 digital tracks to generate the 17-bit absolute position value.

DOUT, SCL, NSL (3wire/2 wire SSI)

The absolute position is serially streamed out using SSI protocol. The most significant bit, MSB (D17) will always be sent first from the DOUT pin. The positional data can be inverted (i.e. count down instead of up) with MSBINV pulled to high. By default it will be low once powered on.

The NSL pin acts as the chip enable pin. NSL has to be triggered first to low before SCL clock can reach the encoder to read out the positional data. The maximum SCL clock frequency is up to 10 MHz.

Valid data of DOUT should be read when the SCL clock is low. Please refer to timing diagram on Figure 1.

In some application of point to point interface, 2 wire SSI is use which will eliminate the use of NSL pin. In this case NSL will need to pull to low all times. For 2 wire SSI, the SCL timing will be limited to about 1.5 MHz.

LERR pin is a general error pin as a feedback to user on some errors such as temperature sensor exceeding operating limit, LED ray is low, and this is an indication when light intensity is at a critical stage affecting the performance of the encoder. It is caused either by contamination of the code disc or LED degradation.

Incremental A/B output

Besides the absolute position read out, AEAT-9000 also comes with 2 channel incremental output with 2048CPR. These A/B channel is generated from differential Sin/Cosine. The frequency response of the A/B will be based on the differential Sin/Cosine response with a max of 500 kHz without much degradation on the Vpp amplitude.

SPI Interface (SPI_SO, SPI_SI, SPI_CLK)

SPI is the interface that is used to configure the internal register settings to turn on alignment mode and calibration mode.

During alignment mode, Loctest signal and Tiltout will provide an output to perform alignment.

During calibration mode, the SPI interface is used to perform Sine/Cosine gain and offset calibration. It is also used to program the EEPROM once the calibration has been done.

To access the SPI register, write the data 1110 1011 to address 0x1b to enable changes on the register setting. This is needed every time the device is power on.

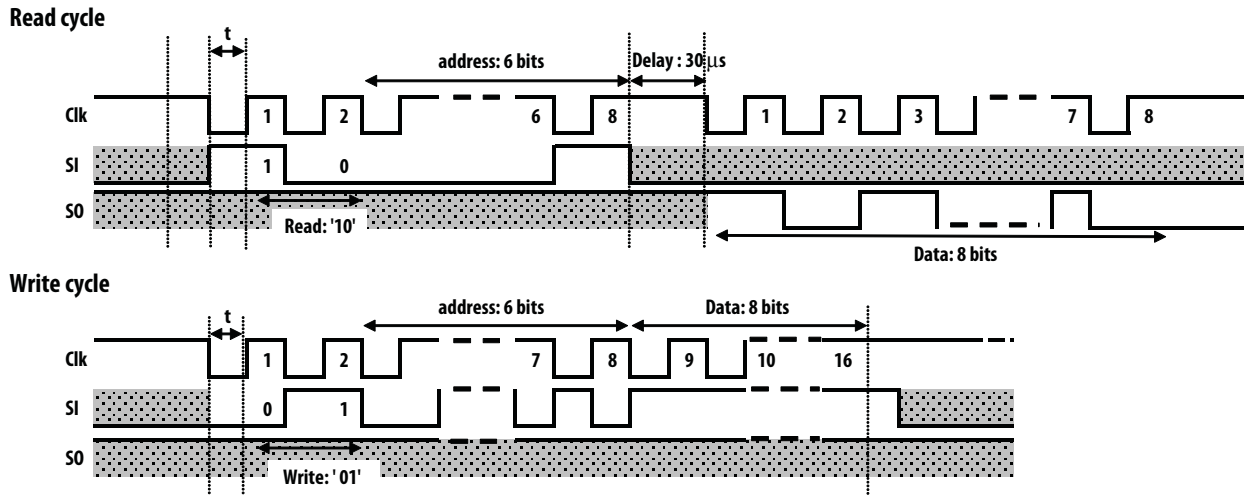


Figure 6. SPI timing diagram for read and write

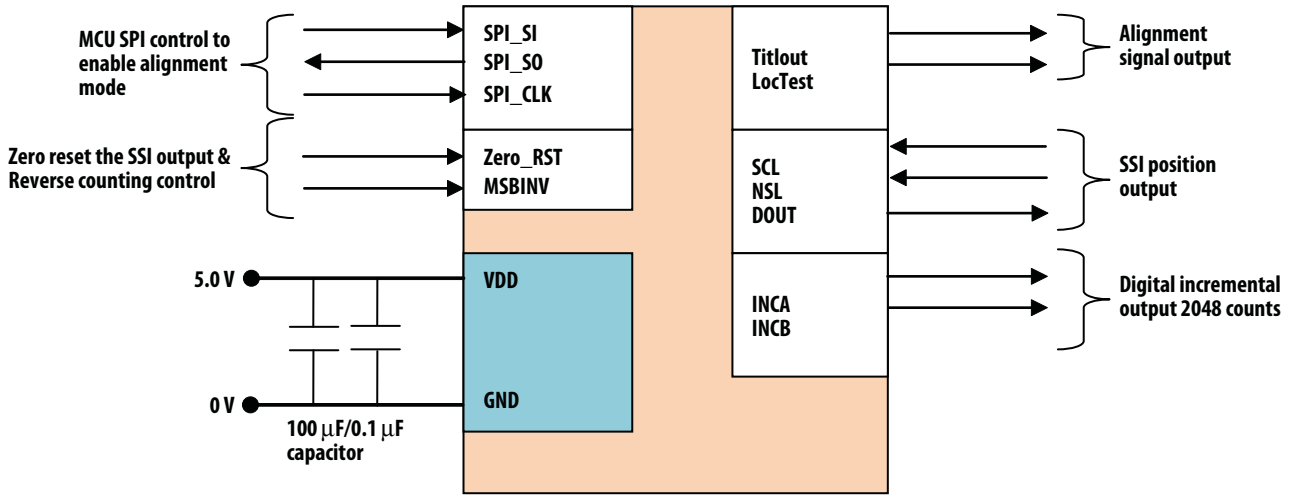


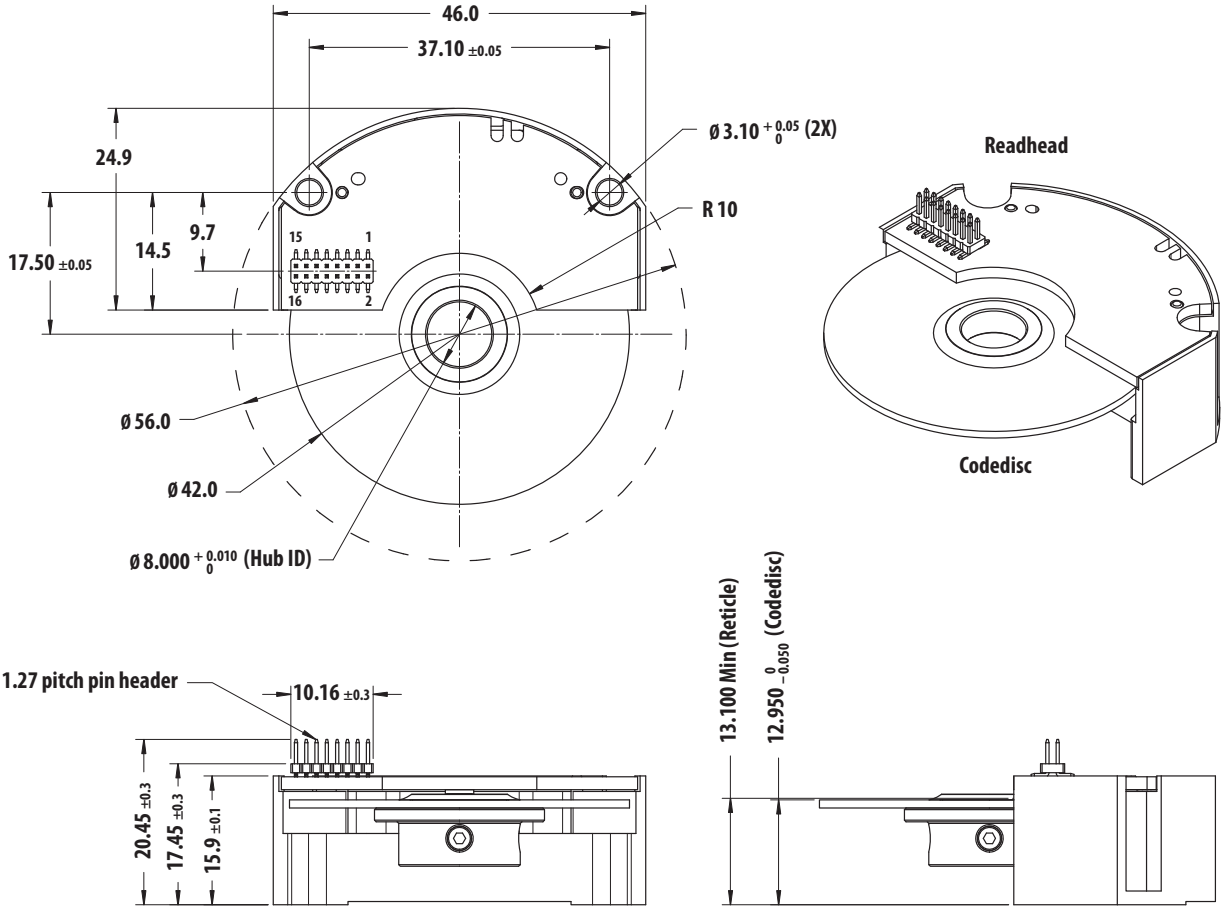
Figure 7. AEAT9000 interface Block diagram

Pin out Descriptions (Serial SSI 2/3wire option)

No.	Pin Name	Description	Function	Notes
1	VDDIN	Supply Voltage	+5V Supply	
2	SCL	Digital Input	SCL clock (for 3wire/2wire SSI)	
3	DGND	Ground for supply voltage	Connect ground	
4	NSL	Digital Input	NSL (for 3wire SSI only)Note2	
5	NC(nRST)	Digital Output	Chip Reset	CMOS, internal pu
6	DOUT	Digital Output	DOUT (for 3wire/2wire SSI)	
7	LERR	Digital Output	ERROR pin, error(=1)/no error(=0)	CMOS
8	LocTest	Analog Output	Alignment locate signal	CMOS, analog out
9	Zero_RST	Digital Input	Pull down to zero the absolute position	CMOS, internal pu
10	TiltOut	Digital Output	Tilt alignment output	CMOS
11	MSBINV	Digital Input	Inverted counting	CMOS, internal pd
12	SPI_SO	Digital Output	SPI data output	CMOS
13	INCB	Digital Output	B Digital output	CMOS
14	SPI_SI	Digital Input	SPI data input	CMOS, internal pd
15	INCA	Digital Output	A Digital output	CMOS
16	SPI_CLK	Digital Input	SPI clock input	CMOS, internal pu

Note2: For 2wire SSI NSL pin will be not use, just pull it to Ground before power on.

Mechanical Dimensions



Notes:
1. All dimensions are in millimeter.
2. Tolerance: X.X ± 0.10mm.
3. Code disk and readhead mounting tolerances for radial, tangential and gap are as below
   Radial : +/-50 µm (inclusive shaft eccentricity)
   Tangential : +/-100 µm (inclusive shaft eccentricity)
   Gap : 150 to 300 µm
4. Recommended mounting screw:-
   Socket Head cap screw, M2.5 (ISO 4762)
   Flat Washer, M2.5 (ISO 7092)

Ordering Information

AEAT - 9000 - 1 ☐ S ☐ 1

- T – High Temp (-40° C to +115° C)
- G = Gray code
- H - 17 bits

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