EFM32

... the world's most energy friendly microcontrollers

EFM32WG942 DATASHEET

F256/F128/F64

Preliminary

- **ARM Cortex-M4 CPU platform**
  - High Performance 32-bit processor @ up to 48 MHz
  - DSP instruction support and floating-point unit
  - Memory Protection Unit
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.4µA @ 3 V Shufoff Mode with RTC
  - 0.65 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.95 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 67 µA/MHz @ 3 V Sleep Mode
  - 230 µA/MHz @ 3 V Run Mode, with code executed from flash
- **256/128/64 KB Flash**
- **32/32/32 KB RAM**
- **50 General Purpose I/O pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
  - Output state retention and wakeup from Shutoff Mode
- **12 Channel DMA Controller**
- **12 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware AES with 128/256-bit keys in 54/75 cycles**
- **Timers/Counters**
  - 4× 16-bit Timer/Counter
    - 4×3 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 16-bit Low Energy Timer
  - 1× 24-bit Real-Time Counter and 1× 32-bit Real-Time Counter
  - 3× 16/8-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Integrated LCD Controller for up to 8×16 segments**
  - Voltage boost, adjustable contrast and autonomous animation
- **Backup Power Domain**
  - RTC and retention registers in a separate power domain, available in all energy modes
  - Operation from backup battery when main power drains out
- **Communication interfaces**
  - 3× Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816) /IrDA /I2S
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2× I^2C Interface with SMBus support
    - Address recognition in Stop Mode
  - Universal Serial Bus (USB) with Host & OTG support
    - Fully USB 2.0 compliant
    - On-chip PHY and embedded 5V to 3.3V regulator
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 8 single ended channels/4 differential channels
    - On-chip temperature sensor
  - 12-bit 500 ksamples/s Digital to Analog Converter
  - 2× Analog Comparator
    - Capacitive sensing with up to 4 inputs
  - 3× Operational Amplifier
    - 6.1 MHz GBW, Rail-to-rail, Programmable Gain
  - Supply Voltage Comparator
- **Low Energy Sensor Interface (LESENSE)**
  - Autonomous sensor monitoring in Deep Sleep Mode
  - Wide range of sensors supported, including LC sensors and capacitive buttons
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
  - 2-pin Serial Wire Debug interface
    - 1-pin Serial Wire Viewer
  - Embedded Trace Module v3.5 (ETM)
- **Pre-Programmed Serial Bootloader**
- **Temperature range -40 to 85 ºC**
- **Single power supply 1.85 to 3.8 V**
- **TQFP64 package**

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1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32WG942 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32WG942F64-QFP64	64	32	48	1.85 - 3.8	-40 - 85	TQFP64
EFM32WG942F128-QFP64	128	32	48	1.85 - 3.8	-40 - 85	TQFP64
EFM32WG942F256-QFP64	256	32	48	1.85 - 3.8	-40 - 85	TQFP64

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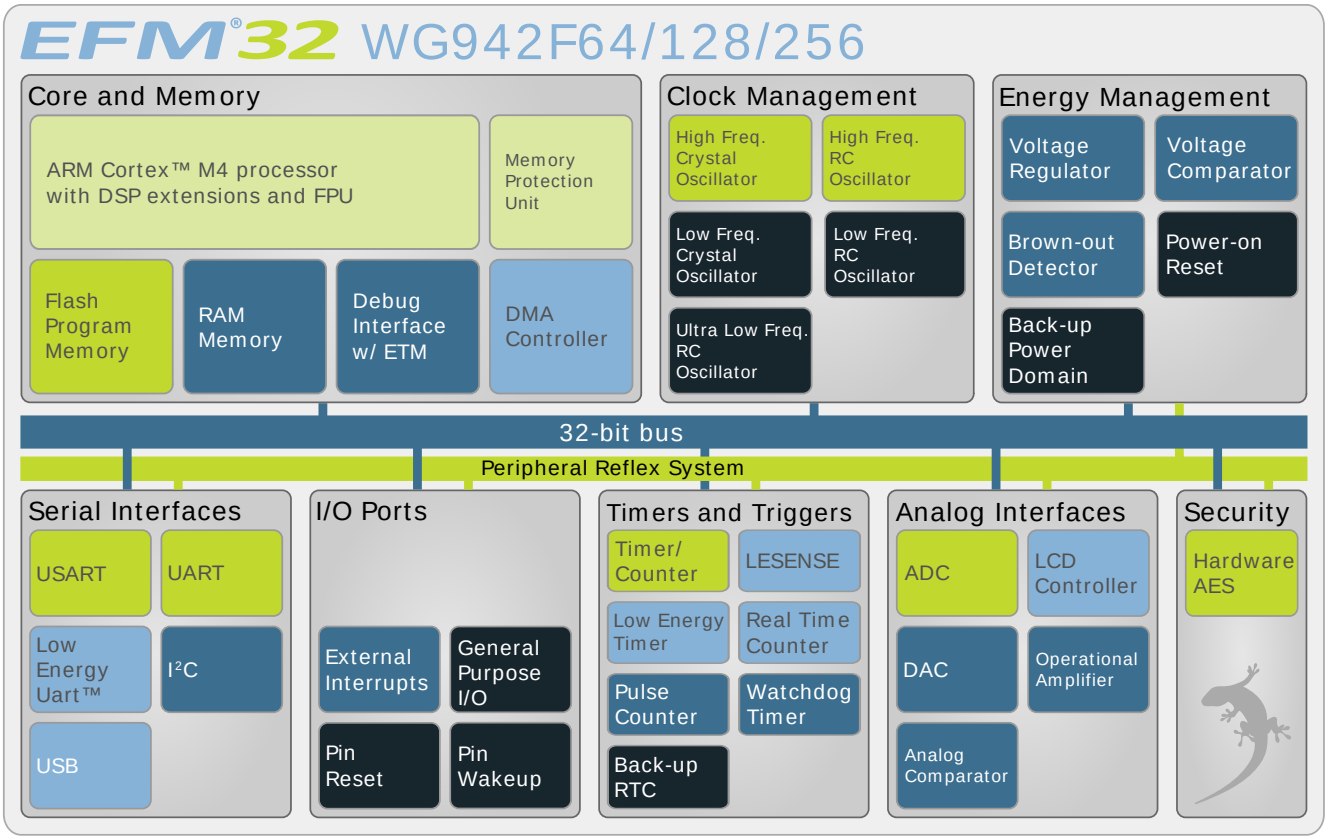
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M4, with DSP instruction support and floating-point unit, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32WG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32WG942 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32WG Reference Manual*.

A block diagram of the EFM32WG942 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M4 Core

The ARM Cortex-M4 includes a 32-bit RISC processor, with DSP instruction support and floating-point unit, which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep . The EFM32 implementation of the Cortex-M4 is described in detail in *ARM Cortex-M4 Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32WG microcontroller. The flash memory is readable and writable from both the Cortex-M4 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32WG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32WG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32WG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Universal Serial Bus Controller (USB)

The USB is a full-speed USB 2.0 compliant OTG host/device controller. The USB can be used in Device, On-the-go (OTG) Dual Role Device or Host-only configuration. In OTG mode the USB supports both Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation. The USB device includes an internal dedicated Descriptor-Based Scatter/Garther DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes all OTG features, except for the voltage booster for supplying 5V to VBUS when operating as host.

2.1.11 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.13 Pre-Programmed Serial Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.14 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.15 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.16 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.17 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

2.1.18 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms

with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.19 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

2.1.20 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.21 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.22 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

2.1.23 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has one single ended output buffer connected to channel 0. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.24 Operational Amplifier (OPAMP)

The EFM32WG942 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

2.1.25 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE™), is a highly configurable sensor interface with support for up to 4 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.26 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to

automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32WG942 to keep track of time and retain data, even if the main power source should drain out.

2.1.27 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.28 General Purpose Input/Output (GPIO)

In the EFM32WG942, there are 50 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.1.29 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

2.2 Configuration Summary

The features of the EFM32WG942 is a subset of the feature set described in the EFM32WG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Table 2.1. Configuration Summary

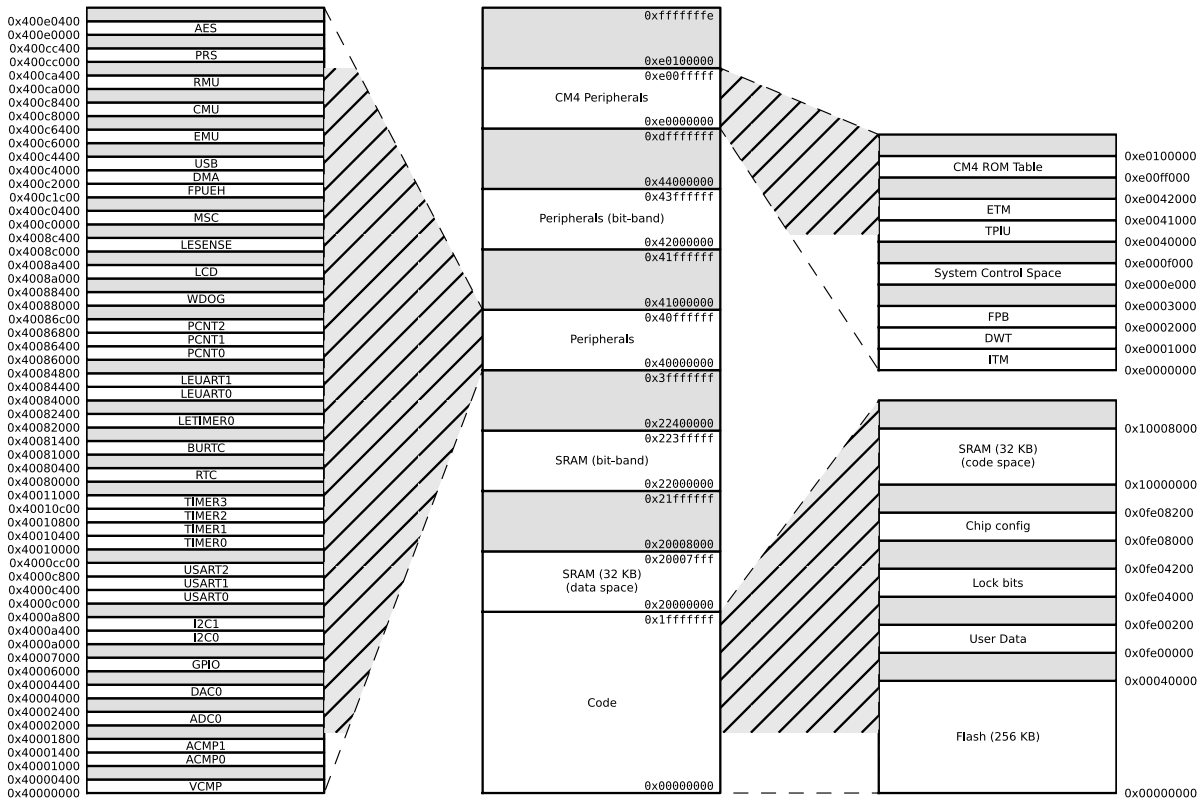
Module	Configuration	Pin Connections
Cortex-M4	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID

Module	Configuration	Pin Connections
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	I2S	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI.	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0		PCNT0_S[1:0]
PCNT1	8-bit count register	PCNT1_S[1:0]
PCNT2	8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[3:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP		
AES	Full configuration	NA
GPIO	50 pins	Available pins are shown in Table 4.3 (p. 62)
LCD	Full configuration	LCD_SEG[15:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

2.3 Memory Map

The *EFM32WG942* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32WG942 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 10), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 10), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 10) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 10) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150[1]	°C
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

[1]Based on programmed devices tested for 10000 hours at 150ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	°C
V_{DDOP}	Operating supply voltage	1.85		3.8	V
f_{APB}	Internal APB clock frequency			48	MHz
f_{AHB}	Internal AHB clock frequency			48	MHz

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ESDHBM}	ESD (Human Body Model HBM)	T_{AMB}=25°C			2	kV
V_{ESDCDM}	ESD (Charged Device Model, CDM)	T_{AMB}=25°C			1	kV

Latch-up sensitivity test passed level A according to JEDEC JESD 78B method Class II, 85°C.

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		229		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		230		µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		232		µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		234		µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		236		µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		242		µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		276		µA/MHz
I_{EM1}	EM1 current	48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		66		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		67		µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		68		µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		70		µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		72		µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		77		µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V		110		µA/MHz
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C		0.95[1]		µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		3.0[1]		µA
I_{EM3}	EM3 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.65		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		2.65		µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.44		µA

[1]Using backup RTC.

3.4.1 EM0 Current Consumption

Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFXO running at 48MHz

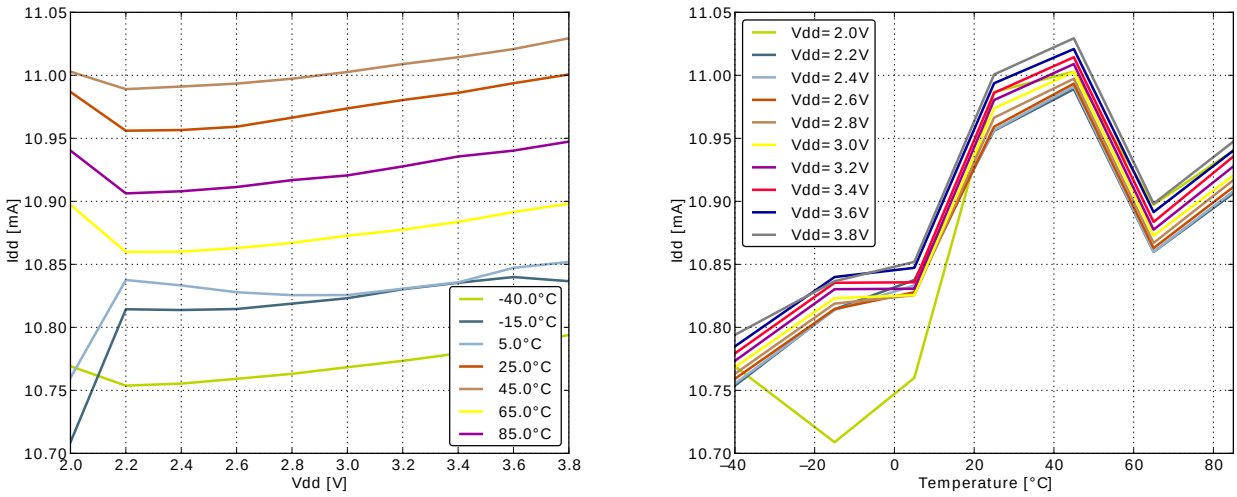


Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28MHz

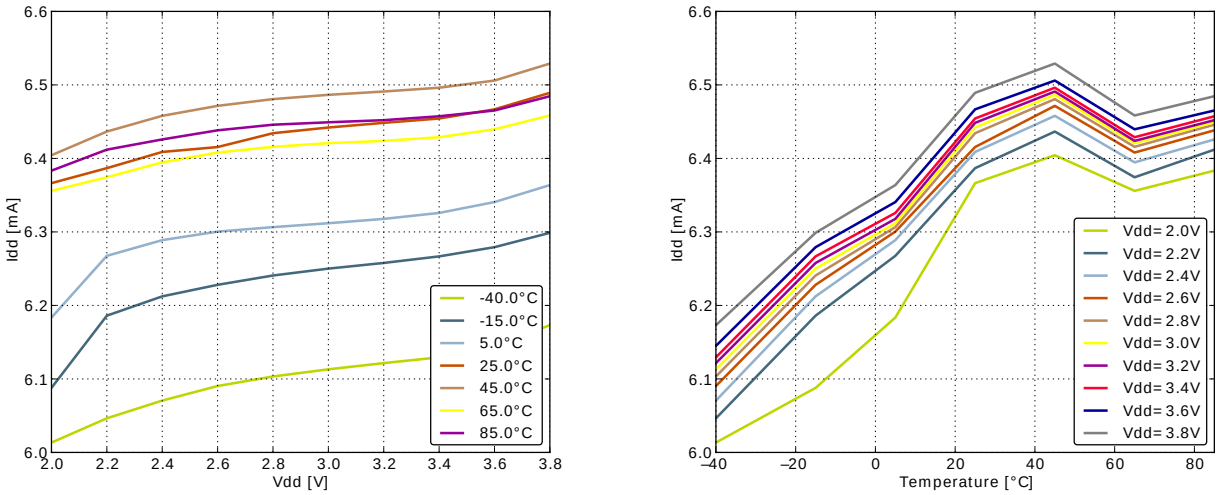


Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21MHz

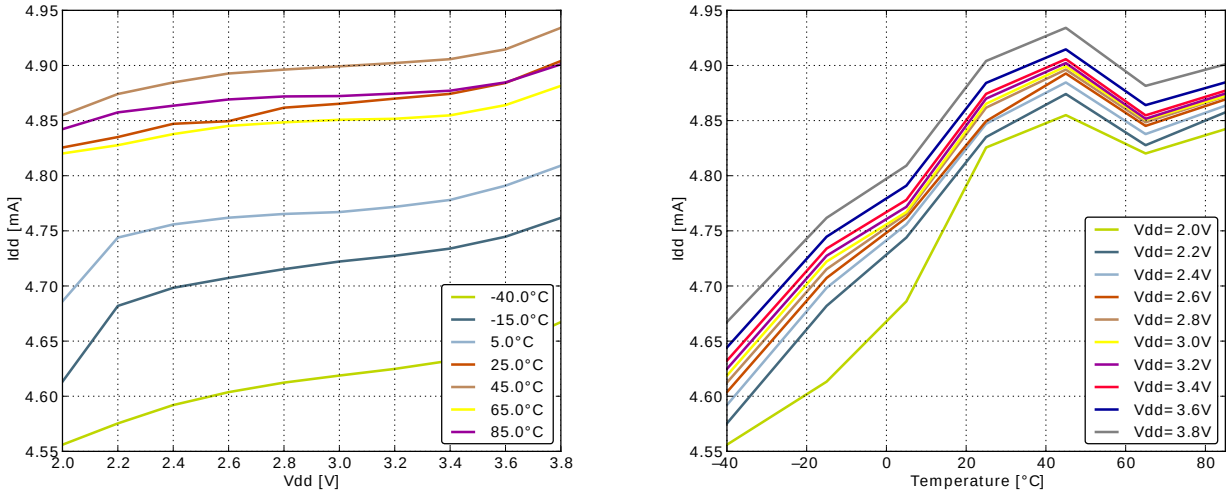


Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14MHz

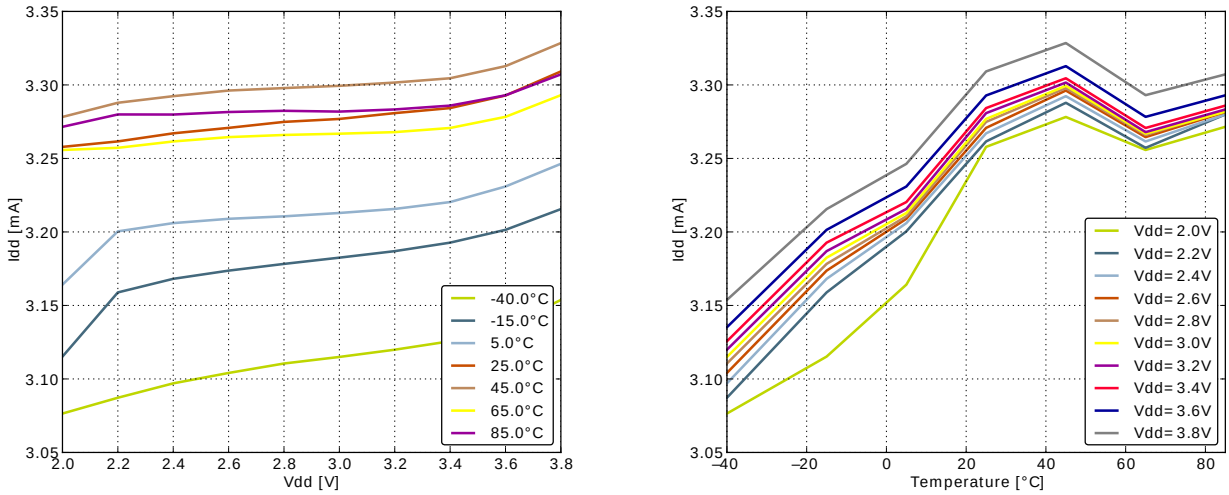


Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11MHz

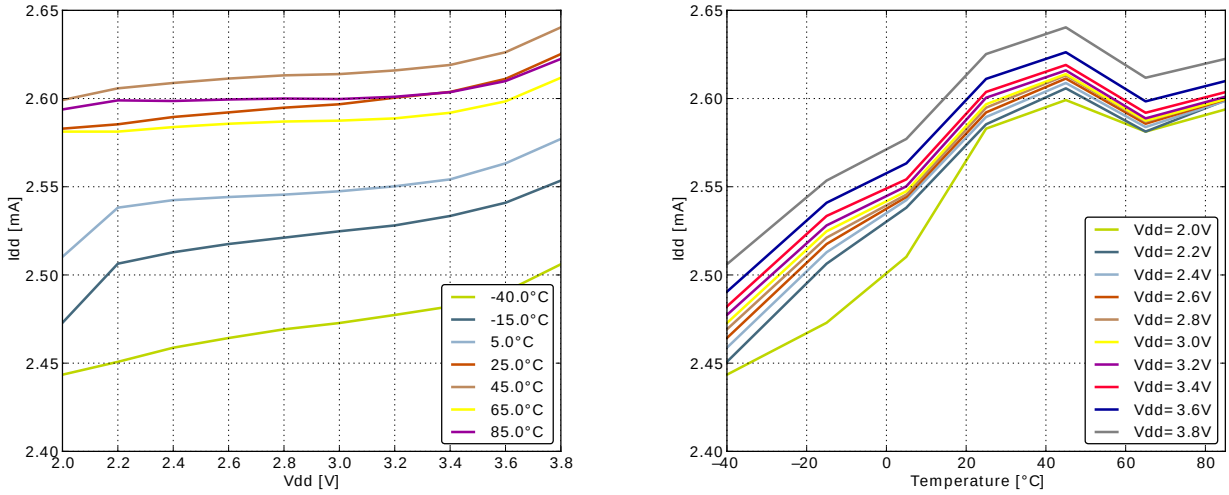
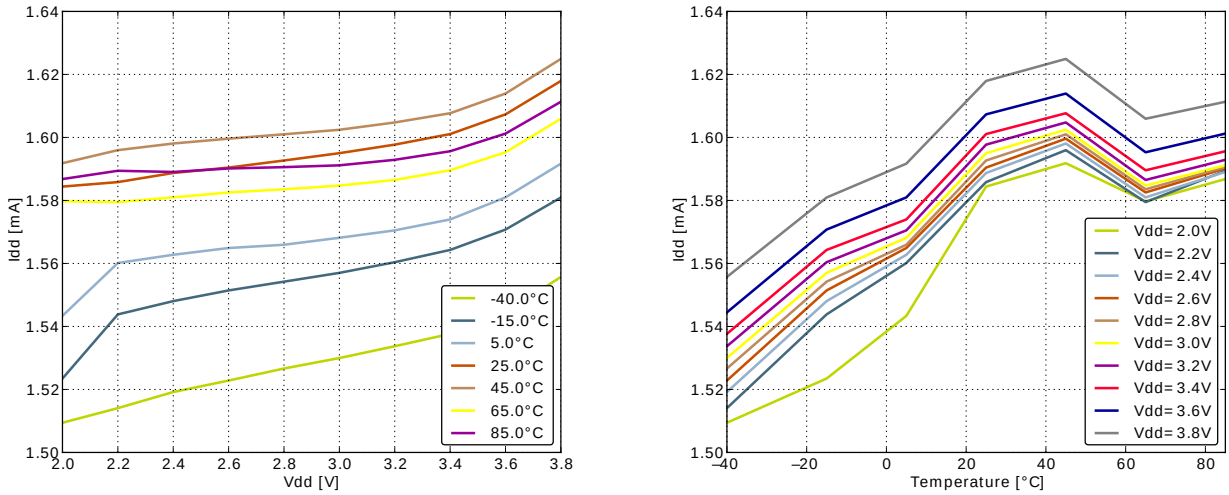


Figure 3.6. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 7MHz



3.4.2 EM1 Current Consumption

Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFXO running at 48MHz

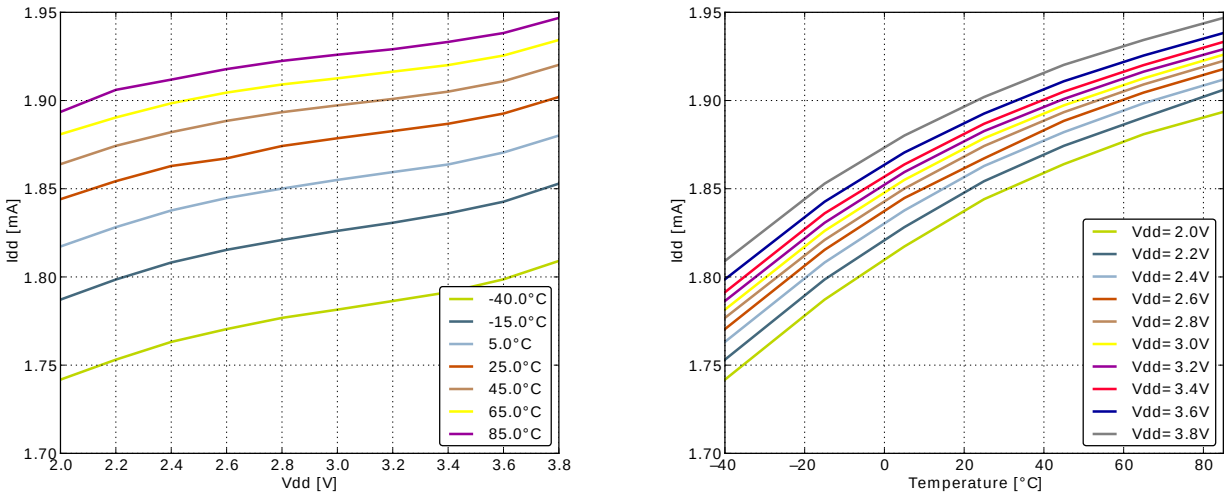


Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28MHz

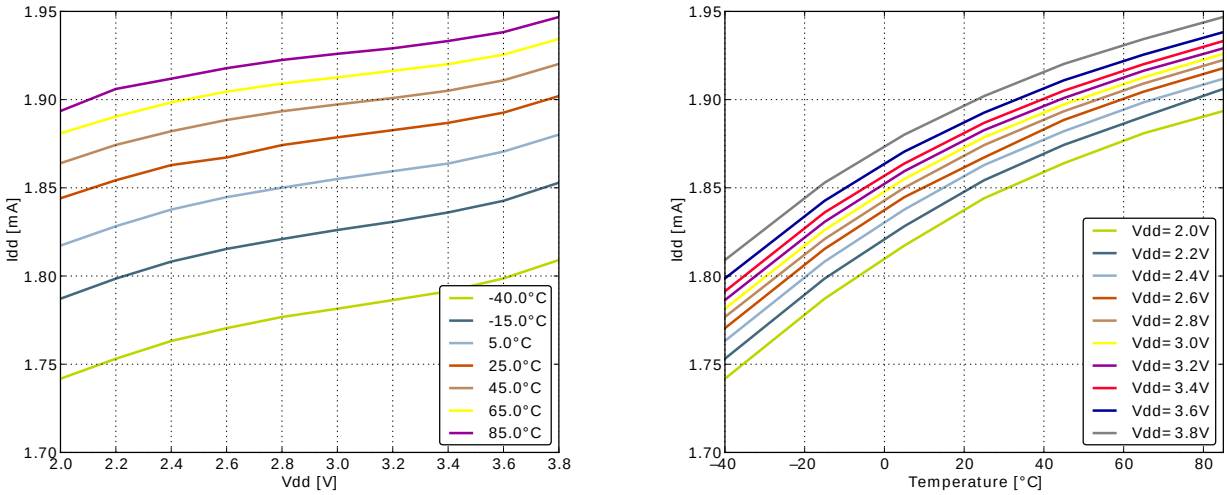


Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21MHz

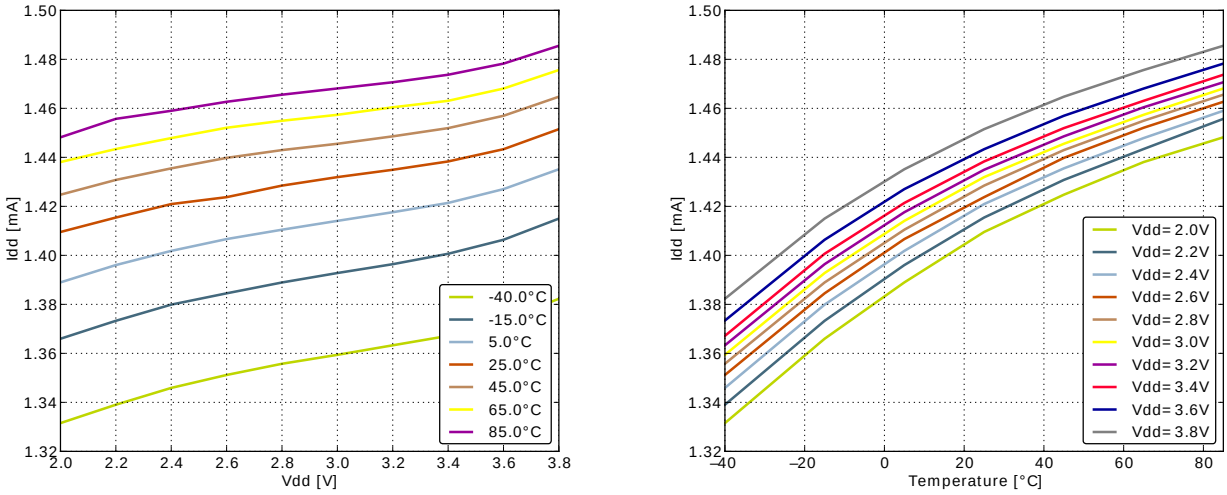


Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14MHz

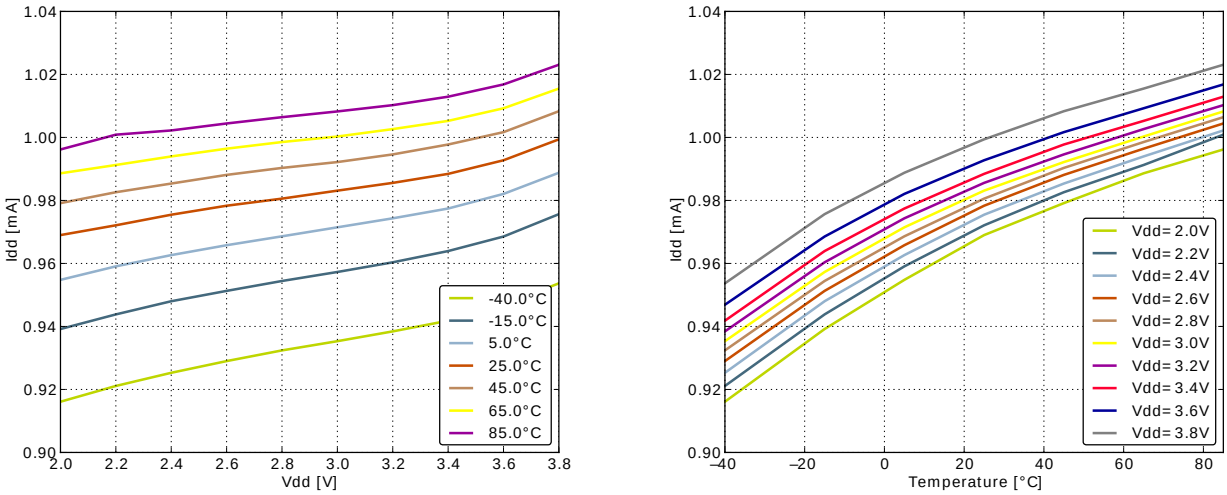


Figure 3.11. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

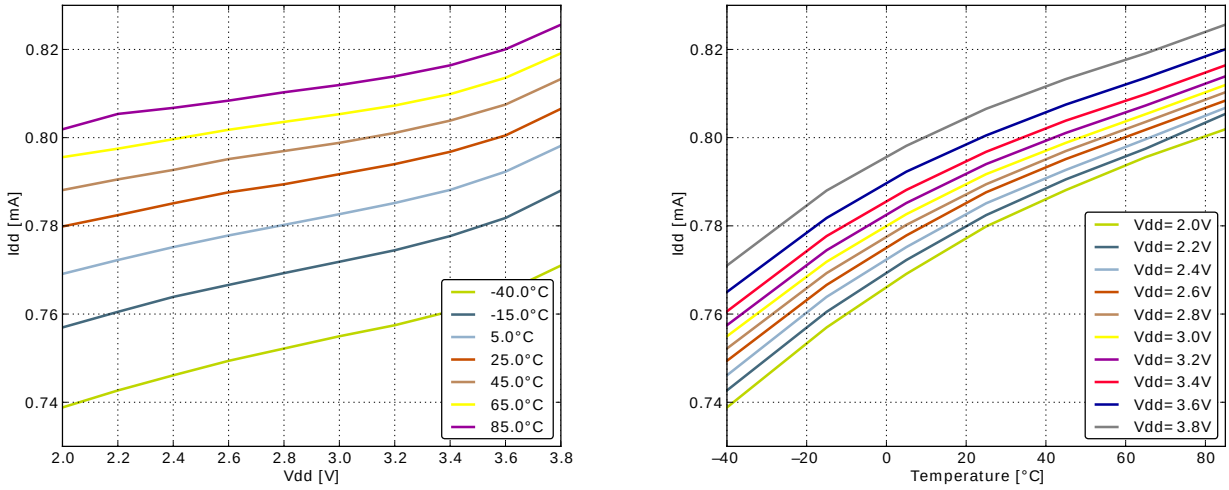
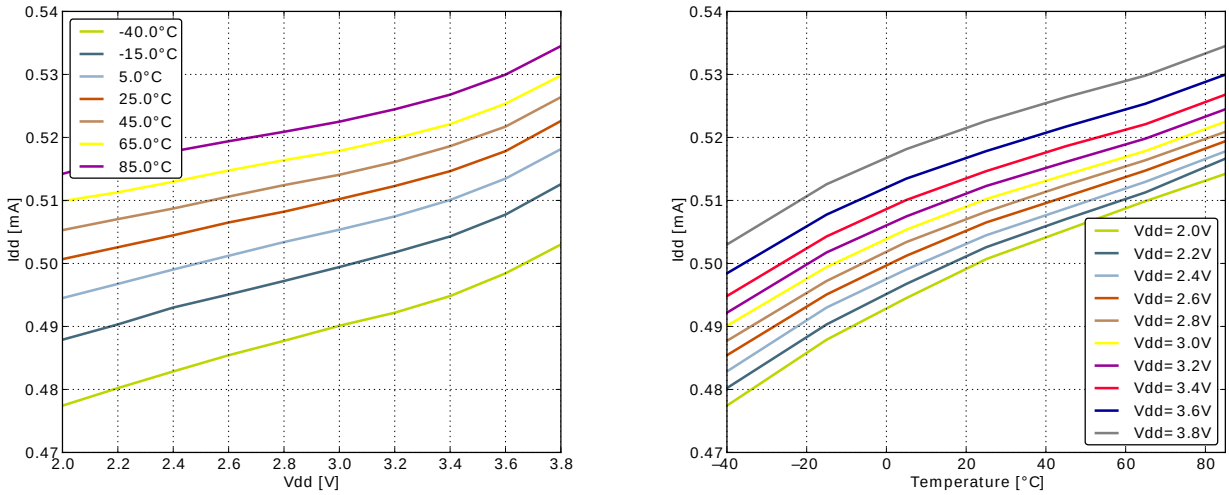
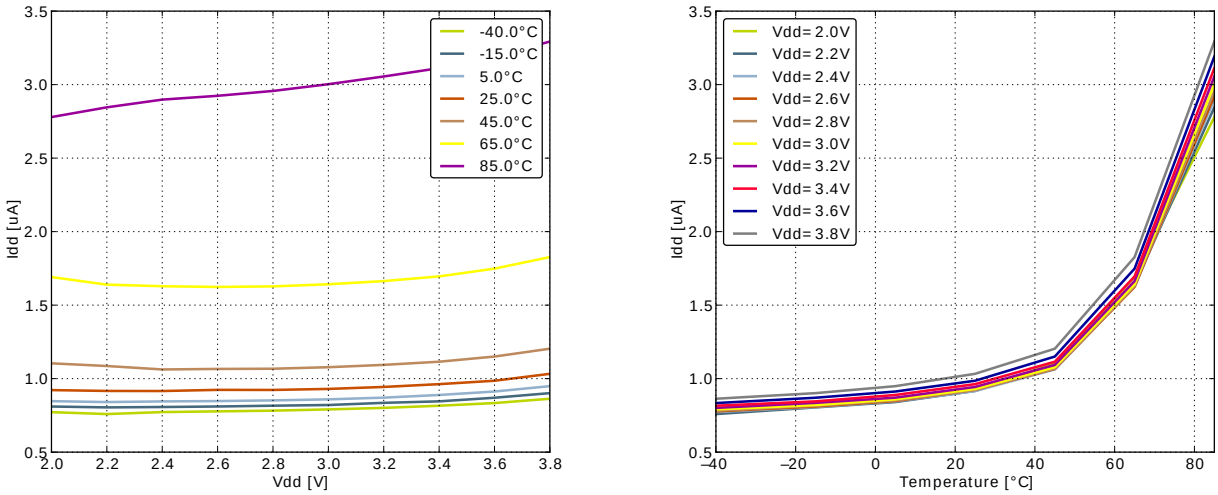


Figure 3.12. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 7MHz



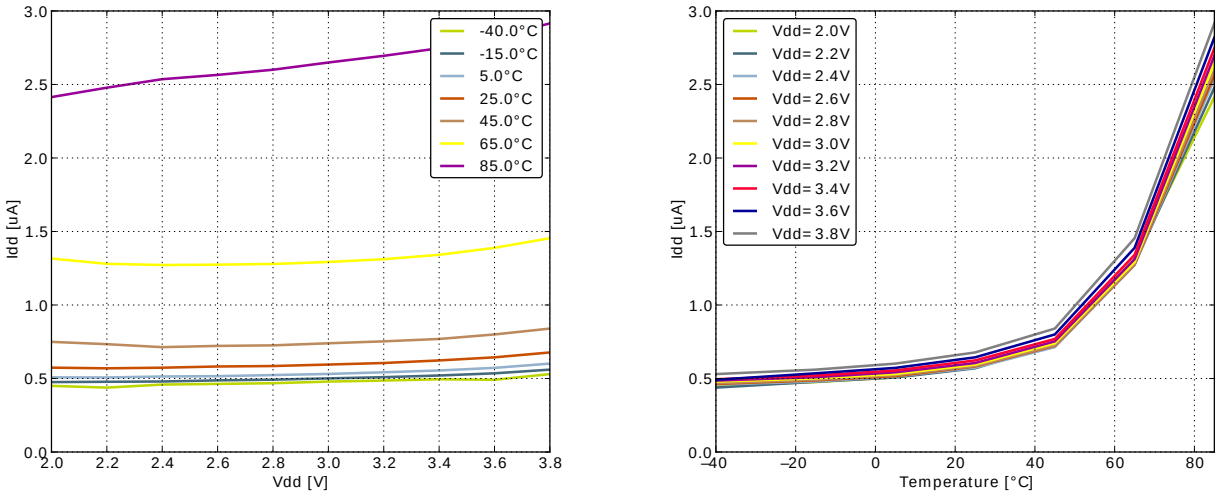
3.4.3 EM2 Current Consumption

Figure 3.13. EM2 current consumption. RTC[1] prescaled to 1kHz, 32 kHz LFRCO.



3.4.4 EM3 Current Consumption

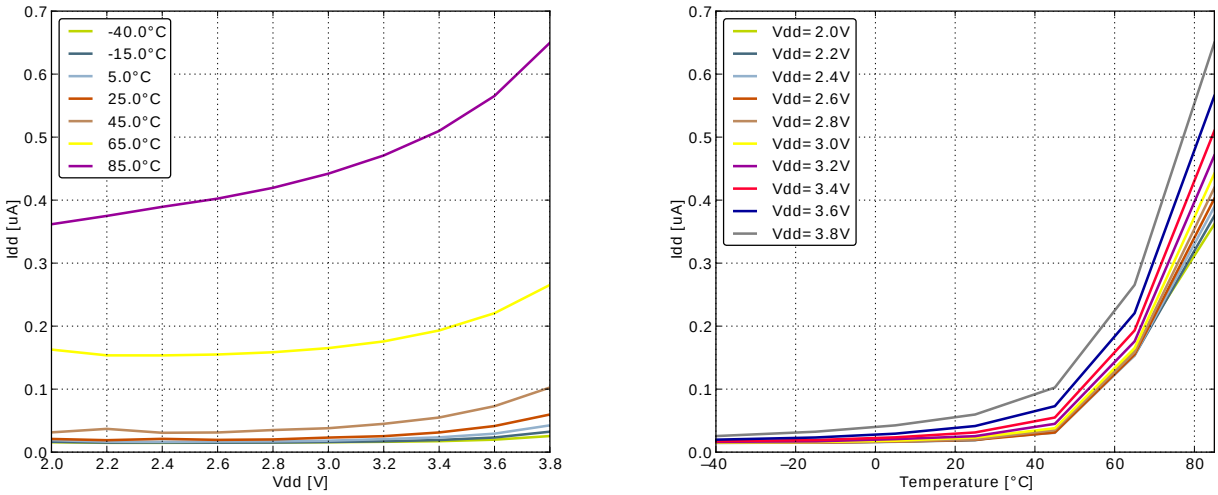
Figure 3.14. EM3 current consumption.



[1]Using backup RTC.

3.4.5 EM4 Current Consumption

Figure 3.15. EM4 current consumption.



3.5 Transition between Energy Modes

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0[1]		HF core CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

[1]Core wakeup time only.

3.6 Power Management

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.82		1.85	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.62		1.68	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85		V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF
C_{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		µF
C_{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		µF

3.7 Flash

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{PERASE}	Page erase time	< 512KB	20	20.4	20.8	ms
		>= 512KB, LPERASE == 0	20	20.4	20.8	ms
		>= 512KB, LPERASE == 1	40	40.4	40.8	ms
t_{DERASE}	Device erase time	< 512KB	40	40.8	41.6	ms
		>= 512KB			161.6	ms
I_{ERASE}	Erase current	< 512KB			7[1]	mA
		>= 512KB, LPERASE == 0			14[1]	mA
		>= 512KB, LPERASE == 1			7[1]	mA
I_{WRITE}	Write current	< 512KB			7[1]	mA
		>= 512KB, LPWRITE == 0			14[1]	mA
		>= 512KB, LPWRITE == 1			7[1]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.8		3.8	V

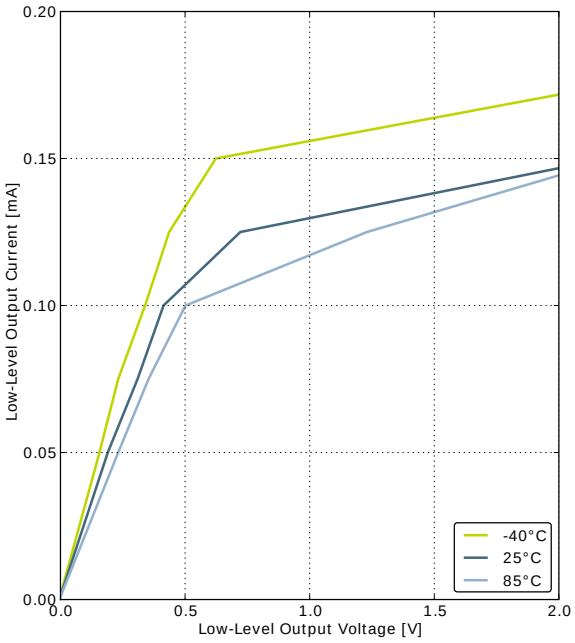
[1]Measured at 25°C

3.8 General Purpose Input Output

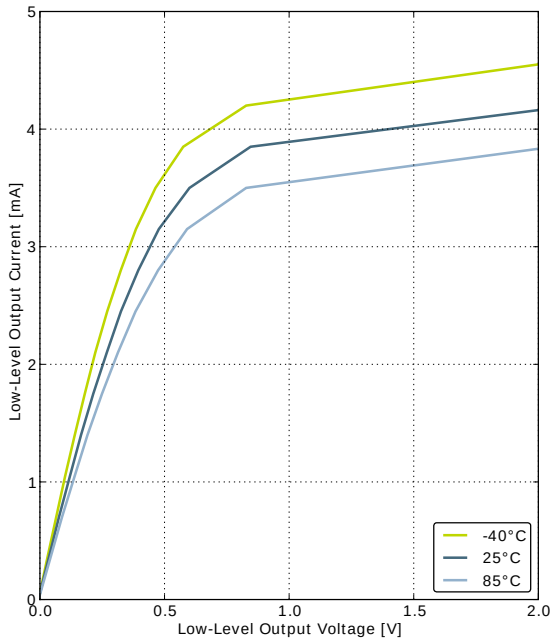
Table 3.8. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IOIL}	Input low voltage				$0.3V_{DD}$	V
V_{IOIH}	Input high voltage		$0.7V_{DD}$			V
V_{IOOH}	Output high voltage	Sourcing 6 mA, V_{DD}=1.85V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75V_{DD}$			V
		Sourcing 6 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.95V_{DD}$			V
		Sourcing 20 mA, V_{DD}=1.85V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.7V_{DD}$			V
		Sourcing 20 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.9V_{DD}$			V
V_{IOOL}	Output low voltage	Sinking 6 mA, V_{DD}=1.85V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.25V_{DD}$	V
		Sinking 6 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.05V_{DD}$	V
		Sinking 20 mA, V_{DD}=1.85V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.3V_{DD}$	V
		Sinking 20 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.1V_{DD}$	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd			+/-25	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	0.5 mA drive strength and load capacitance C_L=12.5-25pF.	$20+0.1C_L$		250	ns
		2mA drive strength and load capacitance C_L=350-600pF	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.85 - 3.8 V	$0.1V_{DD}$			V

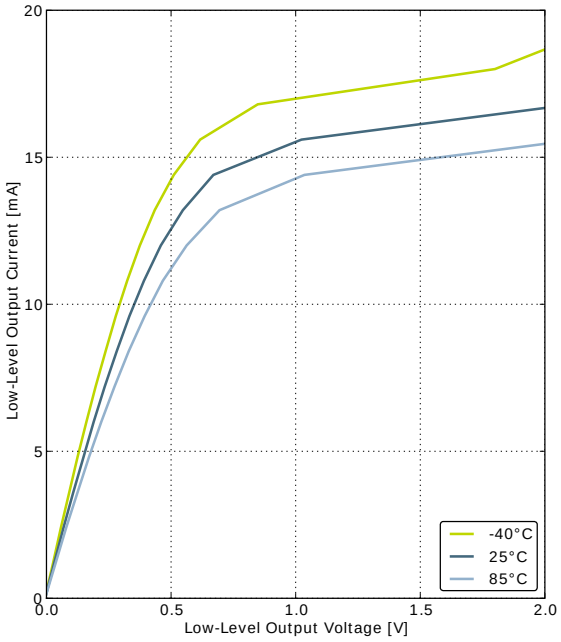
Figure 3.16. Typical Low-Level Output Current, 2V Supply Voltage



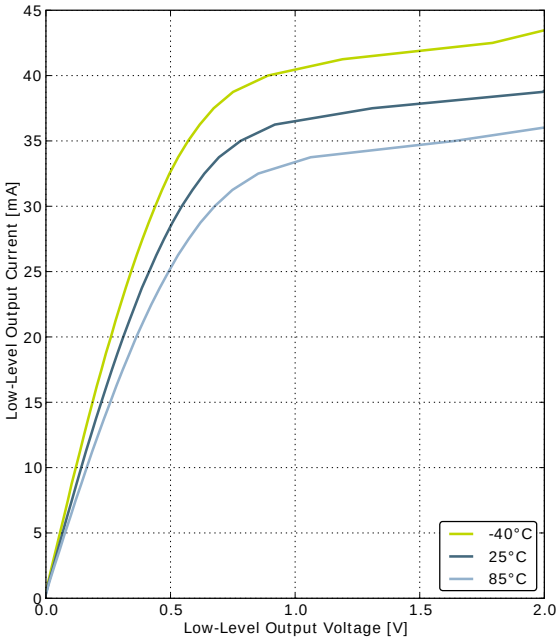
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

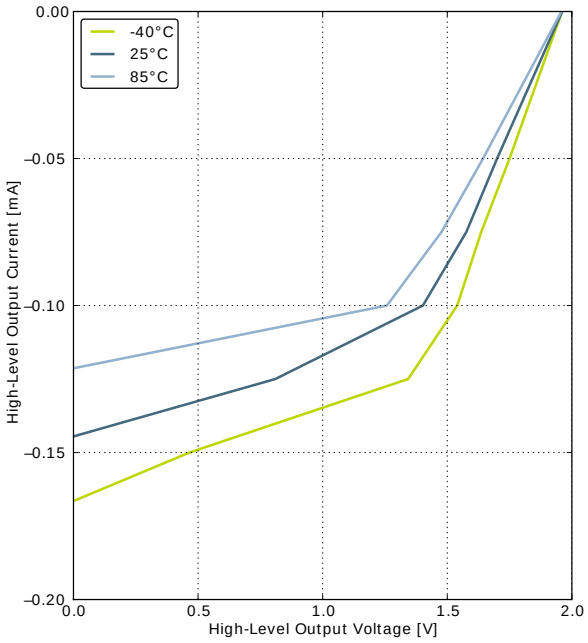


GPIO_Px_CTRL DRIVEMODE = STANDARD

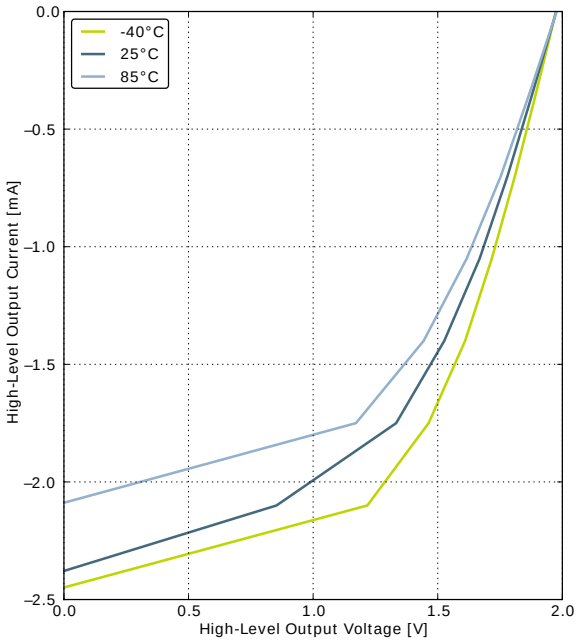


GPIO_Px_CTRL DRIVEMODE = HIGH

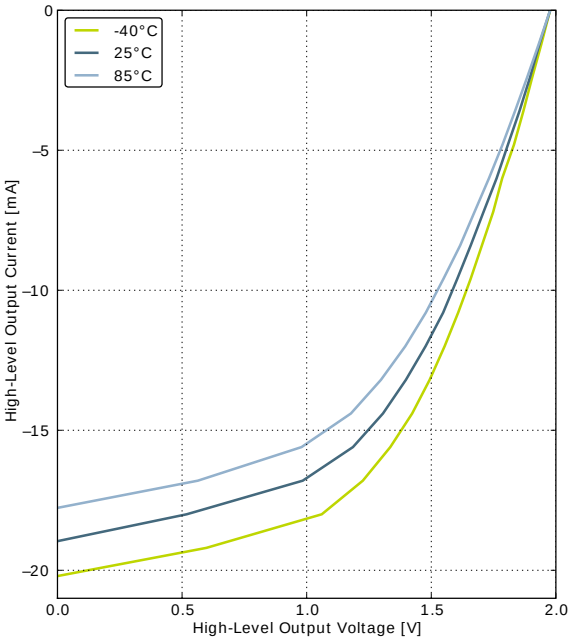
Figure 3.17. Typical High-Level Output Current, 2V Supply Voltage



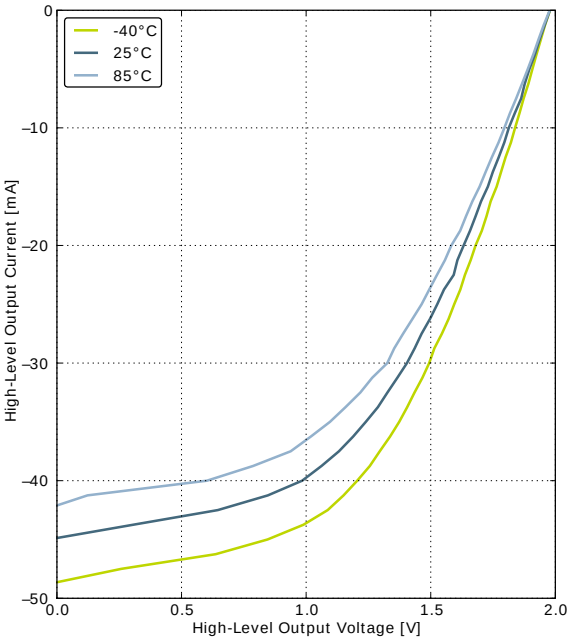
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

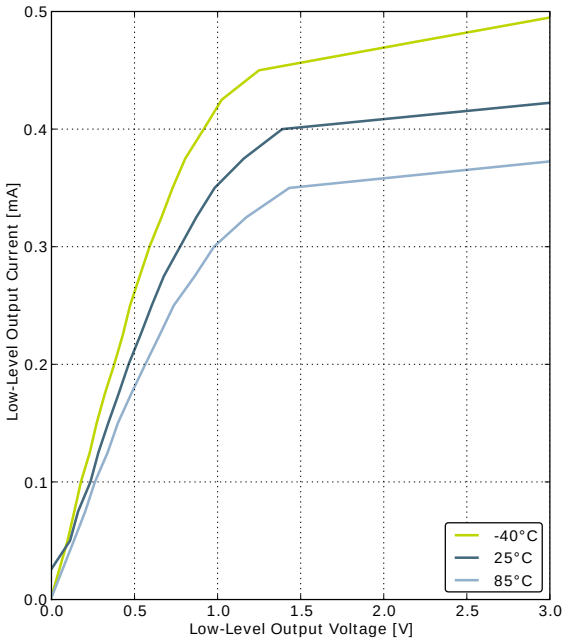


GPIO_Px_CTRL DRIVEMODE = STANDARD

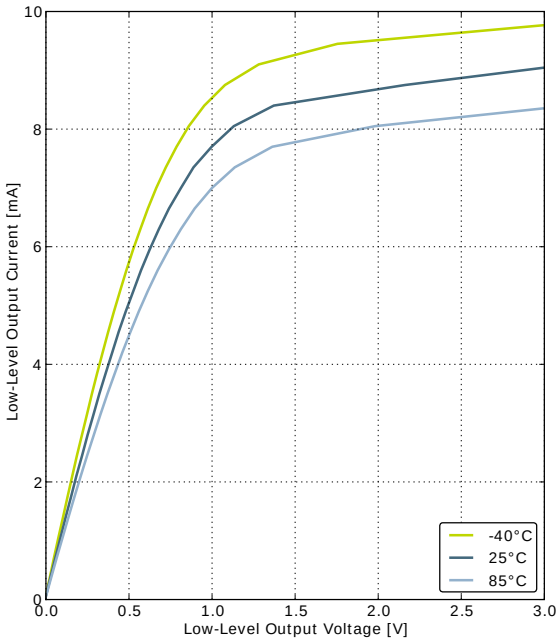


GPIO_Px_CTRL DRIVEMODE = HIGH

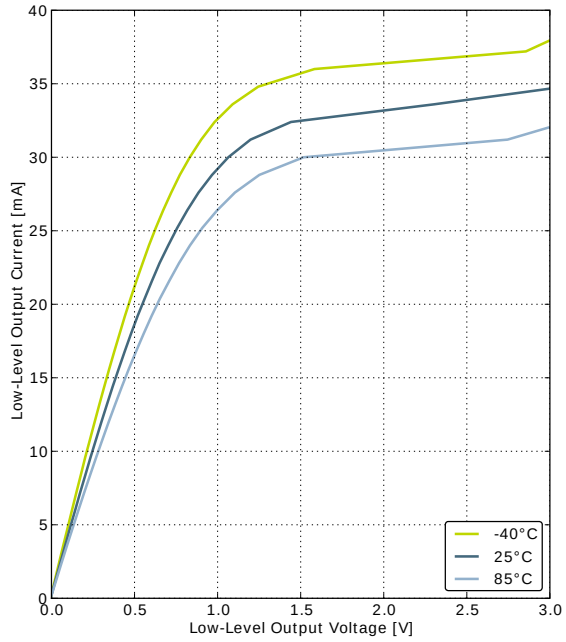
Figure 3.18. Typical Low-Level Output Current, 3V Supply Voltage



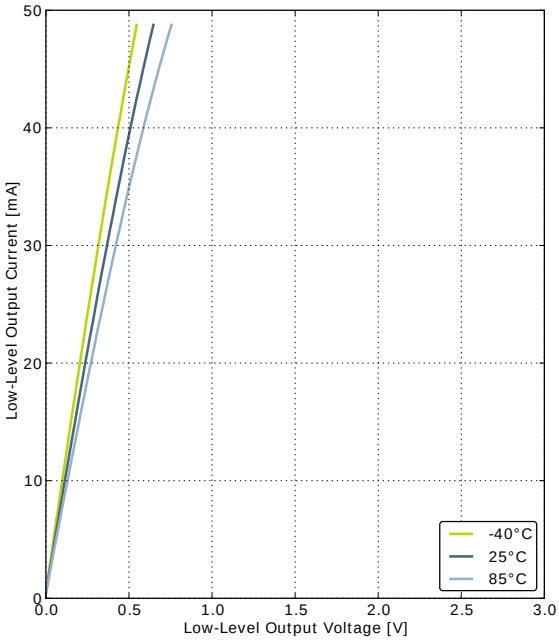
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

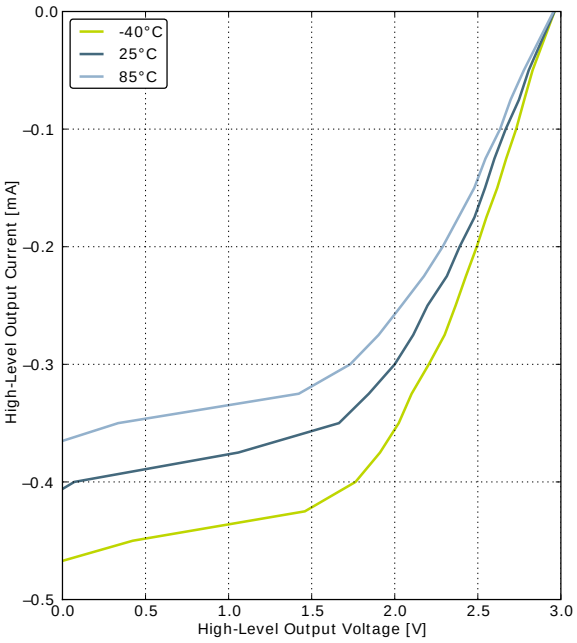


GPIO_Px_CTRL DRIVEMODE = STANDARD

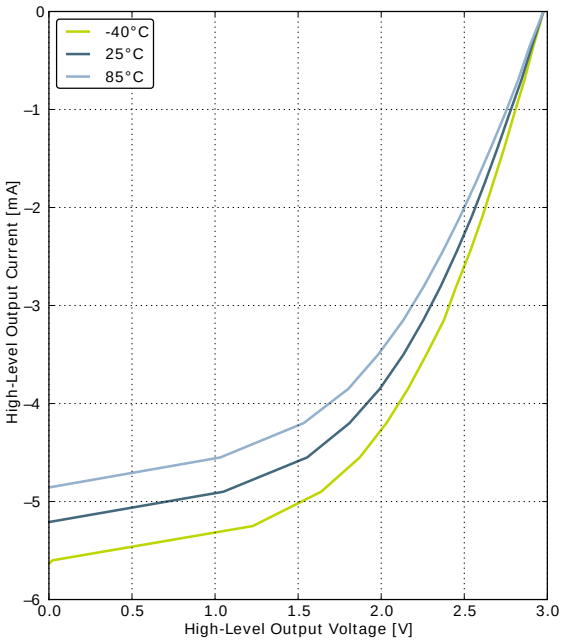


GPIO_Px_CTRL DRIVEMODE = HIGH

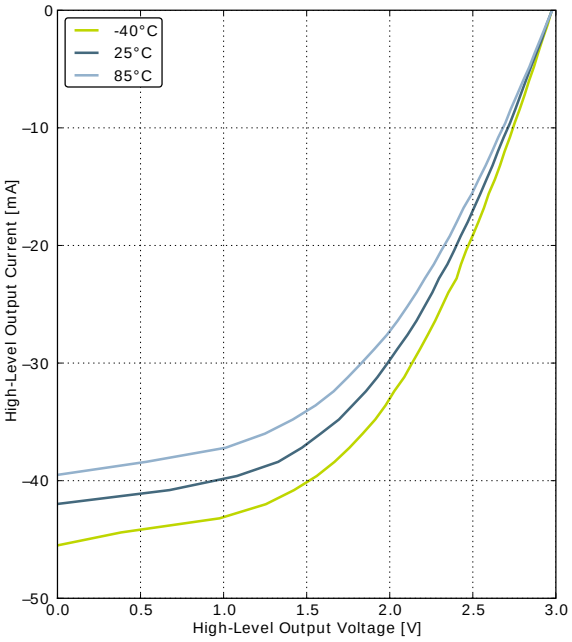
Figure 3.19. Typical High-Level Output Current, 3V Supply Voltage



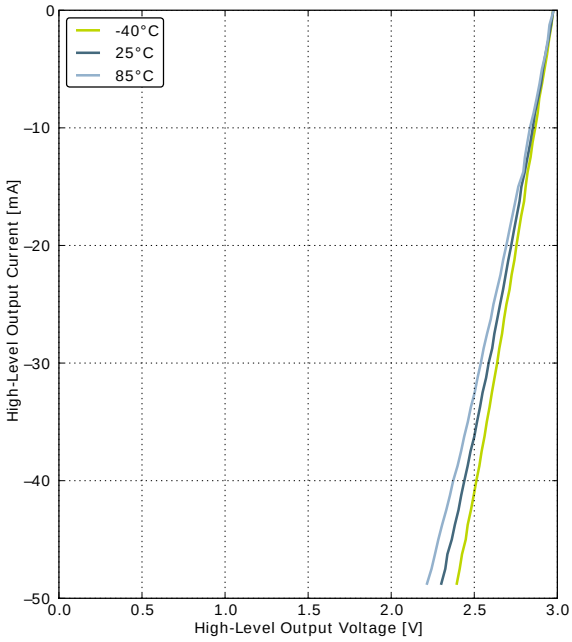
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

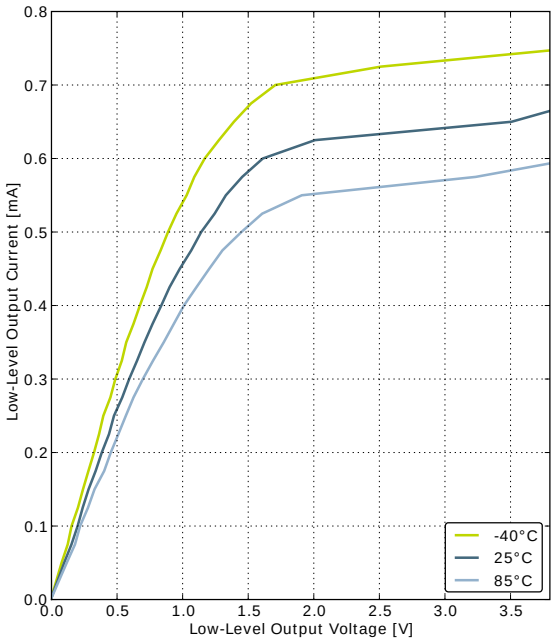


GPIO_Px_CTRL DRIVEMODE = STANDARD

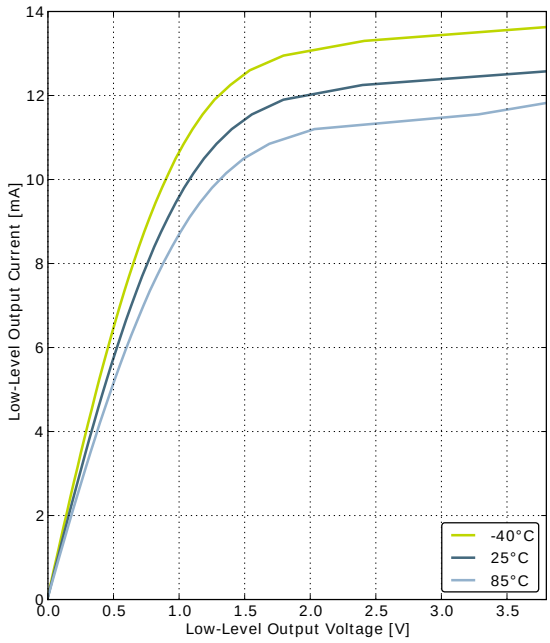


GPIO_Px_CTRL DRIVEMODE = HIGH

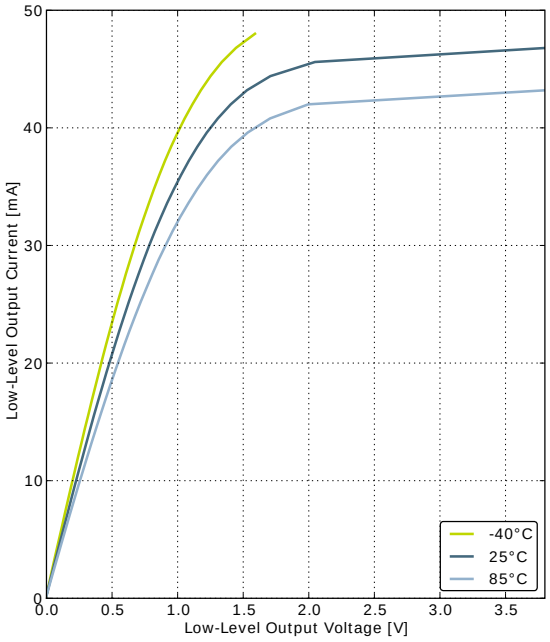
Figure 3.20. Typical Low-Level Output Current, 3.8V Supply Voltage



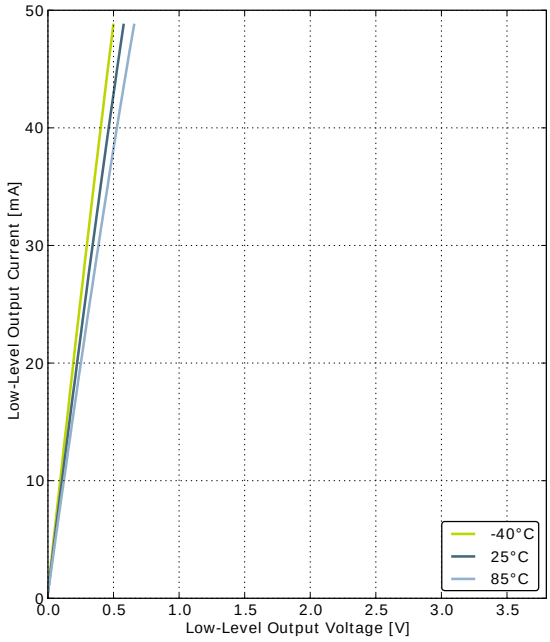
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

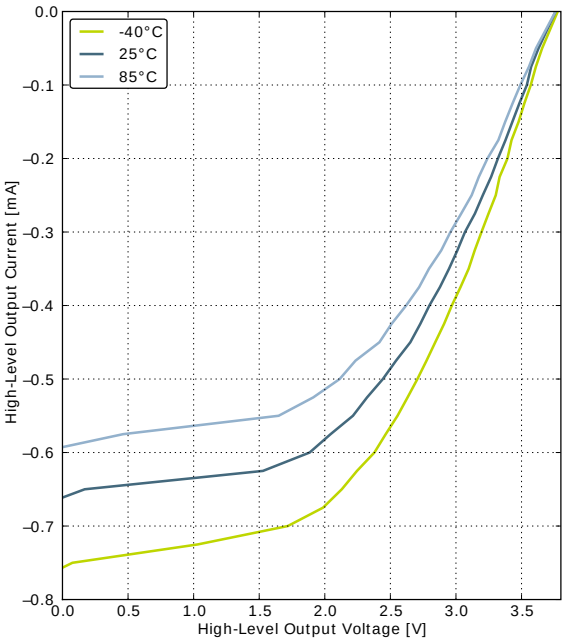


GPIO_Px_CTRL DRIVEMODE = STANDARD

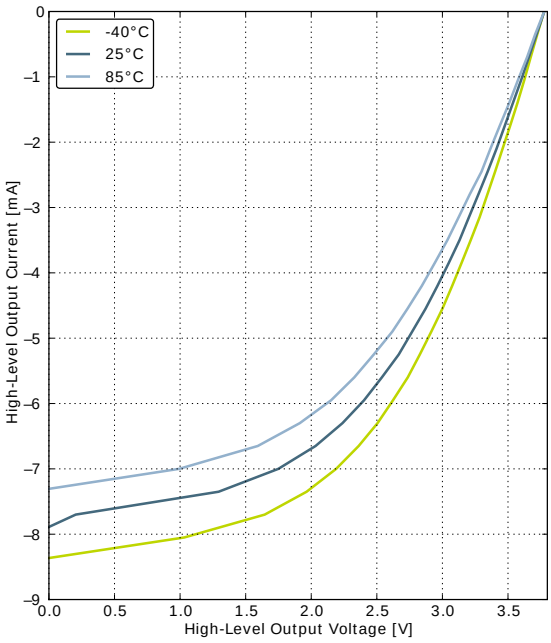


GPIO_Px_CTRL DRIVEMODE = HIGH

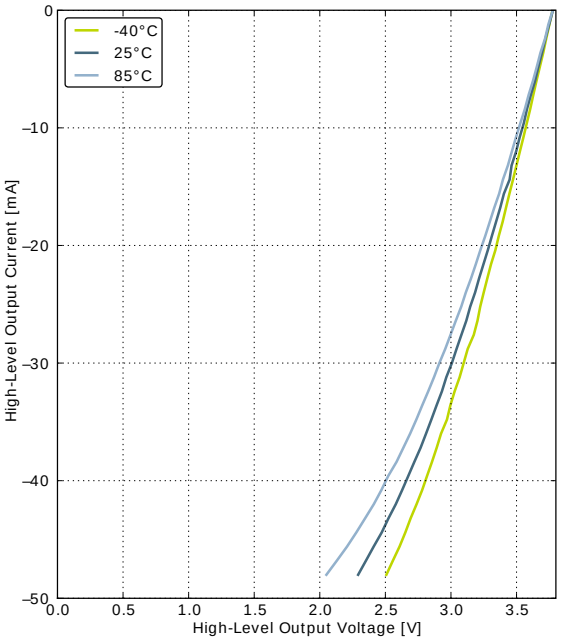
Figure 3.21. Typical High-Level Output Current, 3.8V Supply Voltage



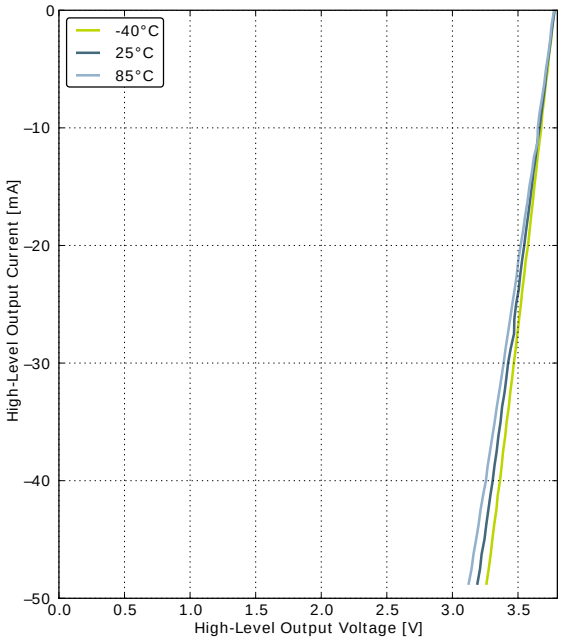
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after start-up.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

For safe startup of a given crystal, the load capacitance should be larger than the value indicated in Figure 3.22 (p. 30) and in Table 3.10 (p. 31) for a given LFXOBOOST setting. The minimum supported load capacitance depends on the crystal shunt capacitance, C_0, which is specified in crystal vendors' datasheet.

Figure 3.22. Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup

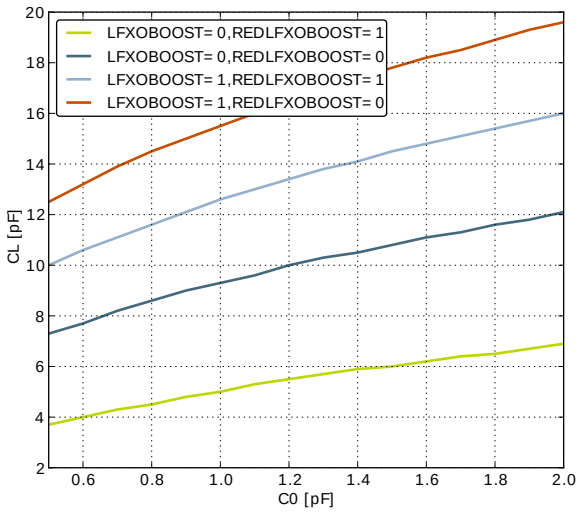


Table 3.10. Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup

Symbol	Capacitance [pF]															
Shunt Capacitance C_0	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0
CL_{min} lfxoboost = 0 redlfxoboost = 1	3.7	4.0	4.3	4.5	4.8	5.0	5.3	5.5	5.7	5.9	6.0	6.2	6.4	6.5	6.7	6.9
CL_{min} lfxoboost = 1 redlfxoboost = 0	7.3	7.7	8.2	8.6	9.0	9.3	9.6	10.0	10.3	10.5	10.8	11.1	11.3	11.6	11.8	12.1
CL_{min} lfxoboost = 1 redlfxoboost = 1	10.0	10.6	11.1	11.6	12.1	12.6	13.0	13.4	13.8	14.1	14.5	14.8	15.1	15.4	15.7	16.0
CL_{min} lfxoboost = 1 redlfxoboost = 0	12.5	13.2	13.9	14.5	15.0	15.5	16.0	16.5	16.9	17.4	17.8	18.2	18.5	18.9	19.3	19.6

3.9.2 HFXO

Table 3.11. HFXO

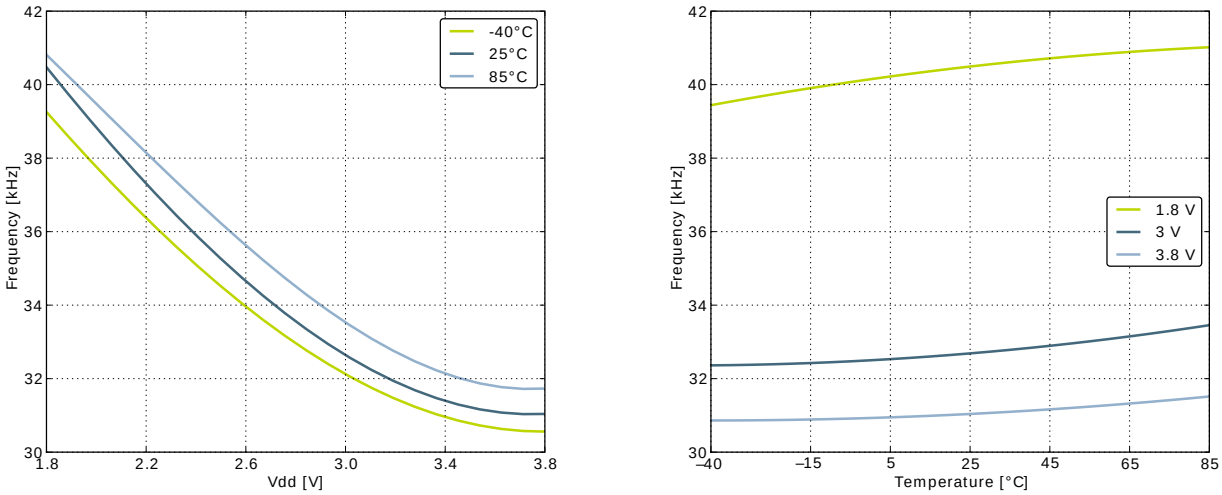
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		48	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
DC_{HFXO}	Duty cycle		46	50	54	%
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

3.9.3 LFRCO

Table 3.12. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C			32.768		kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			190		nA
$TUNESTEP_{L-FRCO}$	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.23. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



3.9.4 HFRCO

Table 3.13. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	28 MHz frequency band		28		MHz
		21 MHz frequency band		21		MHz
		14 MHz frequency band		14		MHz
		11 MHz frequency band		11		MHz
		7 MHz frequency band		6.6		MHz
		1 MHz frequency band		1.2		MHz
$t_{HFRCO_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
I_{HFRCO}	Current consumption	f_{HFRCO} = 28 MHz		106		µA
		f_{HFRCO} = 21 MHz		93		µA
		f_{HFRCO} = 14 MHz		77		µA
		f_{HFRCO} = 11 MHz		72		µA
		f_{HFRCO} = 6.6 MHz		63		µA
		f_{HFRCO} = 1.2 MHz		22		µA
DC_{HFRCO}	Duty cycle	f_{HFRCO} = 14 MHz	48.5	50	51	%
$TUNESTEP_{H-FRCO}$	Frequency step for LSB change in TUNING value			0.3		%

Figure 3.24. Calibrated HFRCO 11 MHz Band Frequency vs Temperature and Supply Voltage

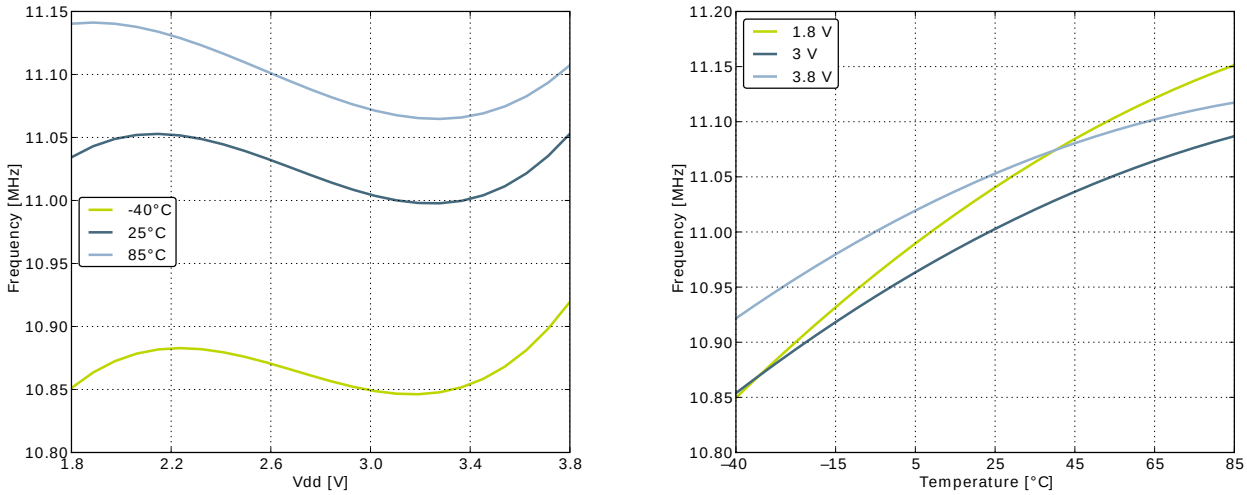


Figure 3.25. Calibrated HFRCO 14 MHz Band Frequency vs Temperature and Supply Voltage

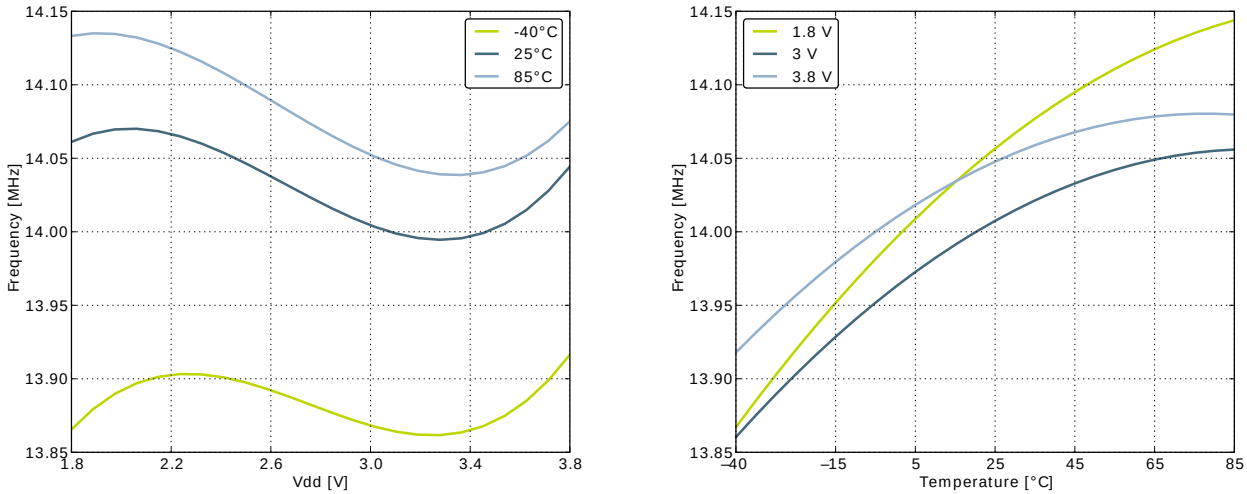


Figure 3.26. Calibrated HFRCO 21 MHz Band Frequency vs Temperature and Supply Voltage

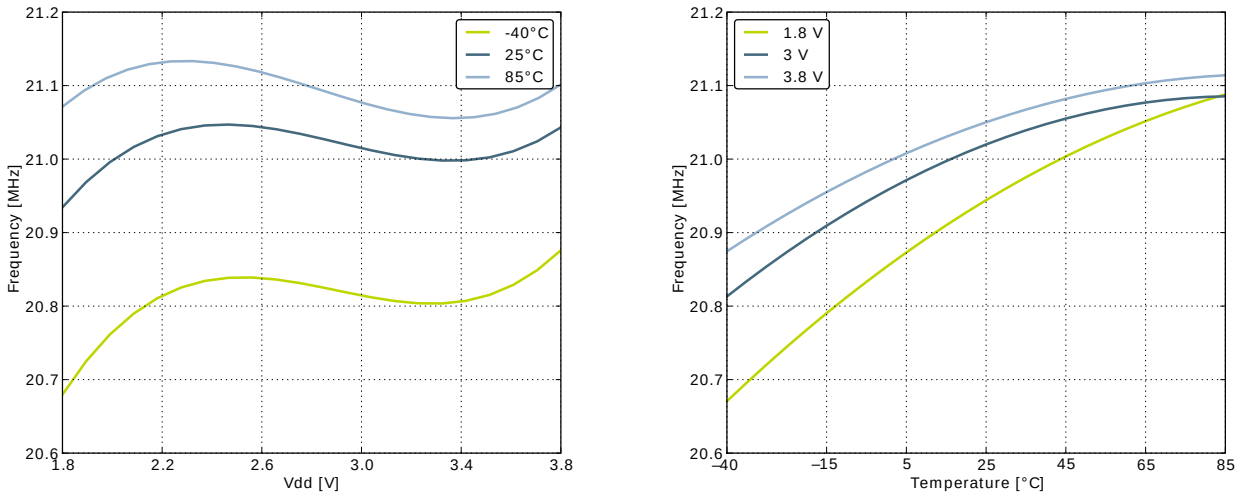
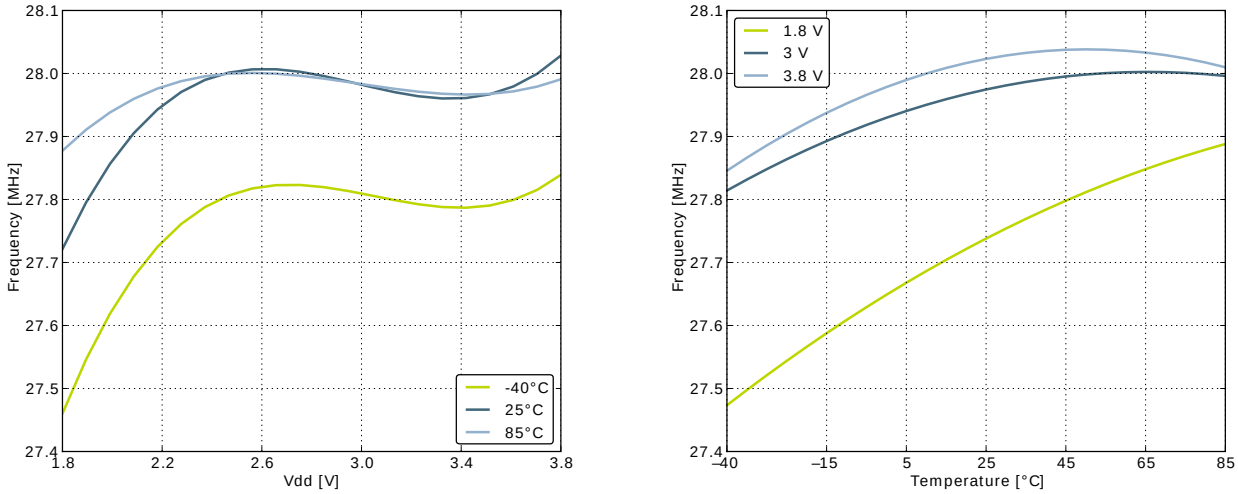


Figure 3.27. Calibrated HFRCO 28 MHz Band Frequency vs Temperature and Supply Voltage



3.9.5 ULFRCO

Table 3.14. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.8		1.5	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.15. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0		V_{REF}	V
		Differential	$-V_{REF}/2$		$V_{REF}/2$	V
$V_{ADCREFIN}$	Input range of external reference voltage, single ended and differential		1.25		V_{DD}	V
$V_{ADCREFIN_CH7}$	Input range of external negative reference voltage on channel 7	See $V_{ADCREFIN}$	0		V_{DD} - 1.1	V
$V_{ADCREFIN_CH6}$	Input range of external positive reference voltage on channel 6	See $V_{ADCREFIN}$	0.625		V_{DD}	V
$V_{ADCCMIN}$	Common mode input range		0		V_{DD}	V
I_{ADCIN}	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		351		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-		67		µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		MODE in ADCn_CTRL set to 0b00				
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		63		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		64		µA
I_{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		µA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCFILT}$	Input RC filter resistance			10		kOhm
$C_{ADCFILT}$	Input RC filter/decoupling capacitance			250		fF
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADC-CLK Cycles
		10 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			µs
$t_{ADCSTART}$	Startup time of reference generator and ADC core in NORMAL mode			5		µs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		µs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		67		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		69		dB
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		70		dB
$SNDR_{ADC}$	Signal to Noise-puls-Distortion Ratio (SNDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		68		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference		79		dBc

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended		0.3		mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/ °C
DNL_{ADC}	Differential non-linearity (DNL)			±0.7		LSB
INL_{ADC}	Integral non-linearity (INL), End point method			±1.2		LSB
MC_{ADC}	No missing codes		11.999[1]	12		bits
$GAIN_{ED}$	Gain error drift	1.25V reference		0.01[2]	0.033[3]	%/°C
		2.5V reference		0.01[2]	0.03[3]	%/°C
$OFFSET_{ED}$	Offset error drift	1.25V reference		0.2[2]	0.7[3]	LSB/°C
		2.5V reference		0.2[2]	0.62[3]	LSB/°C

[1]On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

[2]Typical numbers given by abs(Mean) / (85 - 25).

[3]Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.28 (p. 38) and Figure 3.29 (p. 39) , respectively.

Figure 3.28. Integral Non-Linearity (INL)

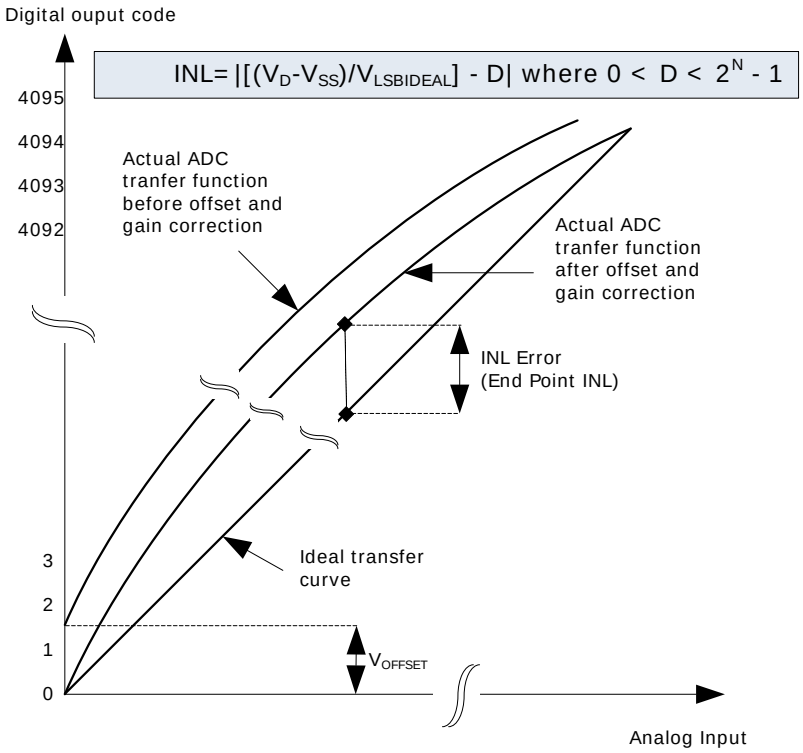
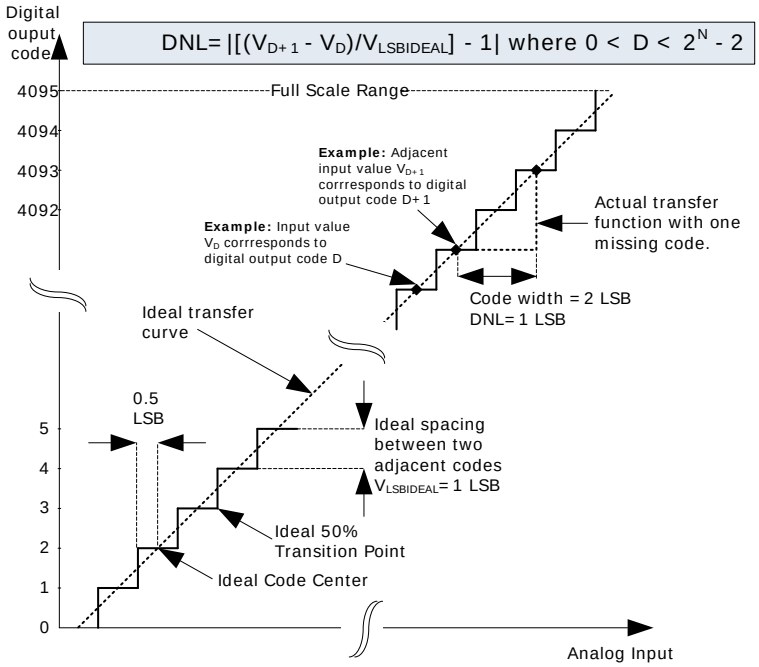
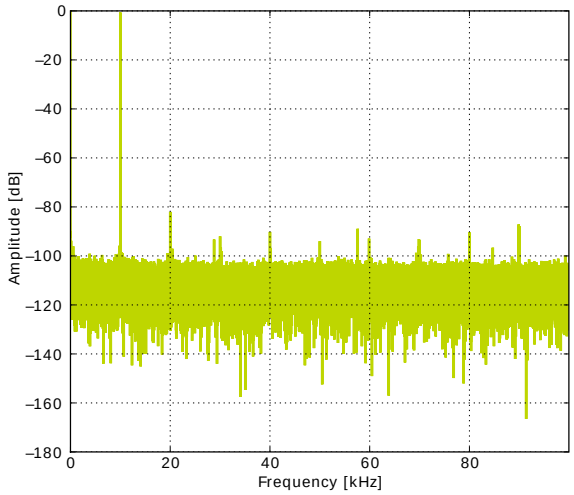


Figure 3.29. Differential Non-Linearity (DNL)

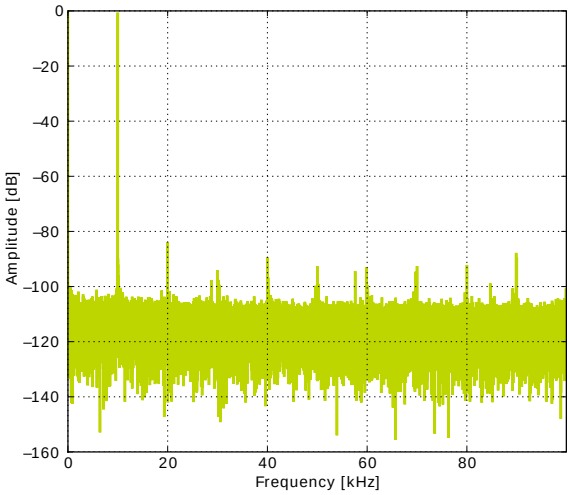


3.10.1 Typical performance

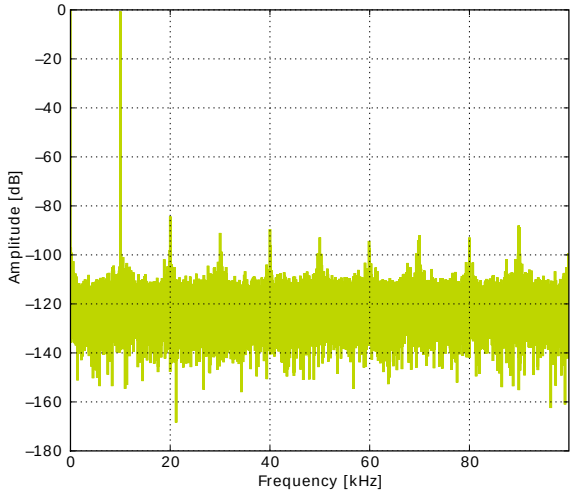
Figure 3.30. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°



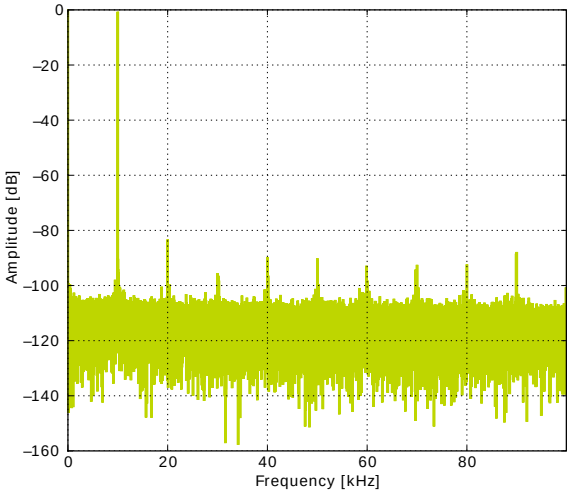
1.25V Reference



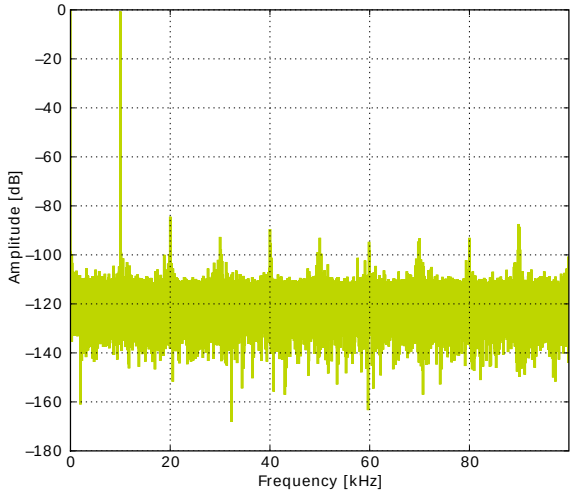
2.5V Reference



2XVDDVSS Reference

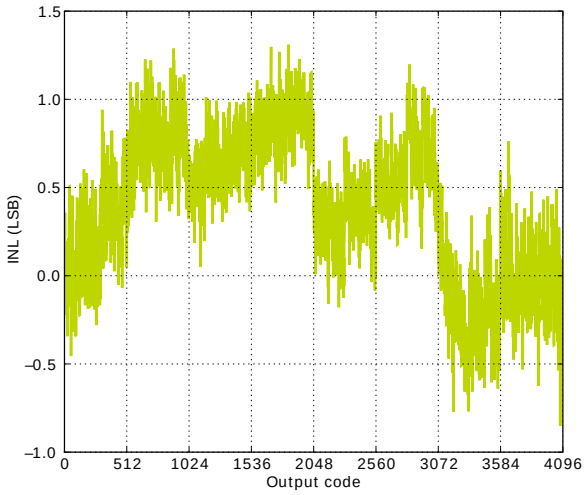


5VDIFF Reference

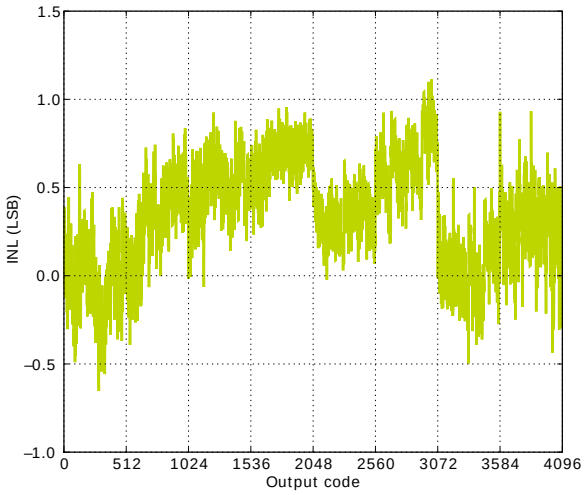


VDD Reference

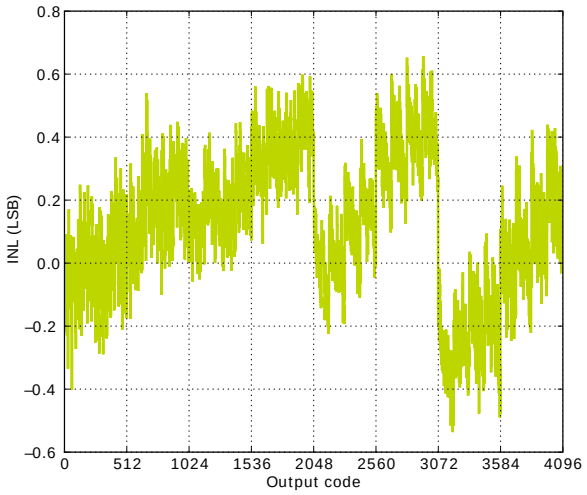
Figure 3.31. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°



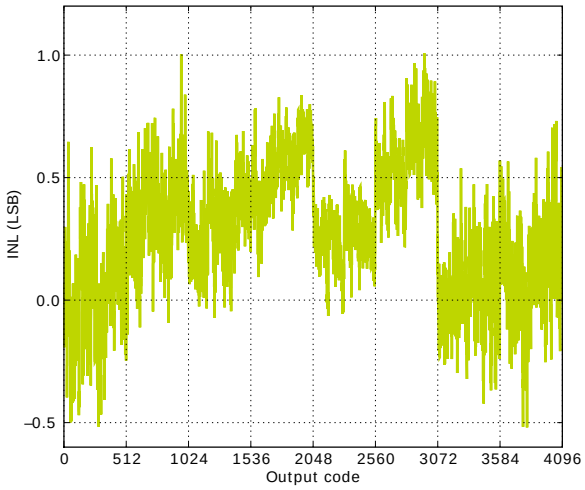
1.25V Reference



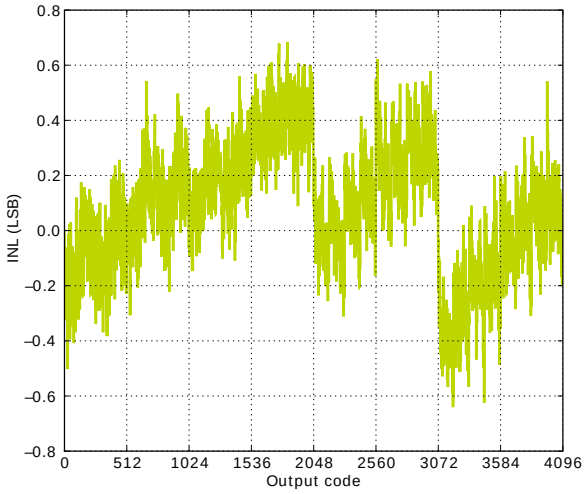
2.5V Reference



2XVDDVSS Reference

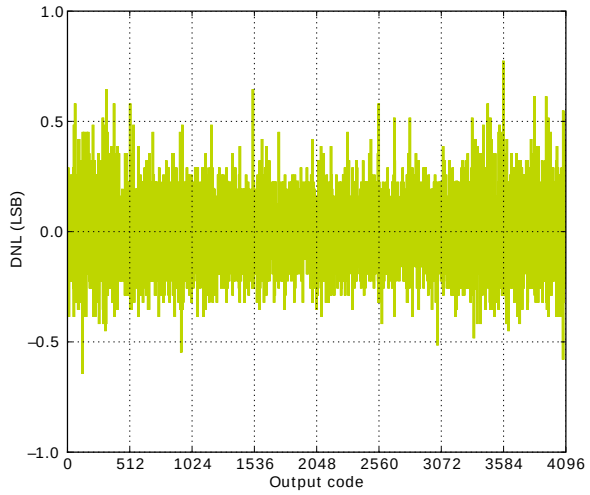


5VDIFF Reference

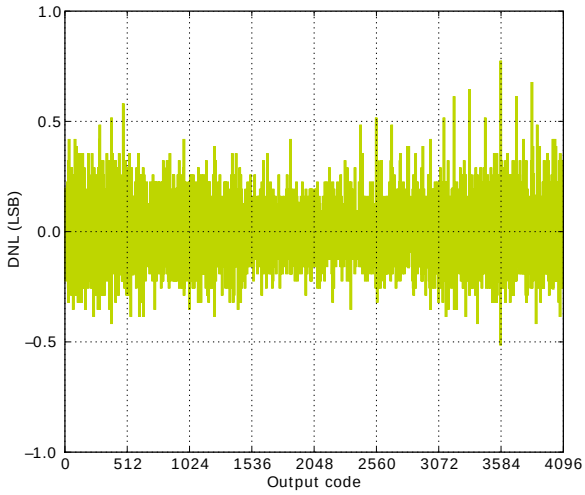


VDD Reference

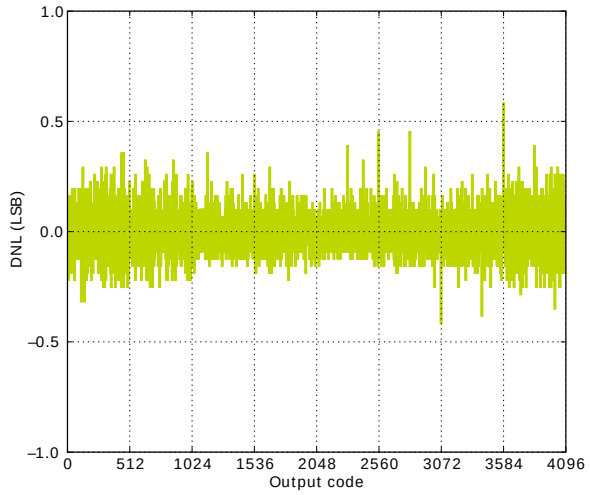
Figure 3.32. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°



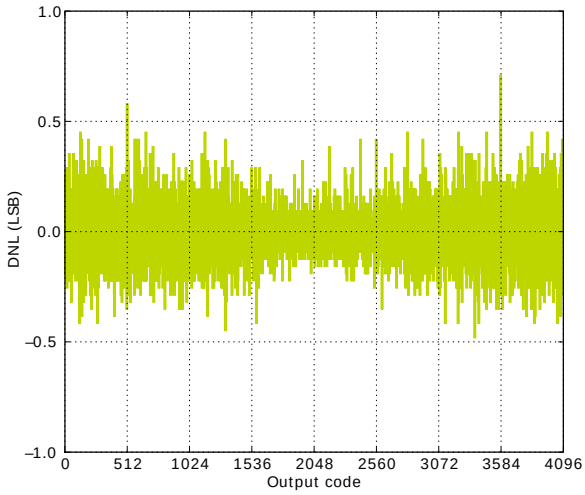
1.25V Reference



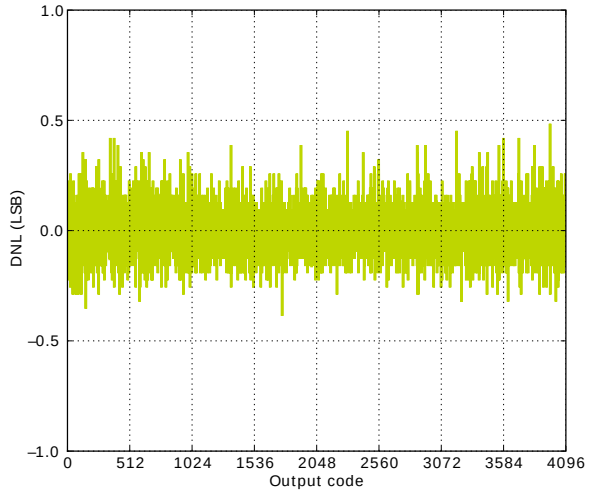
2.5V Reference



2XVDDVSS Reference

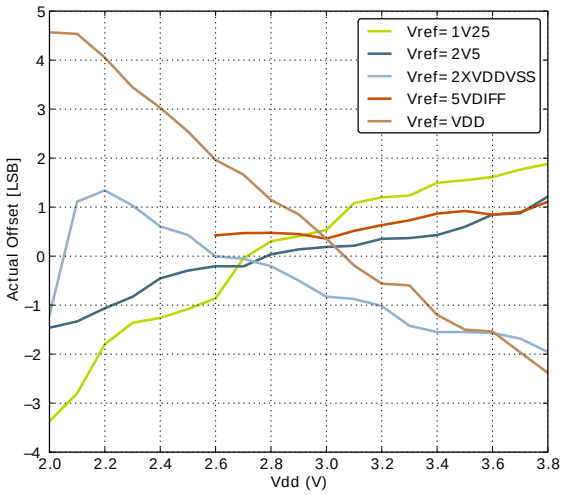


5VDIFF Reference

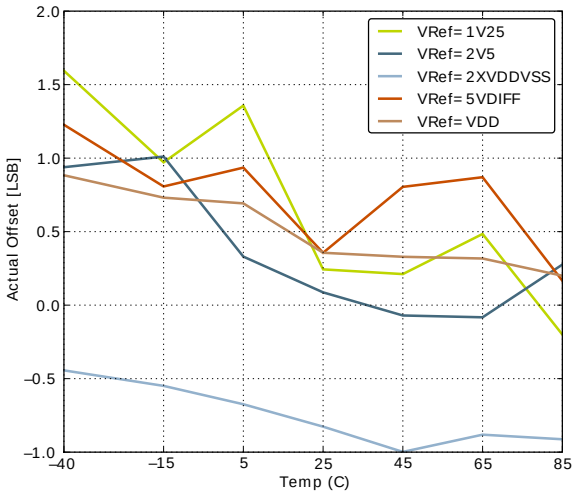


VDD Reference

Figure 3.33. ADC Absolute Offset, Common Mode = Vdd /2

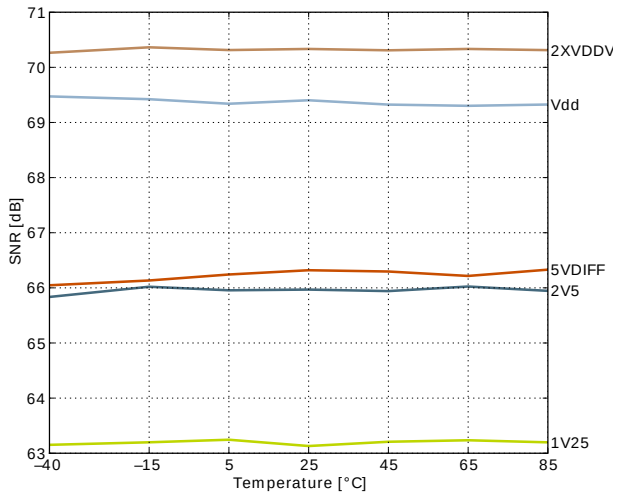


Offset vs Supply Voltage, Temp = 25°

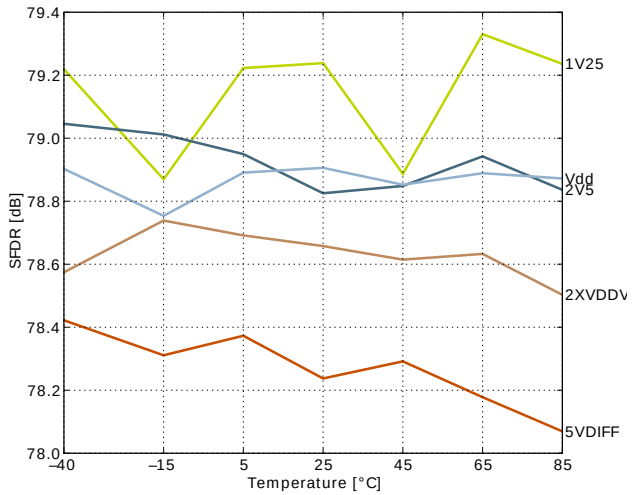


Offset vs Temperature, Vdd = 3V

Figure 3.34. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V

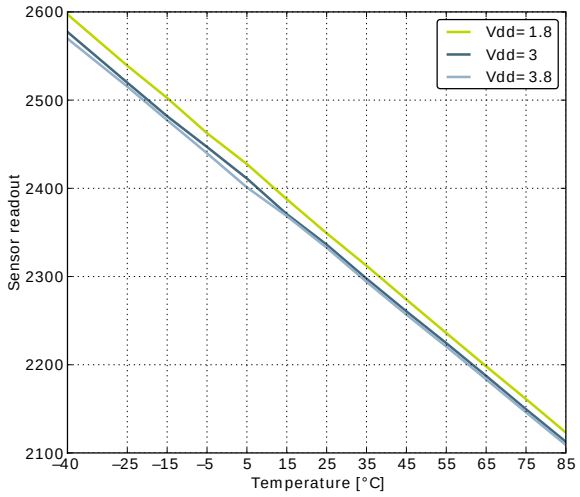


Signal to Noise Ratio (SNR)



Spurious-Free Dynamic Range (SFDR)

Figure 3.35. ADC Temperature sensor readout



3.11 Digital Analog Converter (DAC)

Table 3.16. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	VDD voltage reference, single ended	0		V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12bit		400		µA
		100 kSamples/s, 12 bit		200		µA
		1 kSamples/s 12 bit NORMAL		38		µA
SR_{DAC}	Sample rate				500	ksamples/s
f_{DAC}	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cyckles per conversion			2		
$t_{DACCONV}$	Conversion time		2			µs
$t_{DACSETTLE}$	Settling time			5		µs
SNR_{DAC}	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		58		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		58		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		59		dB
$SNDR_{DAC}$	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		56		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		53		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		55		dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		61		dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		55		dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference		60		dBc
$V_{DACOFFSET}$	Offset voltage	After calibration, single ended		2		mV
		After calibration, differential		2		mV
DNL_{DAC}	Differential non-linearity			±1		LSB
INL_{DAC}	Integral non-linearity			±5		LSB
MC_{DAC}	No missing codes			12		bits

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 3.17. OPAMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OPAMP}	Active Current	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain		400		µA
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain		100		µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13		µA
G_{OL}	Open Loop Gain	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
GBW_{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
PM_{OPAMP}	Phase Margin	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, C_L=75 pF		64		°
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C_L=75 pF		58		°
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C_L=75 pF		58		°
R_{INPUT}	Input Resistance			100		Mohm
R_{LOAD}	Load Resistance		200			Ohm
I_{LOAD_DC}	DC Load Current				11	mA
V_{INPUT}	Input Voltage	OPAxHCMDIS=0	V_{SS}		V_{DD}	V
		OPAxHCMDIS=1	V_{SS}		V_{DD}-1.2	V
V_{OUTPUT}	Output Voltage		V_{SS}		V_{DD}	V
V_{OFFSET}	Input Offset Voltage	Unity Gain, $V_{SS}<V_{in}<_{DD}$, OPAxHCMDIS=0		6		mV
		Unity Gain, $V_{SS}<V_{in}<_{DD}$-1.2, OPAxHCMDIS=1		1		mV
V_{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR_{OPAMP}	Slew Rate	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/µs
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/µs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/µs
N_{OPAMP}	Voltage Noise	V_{out}=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=0		101		$µV_{RMS}$
		V_{out}=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=1		141		$µV_{RMS}$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		V_{out}=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAx-HCMDIS=0		196		μV_{RMS}
		V_{out}=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAx-HCMDIS=1		229		μV_{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0		1230		μV_{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1		2130		μV_{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0		1630		μV_{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1		2590		μV_{RMS}

Figure 3.36. OPAMP Common Mode Rejection Ratio

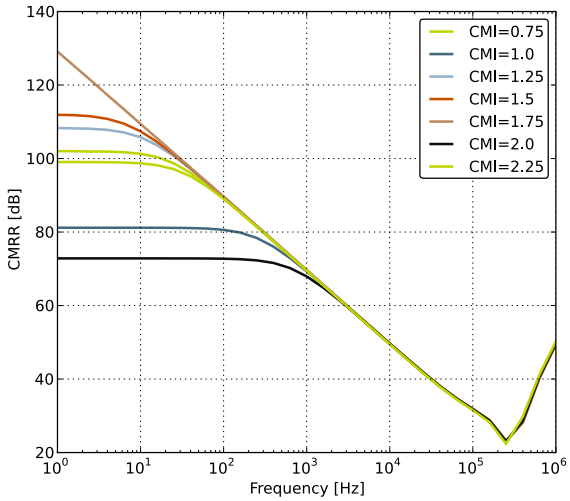


Figure 3.37. OPAMP Positive Power Supply Rejection Ratio

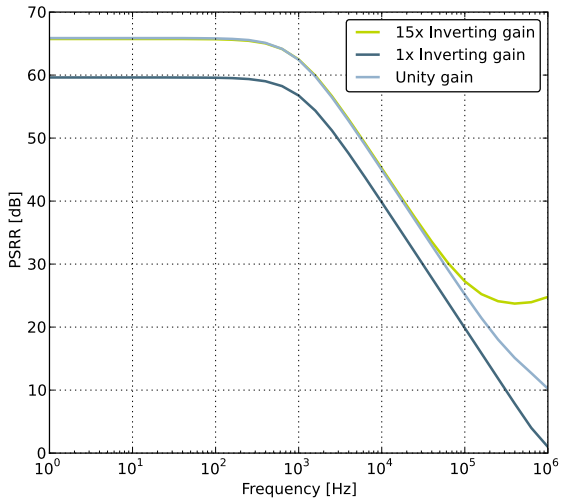


Figure 3.38. OPAMP Negative Power Supply Rejection Ratio

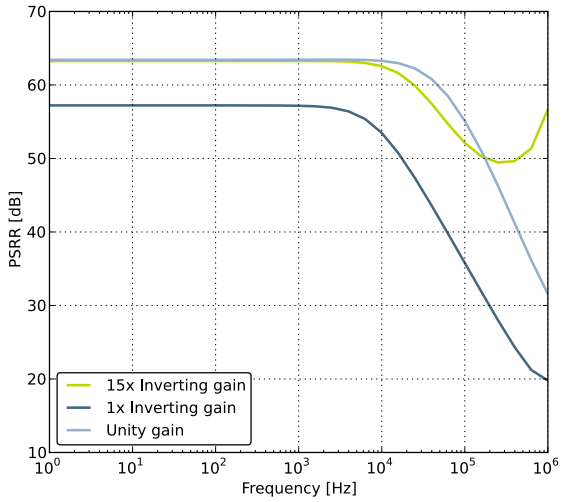


Figure 3.39. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out}=1V

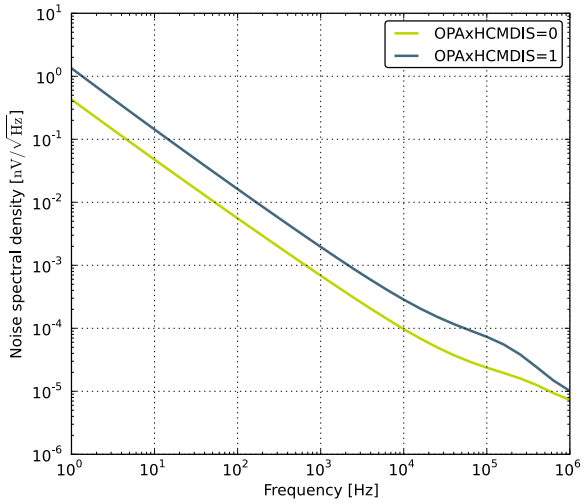
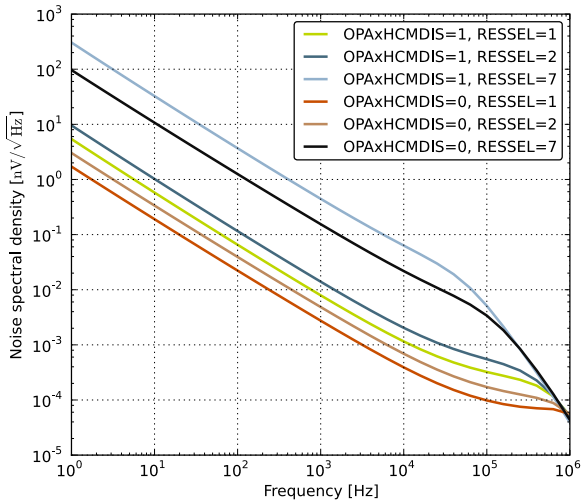


Figure 3.40. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



3.13 Analog Comparator (ACMP)

Table 3.18. ACMP

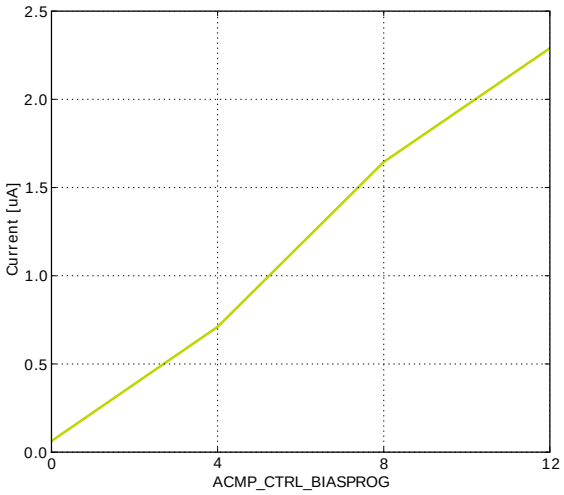
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1		µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87		µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195		µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference		5		µA
$V_{ACMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 49) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

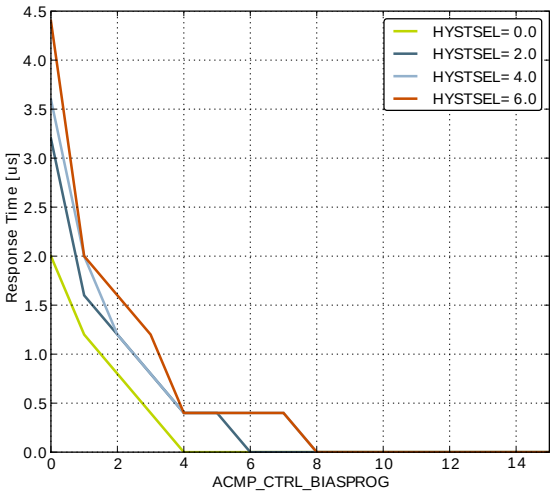
Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

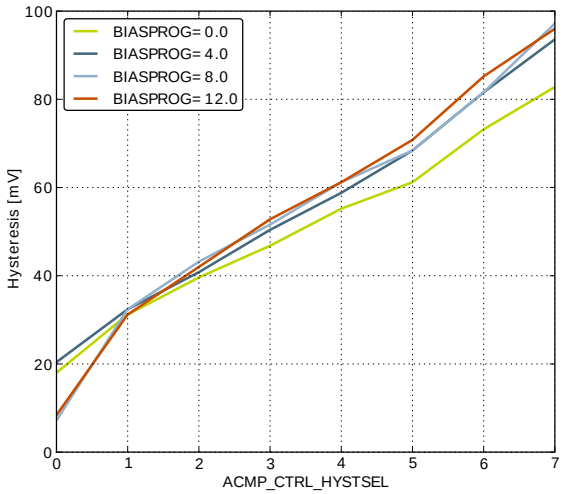
Figure 3.41. Typical ACMP Characteristics



Current consumption



Response time



Hysteresis

3.14 Voltage Comparator (VCMP)

Table 3.19. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.1		µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		14.7		µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			17		mV

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

3.15 LCD

Table 3.20. LCD

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LCDFR}	Frame rate		30		200	Hz
NUM_{SEG}	Number of segments supported			16×8		seg
V_{LCD}	LCD supply voltage range	Internal boost circuit enabled	2.0		3.8	V
I_{LCD}	Steady state current consumption.	Display disconnected, static mode, framerate 32 Hz, all segments on.		250		nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register.		550		nA
$I_{LCDBOOST}$	Steady state Current contribution of internal boost.	Internal voltage boost off		0		µA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.		8.4		µA
V_{BOOST}	Boost Voltage	VBLEV of LCD_DISPCTRL register to LEVEL0		3.0		V
		VBLEV of LCD_DISPCTRL register to LEVEL1		3.08		V
		VBLEV of LCD_DISPCTRL register to LEVEL2		3.17		V
		VBLEV of LCD_DISPCTRL register to LEVEL3		3.26		V
		VBLEV of LCD_DISPCTRL register to LEVEL4		3.34		V
		VBLEV of LCD_DISPCTRL register to LEVEL5		3.43		V
		VBLEV of LCD_DISPCTRL register to LEVEL6		3.52		V
		VBLEV of LCD_DISPCTRL register to LEVEL7		3.6		V

The total LCD current is given by Equation 3.3 (p. 52) . $I_{LCDBOOST}$ is zero if internal boost is off.

Total LCD Current Based on Operational Mode and Internal Boost

$$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST} \quad (3.3)$$

3.16 Digital Peripherals

Table 3.21. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/MHz
I_{UART}	UART current	UART idle current, clock enabled		5.63		µA/MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/MHz
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		150		nA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		100		nA
I_{LCD}	LCD current	LCD idle current, clock enabled		100		nA
I_{AES}	AES current	AES idle current, clock enabled		2.5		µA/MHz
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		µA/MHz
I_{PRS}	PRS current	PRS idle current		2,81		µA/MHz
I_{DMA}	DMA current	Clock enable		8.12		µA/MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32WG942.

4.1 Pinout

The *EFM32WG942* pinout is shown in Figure 4.1 (p. 54) and Table 4.1 (p. 54). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32WG942 Pinout (top view, not to scale)

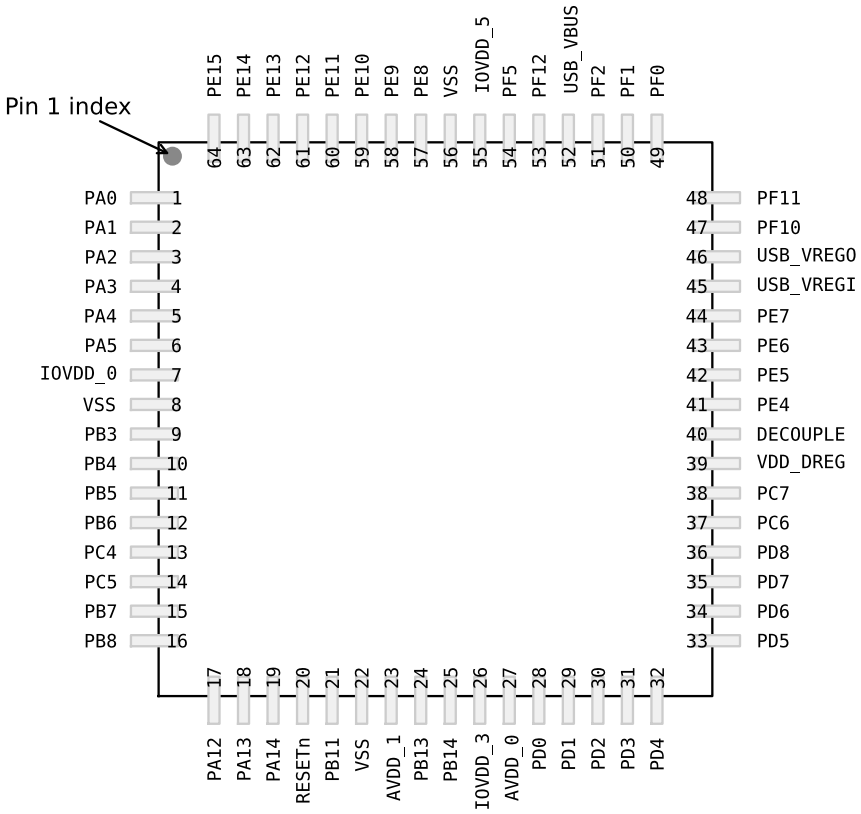


Table 4.1. Device Pinout

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0	LCD_SEG13	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1	LCD_SEG14	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
3	PA2	LCD_SEG15	TIM0_CC2 #0/1		CMU_CLK0 #0

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
					ETM_TD0 #3
4	PA3	LCD_SEG16	TIM0_CDTI0 #0		LES_ALTEX2 #0 ETM_TD1 #3
5	PA4	LCD_SEG17	TIM0_CDTI1 #0		LES_ALTEX3 #0 ETM_TD2 #3
6	PA5	LCD_SEG18	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	IOVDD_0	Digital IO power supply 0.			
8	VSS	Ground			
9	PB3	LCD_SEG20/ LCD_COM4	PCNT1_S0IN #1	US2_TX #1	
10	PB4	LCD_SEG21/ LCD_COM5	PCNT1_S1IN #1	US2_RX #1	
11	PB5	LCD_SEG22/ LCD_COM6		US2_CLK #1	
12	PB6	LCD_SEG23/ LCD_COM7		US2_CS #1	
13	PC4	DAC0_P0 / OPAMP_P0 ACMP0_CH4	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
14	PC5	DAC0_N0 / OPAMP_N0 ACMP0_CH5	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
15	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
16	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
17	PA12	LCD_BCAP_P	TIM2_CC0 #1		
18	PA13	LCD_BCAP_N	TIM2_CC1 #1		
19	PA14	LCD_BEXT	TIM2_CC2 #1		
20	RESETn	Reset input. Active low, with internal pull-up.			
21	PB11	DAC0_OUT0 / OPAMP_OUT0	TIM1_CC2 #3 LETIM0_OUT0 #1	I2C1_SDA #1	
22	VSS	Ground			
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
25	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT DAC0_OUT2 #1/ OPAMP_OUT2	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1 USB_DMPU #0	DBG_SWO #3

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
31	PD3	ADC0_CH3 DAC0_N2 / OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
32	PD4	ADC0_CH4 DAC0_P2 / OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
33	PD5	ADC0_CH5 DAC0_OUT2 #0/ OPAMP_OUT2		LEU0_RX #0	ETM_TD3 #0/2
34	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1	TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
35	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1	TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
36	PD8	BU_VIN			CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	USB_VREGI	USB Input to internal 3.3 V regulator.			
46	USB_VREGO	USB Decoupling for internal 3.3 V USB regulator and regulator output.			
47	PF10			USB_DM	
48	PF11			USB_DP	
49	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
50	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
51	PF2	LCD_SEG0	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
52	USB_VBUS	USB 5.0 V VBUS input.			
53	PF12			USB_ID	
54	PF5	LCD_SEG3	TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground			
57	PE8	LCD_SEG4	PCNT2_S0IN #1		PRS_CH3 #1
58	PE9	LCD_SEG5	PCNT2_S1IN #1		
59	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
60	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
					BOOT_RX
61	PE12	LCD_SEG8	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
62	PE13	LCD_SEG9		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
63	PE14	LCD_SEG10	TIM3_CC0 #0	LEU0_TX #2	
64	PE15	LCD_SEG11	TIM3_CC1 #0	LEU0_RX #2	

4.2 Alternate functionality pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 57). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX
BOOT_TX	PE10							Bootloader TX
BU_VIN	PD8							Battery input for Backup Power Domain
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
DAC0_N0 /	PC5							Operational Amplifier 0 external negative input.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
OPAMP_N0								
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
DAC0_N2 / OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT					PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1ALT / OPAMP_OUT1ALT					PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
DAC0_OUT2 / OPAMP_OUT2	PD5	PD0						Digital to Analog Converter DAC0_OUT2 / OPAMP output channel number 2.
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
DAC0_P2 / OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
ETM_TCLK	PD7		PC6					Embedded Trace Module ETM clock .
ETM_TD0	PD6		PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7			PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6			PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5							I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LES_ALTEX0	PD6							LESENSE alternate exite output 0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7							LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN				PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN				PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0							Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1							Peripheral Reflex System PRS, channel 1.
PRS_CH2		PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3		PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2		PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3		PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3							Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4							Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5		PF5		PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1		PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12						Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13						Timer 2 Capture Compare input / output channel 1.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM2_CC2		PA14						Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14							Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15							Timer 3 Capture Compare input / output channel 1.
US0_CLK	PE12	PE5			PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4			PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6		PE12	PB8			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7		PE13	PB7			USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX		PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX		PD0	PD7					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX		PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX		PB3						USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USV_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

4.3 GPIO pinout overview

The specific GPIO pins available in *EFM32WG942* is shown in Table 4.3 (p. 62). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

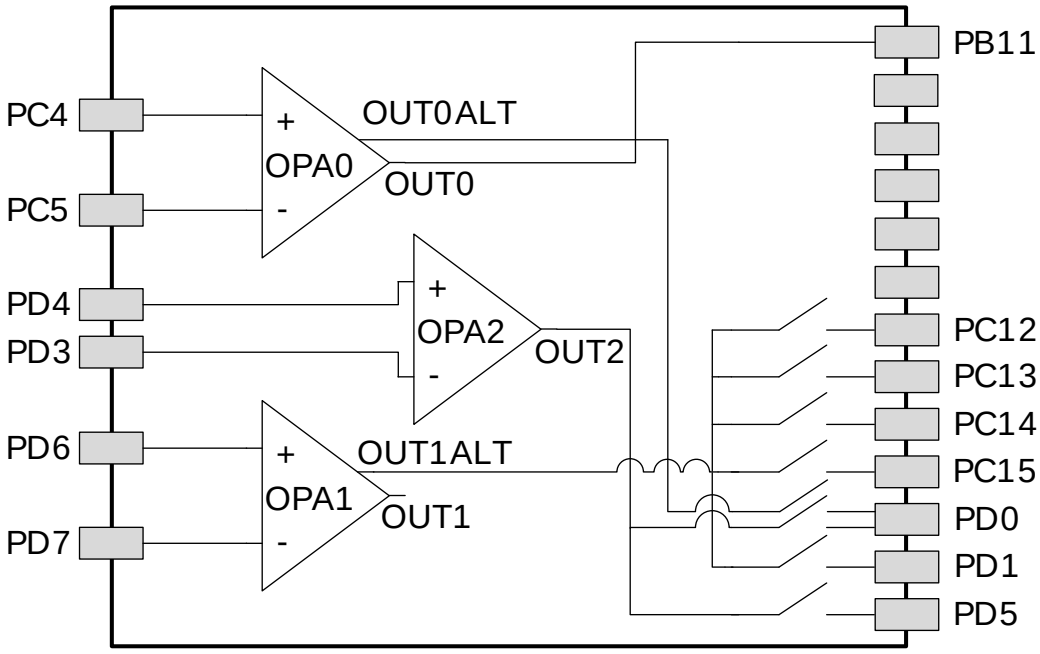
Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	PA14	PA13	PA12	-	-	-	-	-	-	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	PB6	PB5	PB4	PB3	-	-	-
Port C	-	-	-	-	-	-	-	-	PC7	PC6	PC5	PC4	-	-	-	-
Port D	-	-	-	-	-	-	-	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	-	-	-	-
Port F	-	-	-	PF12	PF11	PF10	-	-	-	-	PF5	-	-	PF2	PF1	PF0

4.4 Opamp pinout overview

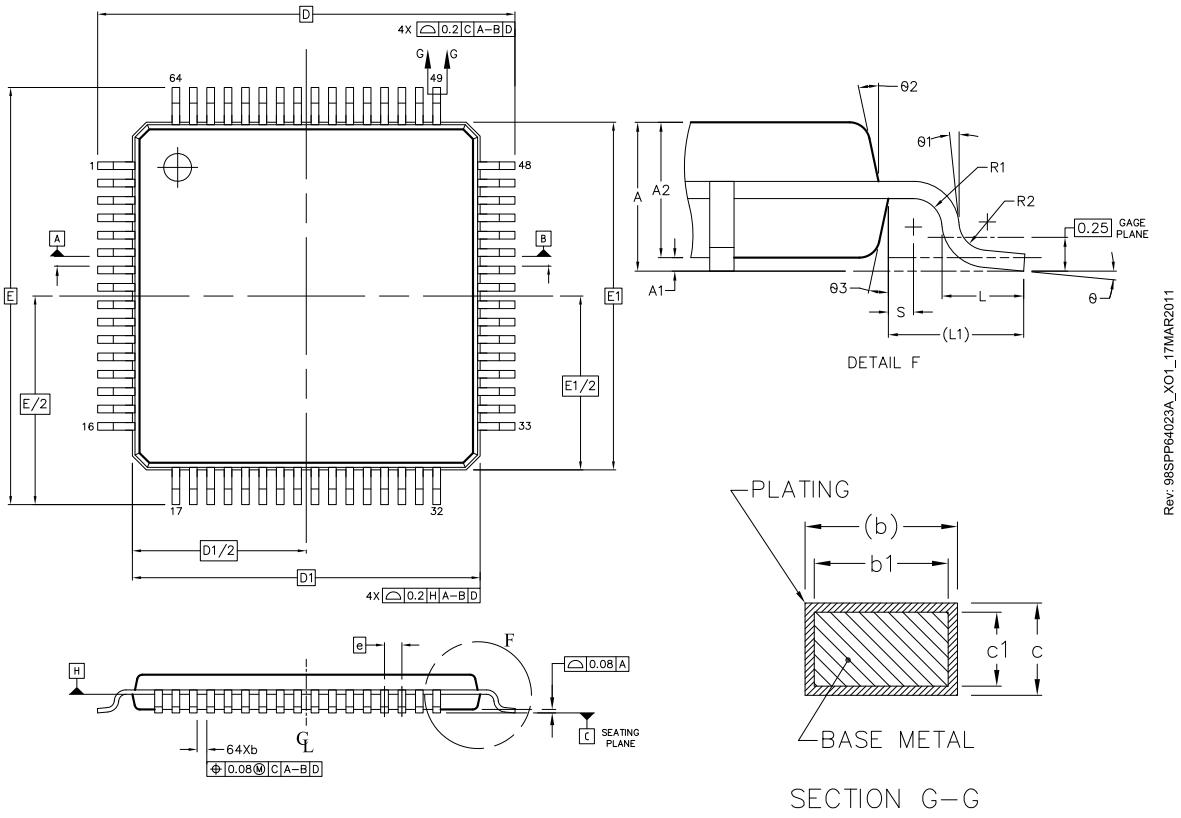
The specific opamp terminals available in *EFM32WG942* is shown in Figure 4.2 (p. 62) .

Figure 4.2. Opamp Pinout



4.5 TQFP64 Package

Figure 4.3. LQFP64



Note:

1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package body size.
3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.
4. To be determined at seating place 'C'.
5. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side. 'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
6. Detail of Pin 1 indicatifier are option all but must be located within the zone indicated.
7. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm
8. Exact shape of each corner is optional.
9. These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. All dimensions are in millimeters.

Table 4.4. QFP64 (Dimensions in mm)

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	-	1.10	1.20	L1		-	
A1	0.05	-	0.15	R1	0.08	-	-
A2	0.95	1.00	1.05	R2	0.08	-	0.20

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
b	0.17	0.22	0.27	S	0.20	-	-
b1	0.17	0.20	0.23	θ	0°	3.5°	7°
c	0.09	-	0.20	θ1	0°	-	-
C1	0.09	-	0.16	θ2	11°	12°	13°
D		12.0 BSC		θ3	11°	12°	13°
D1		10.0 BSC					
e		0.50 BSC					
E		12.0 BSC					
E1		10.0 BSC					
L	0.45	0.60	0.75				

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. TQFP64 PCB Land Pattern

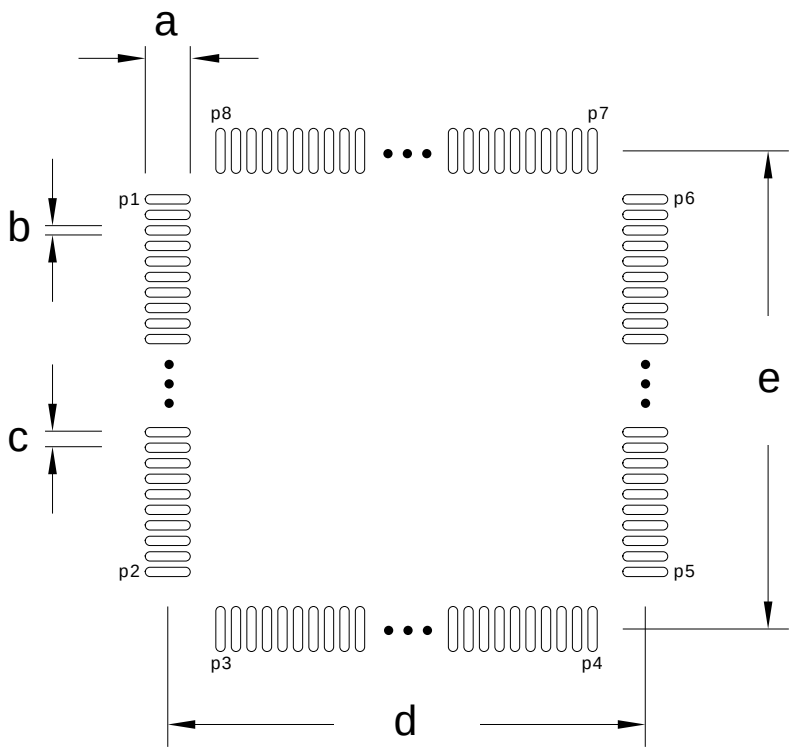


Table 5.1. QFP64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	1.60	P1	1	P6	48
b	0.30	P2	16	P7	49
c	0.50	P3	17	P8	64
d	11.50	P4	32	-	-
e	11.50	P5	33	-	-

Figure 5.2. TQFP64 PCB Solder Mask

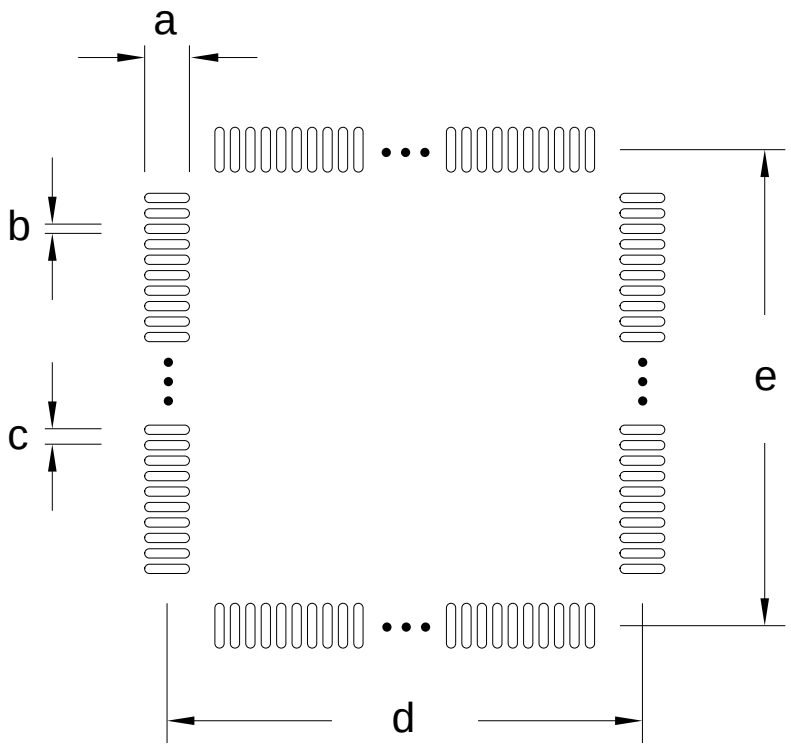


Table 5.2. QFP64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	11.50
e	11.50

Figure 5.3. TQFP64 PCB Stencil Design

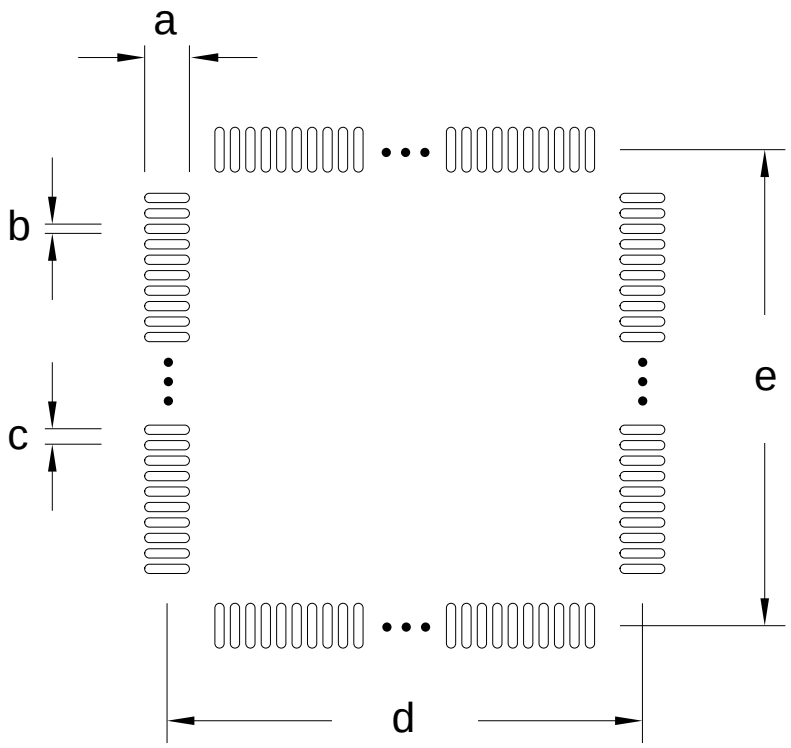


Table 5.3. QFP64 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.50
b	0.20
c	0.50
d	11.50
e	11.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 63) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

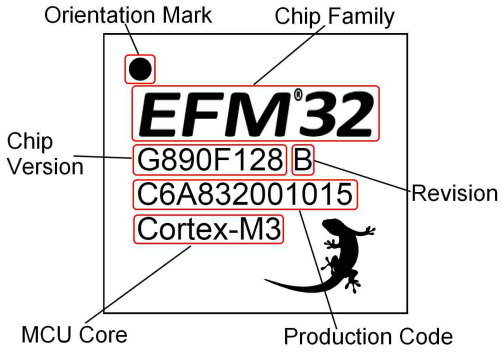
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 68). If the revision says "ES" (Engineering Sample), the revision must be read out electronically as specified in the reference manual.

6.3 Errata

Please see the dxxxx_efm32wg942_errata.pdf for description and resolution of device erratas. This document is available in Simplicity Studio and online at http://www.energymicro.com/downloads/datasheets.

7 Revision History

7.1 Revision 1.10

May 6th, 2013

Updated current consumption table and figures in Electrical characteristics section.

Other minor corrections.

7.2 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.3 Revision 0.95

May 3rd, 2012

Updated EM2/EM3 current consumption at 85°C.

7.4 Revision 0.90

February 27th, 2012

Initial preliminary release.

A Disclaimer and Trademarks

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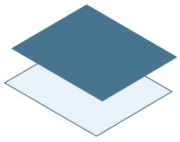

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