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FDD8424H

Dual N & P-Channel PowerTrench[®] MOSFET N-Channel: 40V, 20A, 24m Ω P-Channel: -40V, -20A, 54m Ω

Features

Q1: N-Channel

- Max $r_{DS(on)} = 24m\Omega$ at $V_{GS} = 10V$, $I_D = 9.0A$
- Max $r_{DS(on)} = 30m\Omega$ at $V_{GS} = 4.5V$, $I_D = 7.0A$

Q2: P-Channel

- Max $r_{DS(on)}$ = 54m Ω at V_{GS} = -10V, I_D = -6.5A
- Max $r_{DS(on)} = 70m\Omega$ at $V_{GS} = -4.5V$, $I_D = -5.6A$
- Fast switching speed
- RoHS Compliant



General Description

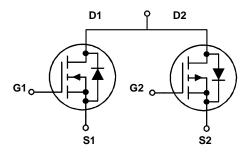
These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench- process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Application

- Inverter
- H-Bridge







N-Channel F

P-Channel

MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			Q1	Q2	Units	
V _{DS}	Drain to Source Voltage			40	-40	V	
V_{GS}	Gate to Source Voltage			±20	±20	V	
	Drain Current - Continuous (Package Limited)			20	-20		
	- Continuous (Silicon Limited) T _C = 25°C			26	-20	Α	
ID	- Continuous	T _A = 25°C		9.0	-6.5		
	- Pulsed			55	-40	7	
	Power Dissipation for Single Operation	$T_C = 25^{\circ}C$	(Note 1)	30	35		
P_{D}		$T_A = 25^{\circ}C$ (N	Note 1a)	3	.1	W	
	$T_A = 25$ °C (N		Note 1b)	1	.3		
E _{AS}	Single Pulse Avalanche Energy	((Note 3)	29	33	mJ	
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to	+150	°C	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q1	(Note 1)	4.1	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q2	(Note 1)	3.5	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8424H	FDD8424H	TO-252-4L	13"	16mm	2500 units

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Off Chara	acteristics						
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A, V_{GS} = 0V$ $I_D = -250\mu A, V_{GS} = 0V$	Q1 Q2	40 -40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = -250μA, referenced to 25°C	Q1 Q2		34 -32		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32V, V_{GS} = 0V$ $V_{DS} = -32V, V_{GS} = 0V$	Q1 Q2			1 -1	μА
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	Q1 Q2			±100 ±100	nA nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$ $V_{GS} = V_{DS}, I_D = -250\mu A$	Q1 Q2	1 -1	1.7 -1.6	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25°C I_D = -250 μ A, referenced to 25°C	Q1 Q2		-5.3 4.8		mV/°C
_	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 9.0A$ $V_{GS} = 4.5V, I_D = 7.0A$ $V_{GS} = 10V, I_D = 9.0A, T_J = 125^{\circ}C$	Q1		19 23 29	24 30 37	mΩ
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = -10V$, $I_D = -6.5A$ $V_{GS} = -4.5V$, $I_D = -5.6A$ $V_{GS} = -10V$, $I_D = -6.5A$, $T_J = 125$ °C	Q2		42 58 62	54 70 80	11152
g _{FS}	Forward Transconductance	$V_{DS} = 5V, I_{D} = 9.0A$ $V_{DS} = -5V, I_{D} = -6.5A$	Q1 Q2		29 13		S

Dynamic Characteristics

C _{iss}	Input Capacitance	Q1 V _{DS} = 20V, V _{GS} = 0V, f = 1MHZ	Q1 Q2		750 1000	1000 1330	pF
C _{oss}	Output Capacitance	Q2	Q1 Q2		115 140	155 185	pF
C _{rss}	Reverse Transfer Capacitance	$V_{DS} = -20V, V_{GS} = 0V, f = 1MHZ$	Q1 Q2		75 75	115 115	pF
R _g	Gate Resistance	f = 1MHz	Q1 Q2	0.1 0.1	1.1 3.3	3.3 9.9	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	Q1	Q1 Q2	7 7	14 14	ns
t _r	Rise Time	$V_{DD} = 20V, I_{D} = 9.0A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$	Q1 Q2	13 3	24 10	ns
t _{d(off)}	Turn-Off Delay Time	Q2 V _{DD} = -20V, I _D = -6.5A,	Q1 Q2	17 20	31 36	ns
t _f	Fall Time	$V_{GS} = -10V, R_{GEN} = 6\Omega$	Q1 Q2	6 3	12 10	ns
Q _{g(TOT)}	Total Gate Charge	Q1	Q1 Q2	14 17	20 24	nC
Q_{gs}	Gate to Source Charge	$V_{GS} = 10V, V_{DD} = 20V, I_D = 9.0A$ $Q2$	Q1 Q2	2.3 3.0		nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{GS} = -10V, V_{DD} = -20V, I_{D} = -6.5A$	Q1 Q2	3.2 3.6		nC

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Parameter

Drain-S	Source Diode Characteristics						
Is	Maximum Continuous Drain to Source Diode Forward Current			Q1 Q2		20 -20	Α
I _{SM}	Maximum Pulsed Drain to Source Di	iode Forward Current	(Note 2)	Q1 Q2		55 -40	Α
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 9.0A$ $V_{GS} = 0V, I_S = -6.5A$	(Note 2) (Note 2)	Q1 Q2	0.87 0.88	1.2 -1.2	V
t _{rr}	Reverse Recovery Time	Q1 I _F = 9.0A, di/dt = 100A/s	6	Q1 Q2	25 29	38 44	ns
Q _{rr}	Reverse Recovery Charge	Q2 $I_F = -6.5A$, di/dt = 100A/	s	Q1 Q2	19 29	29 44	nC

Test Conditions

Min

Тур

Type

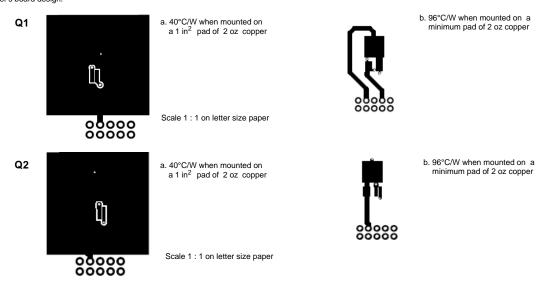
Max

Units

Notes:

Symbol

1. $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- 2. Pulse Test: Pulse Width < 300μ s, Duty cycle < 2.0%. 3. Starting $T_J = 25^{\circ}$ C, N-ch: L = 0.3mH, $I_{AS} = 14A$, $V_{DD} = 40$ V, $V_{GS} = 10$ V; P-ch: L = 0.3mH, $I_{AS} = -15A$, $V_{DD} = -40$ V, $V_{GS} = -10$ V.

Typical Characteristics (Q1 N-Channel)T_J = 25°C unless otherwise noted

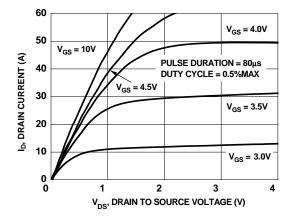


Figure 1. On-Region Characteristics

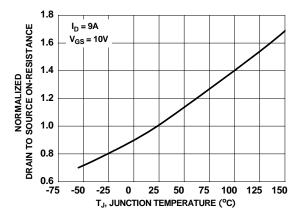


Figure 3. Normalized On-Resistance vs Junction Temperature

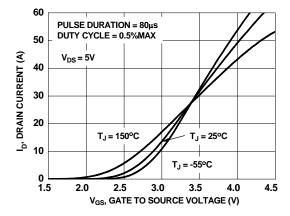


Figure 5. Transfer Characteristics

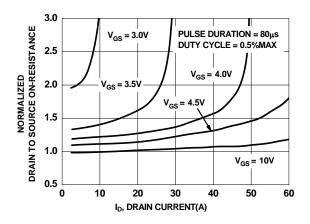


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

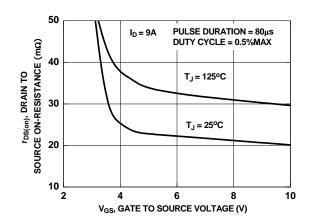


Figure 4. On-Resistance vs Gate to Source Voltage

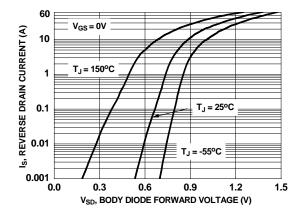


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel)T_J = 25°C unless otherwise noted

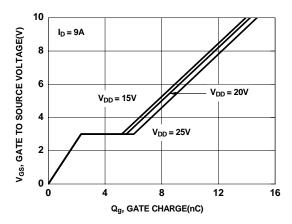


Figure 7. Gate Charge Characteristics

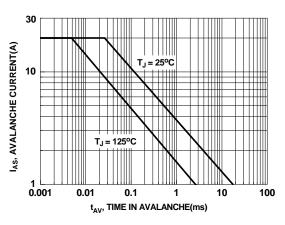


Figure 9. Unclamped Inductive Switching Capability

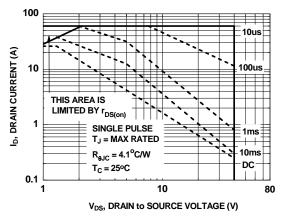


Figure 11. Forward Bias Safe Operating Area

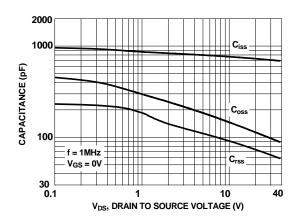


Figure 8. Capacitance vs Drain to Source Voltage

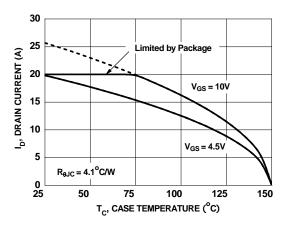


Figure 10. Maximum Continuous Drain Current vs Case Temperature

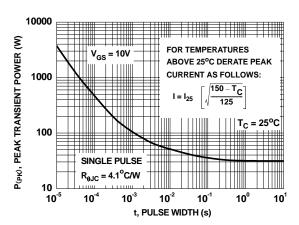


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel)T_J = 25°C unless otherwise noted

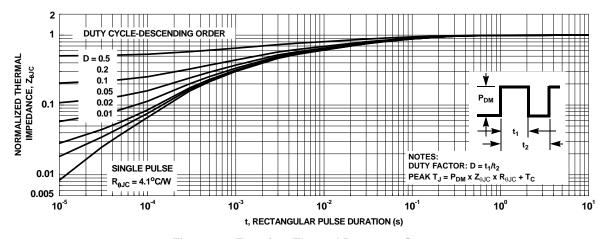


Figure 13. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel)T_J = 25°C unless otherwise noted

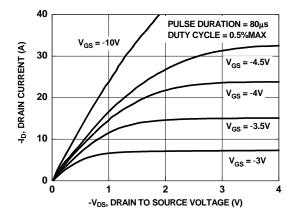


Figure 14. On- Region Characteristics

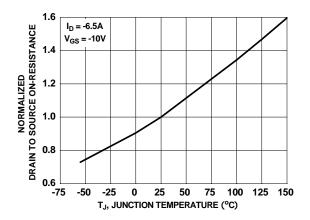


Figure 16. Normalized On-Resistance vs Junction Temperature

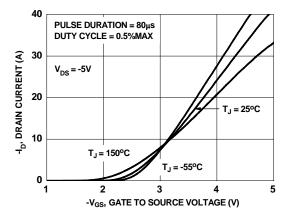


Figure 18. Transfer Characteristics

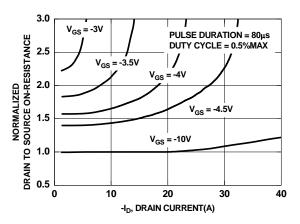


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

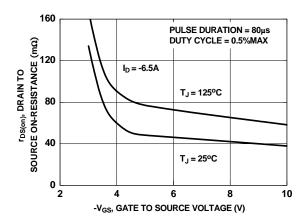


Figure 17. On-Resistance vs Gate to Source Voltage

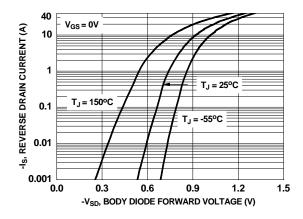


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel)T_J = 25°C unless otherwise noted

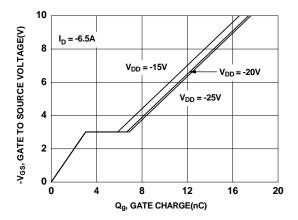


Figure 20. Gate Charge Characteristics

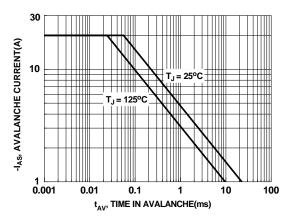


Figure 22. Unclamped Inductive Switching Capability

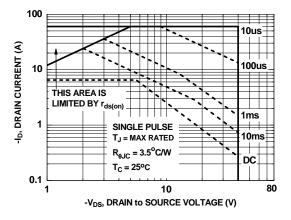


Figure 24. Forward Bias Safe Operating Area

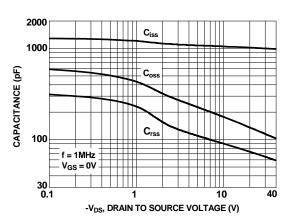


Figure 21. Capacitance vs Drain to Source Voltage

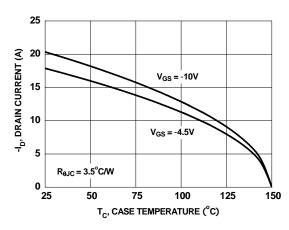


Figure 23. Maximum Continuous Drain Current vs Case Temperature

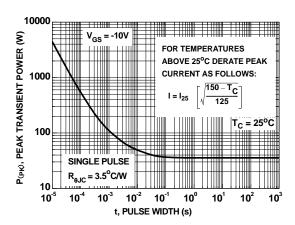


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel)T_J = 25°C unless otherwise noted

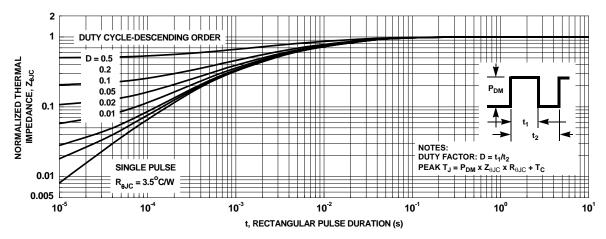
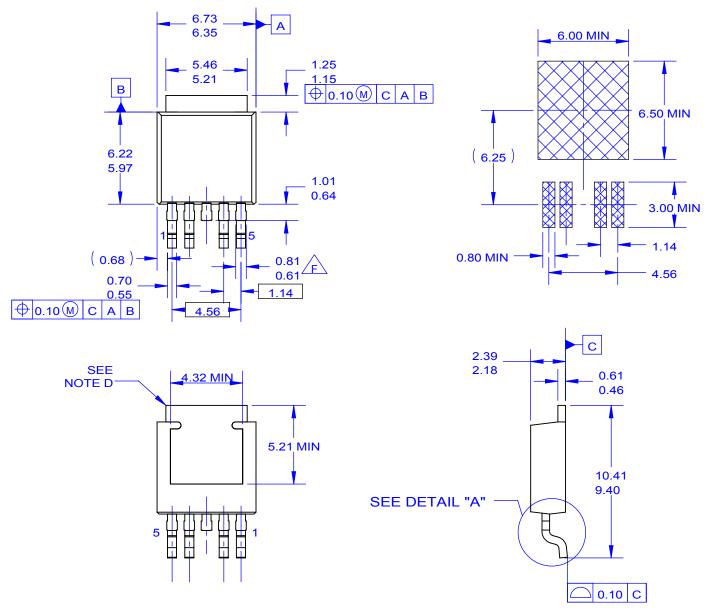
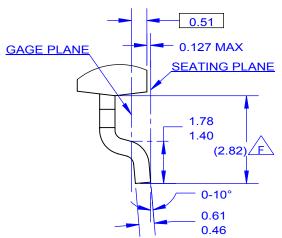


Figure 26. Transient Thermal Response Curve





DETAIL A SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFED

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многоканальный

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

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Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9