Soft-Start Controlled Load Switch

The NCP340 is a low Ron N-channel MOSFET controlled by a soft-start sequence of 2 ms for mobile applications.

The very low $R_{DS(on)}$ allows system supplying or battery charging up to DC 3A. The device is enable automatically if a Power Supply is connected on Vin pin (active High) and maintained off if no Vin (internal pull down).

Due to a current consumption optimization, leakage current is drastically decreased from the battery connected to the device, allowing long battery life.

Features

- 1.8 V 5.5 V Operating Range
- 30 mΩ N-MOSFET
- DC Current Up to 3 A
- Built-in Soft-Start 2 ms
- Reverse Voltage Protection
- Active High with Integrated Bridge
- Compliance to IEC61000-4-2 (Level 4)
 8.0 kV (Contact)
 15 kV (Air)
- ESD Ratings: Machine Model = B Human Body Model = 3
- μDFN4 1.2 x 1.6 mm
- This is a Pb-Free Device

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Computers

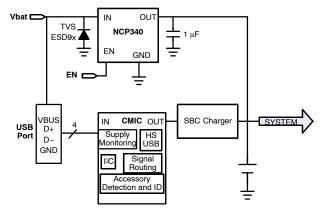


Figure 1. Typical Application Circuit



ON Semiconductor®

http://onsemi.com



UDFN4 CASE 517CE

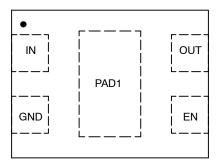
MARKING DIAGRAM



34 = Specific Device Code

M = Date Code

PINOUT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Туре	Description
IN	1	POWER	Power–switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	2	POWER	Ground connection;
EN	3	INPUT	Enable input, logic high turns on power switch.
OUT	4	OUTPUT	Power–switch output; connect a 1 μ F ceramic capacitor from OUT to GND as close as possible to the IC is recommended.
PAD1		POWER	Exposed pad can be connected to GND plane for dissipation purpose or any other thermal plane.

BLOCK DIAGRAM

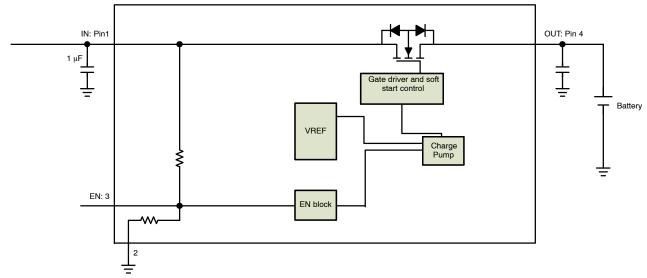


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins:	V _{EN} , V _{IN} , V _{OUT}	-0.3 to + 7.0	V
From IN to OUT Pins: Input/Output	V _{IN} , V _{OUT}	-7.0 to + 7.0	V
ESD Withstand Voltage (IEC 61000–4–2) (Note 1) (IN and OUT when bypassed with 1.0 μF capacitor minimum)	ESD IEC	15 Air, 8 contact	kV
Human Body Model (HBM) ESD Rating are (Notes 2 and 3)	ESD HBM	8000	V
Machine Model (MM) ESD Rating are (Notes 2 and 3)	ESD MM	250	V
Latch-up protection (Note 4) - Pins IN, OUT, EN	LU	100	mA
Maximum Junction Temperature Range	T _J	-40 to + 125	°C
Storage Temperature Range	T _{STG}	-40 to + 150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Guaranteed by design.
- 2. According to JEDEC standard JESD22-A108.
- 2. According to 42D2 standard 42D2—Aros.

 3. This device series contains ESD protection and passes the following tests:

 Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22–A114 for all pins.

 Machine Model (MM) ±200 V per JEDEC standard: JESD22–A115 for all pins.
- Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
 Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.

OPERATING CONDITIONS

Symbol	Parameter	C	Conditions	Min	Тур	Max	Unit
V _{IN}	Operational Power Supply			1.8		5.5	V
V _{EN}	Enable Voltage			0		5.5	
T _A	Ambient Temperature Range	•		- 40	25	+ 85	°C
TJ	Junction Temperature Range	Temperature Range		- 40	25	+ 125	°C
C _{IN}	Decoupling input capacitor		1			μF	
C _{OUT}	Decoupling output capacitor	USB port per Hub		1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	UDFN4 package (Note 6)			170		°C/W
I _{OUT}	Maximum DC current	UDFN4 package				3	Α
I peak	Maximum Peak current	100 μs pulse				15	Α
P _D	Power Dissipation Rating (Note 7)	T _A ≤ 25°C UDFN4 package			0.58		W
		T _A = 85°C	UDFN4 package		0.225		

- 6. The $R_{\theta,JA}$ is dependent of the PCB heat dissipation.
- 7. The maximum power dissipation (PD) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

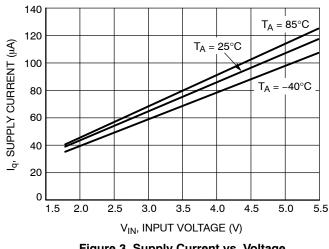
ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between $-40^{\circ}C$ to $+85^{\circ}C$ and T_J up to + 125 $^{\circ}C$ for $_{VIN}$ between 1.8 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 $^{\circ}C$ and $_{VIN}$ = 5 V.

Parameter	ameter Conditions		Min	Тур	Max	Unit	
POWER SWITCH							
Static drain-source on-state resistance	V _{IN} = 3 V, V _{IN} = 5 V	T _J = 25°C		26		m $Ω$	
		-40°C < T _J < 125°C			50	1	
Output rise time	V _{IN} = 5 V	C_{LOAD} = 1 μ F, R _{LOAD} = 125 Ω (Note 8)	0.5	2	4	ms	
Output fall time	V _{IN} = 5 V	C_{LOAD} = 100 μ F, R _{LOAD} = 40 Ω (Note 8)		4		ms	
Gate turn on	V _{IN} = 5 V	From Vin applied to V _{OUT} = 10% of fully on	0.5	2	4	ms	
	V _{IN} = 3 V	From Vin applied to V _{OUT} = 10% of fully on (Note 9)			3		
IPUT EN							
High-level input voltage			1.15			V	
Low-level input voltage					0.85	V	
En pull-down resistor				1		ΜΩ	
En pull-up resistor				1.5		МΩ	
REVERSE-LEAKAGE PROTECTION							
Reverse-current protection	V _{IN} = 0 V, V _{out} =		0.15	1	μΑ		
QUIESCENT CURRENT							
Current consumption			100	200	μΑ		
	Static drain—source on—state resistance Output rise time Output fall time Gate turn on PUT EN High—level input voltage Low—level input voltage En pull—down resistor En pull—up resistor LEAKAGE PROTECTION Reverse—current protection T CURRENT	Static drain_source on_state resistance	VITCH Static drain–source on–state resistance $V_{IN} = 3 \text{ V,} V_{IN} = 5 \text{ V} \qquad T_J = 25^{\circ}\text{C}$ $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ Output rise time $V_{IN} = 5 \text{ V} \qquad C_{LOAD} = 1 \text{ µF,} R_{LOAD} = 125 \Omega \text{ (Note 8)}$ Output fall time $V_{IN} = 5 \text{ V} \qquad C_{LOAD} = 100 \text{ µF,} R_{LOAD} = 40 \Omega \text{ (Note 8)}$ Gate turn on $V_{IN} = 5 \text{ V} \qquad From \text{ Vin applied to V}_{OUT} = 10\% \text{ of fully on (Note 9)}$ PUT EN High–level input voltage Low–level input voltage En pull–down resistor En pull–up resistor LEAKAGE PROTECTION Reverse–current protection $V_{IN} = 0 \text{ V, V}_{out} = 4.2 \text{ V (part disable), T}_{J} = 25^{\circ}\text{C}$ T CURRENT	VITCH Static drain–source on–state resistance Output rise time V _{IN} = 3 V, $V_{IN} = 5 V$ $V_{IN} = 5 V$ Output rise time V _{IN} = 5 V $V_{IN} = 5 V$ $V_{IN} = 5 V$ $V_{IN} = 5 V$ Output fall time V _{IN} = 5 V $V_{IN} = 5 V$ From Vin applied to $V_{OUT} = 100\%$ of fully on (Note 8) PUT EN High–level input voltage En pull–down resistor En pull–up resistor LEAKAGE PROTECTION Reverse–current protection $V_{IN} = 0 V, V_{Out} = 4.2 V \text{ (part disable), T}_{J} = 25^{\circ}\text{C}$ T CURRENT	VITCH Static drain–source on–state resistance $V_{IN} = 3 \text{ V,} V_{IN} = 5 \text{ V} $	VITCH Static drain–source on–state resistance $V_{IN} = 3 \text{ V}, \\ V_{IN} = 5 \text{ V}$ $T_J = 25^{\circ}\text{C}$ 26 Output rise time $V_{IN} = 5 \text{ V}$ $C_{LOAD} = 1 \mu F, \\ R_{LOAD} = 125 \Omega \text{ (Note 8)}$ 0.5 2 4 Output fall time $V_{IN} = 5 \text{ V}$ $C_{LOAD} = 100 \mu F, \\ R_{LOAD} = 40 \Omega \text{ (Note 8)}$ 4 4 Gate turn on $V_{IN} = 5 \text{ V}$ From Vin applied to $V_{OUT} = 10\%$ of fully on (Note 9) 0.5 2 4 PPUT EN High–level input voltage 1.15 1.15 0.85 En pull–down resistor 1 1.5 0.85 LEAKAGE PROTECTION Reverse–current protection $V_{IN} = 0 \text{ V}$, $V_{out} = 4.2 \text{ V}$ (part disable), $T_J = 25^{\circ}\text{C}$ 0.15 1 T CURRENT	

 ^{8.} Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground.
 9. Guaranteed by characterization.

TYPICAL CHARACTERISTICS

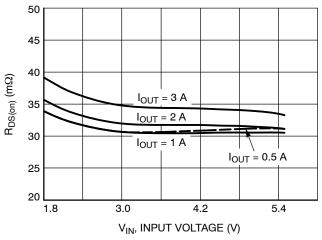
0.35



 $T_A = 85^{\circ}C$ $T_A = -40^{\circ}C$ 0 2.0 4.5 1.5 5.0 5.5 V_{OUT}, OUTPUT VOLTAGE (V)

Figure 3. Supply Current vs. Voltage

Figure 4. Reverse Current vs. Output Voltage



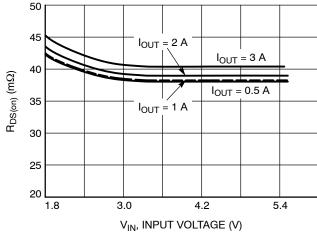
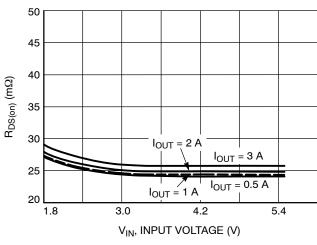


Figure 5. R_{DS(on)} vs. V_{IN} Voltage at 25°C

Figure 6. R_{DS(on)} vs. V_{IN} Voltage at 85°C



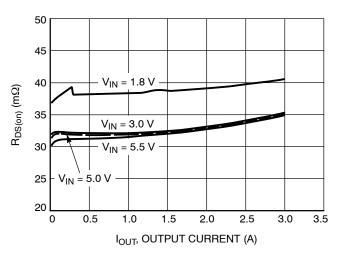


Figure 7. $R_{DS(on)}$ vs. V_{IN} Voltage at -40°C

Figure 8. R_{DS(on)} vs. I_{OUT} at 25°C

TYPICAL CHARACTERISTICS

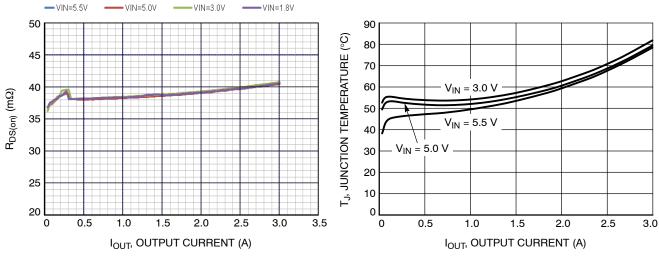


Figure 9. R_{DS(on)} vs. I_{OUT} at 85°C

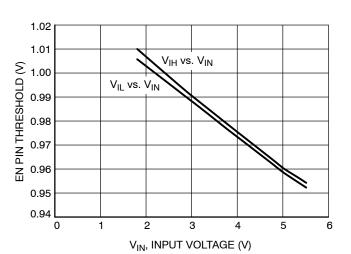


Figure 11. Logic Threshold vs. V_{IN}

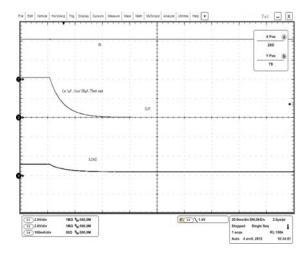


Figure 13. T_{OFF} Time on 75 mA Load



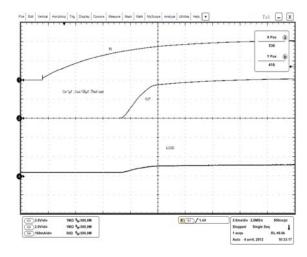


Figure 12. ToN Time on 75 mA Load

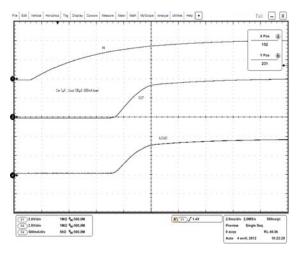
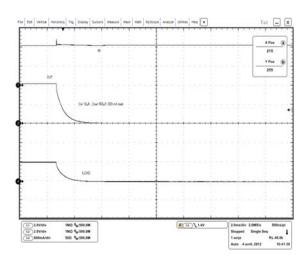


Figure 14. ToN Time on 800 mA Load

TYPICAL CHARACTERISTICS



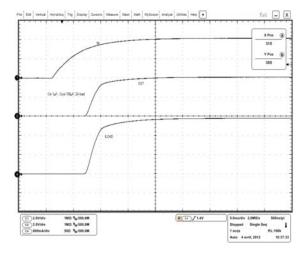


Figure 15. T_{OFF} Time on 800 mA Load

Figure 16. T_{ON} Time on 2 A Load

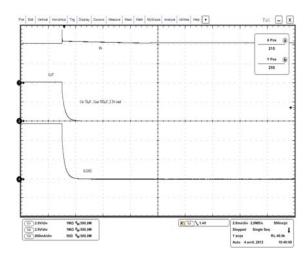


Figure 17. T_{OFF} Time on 2.3 A Load

FUNCTIONAL DESCRIPTION

Overview

The NCP340 is a high side N-channel MOSFET power distribution switch designed to connect external voltage directly to the system. The high side MOSFET is automatically turned on if the Vin voltage is applied thanks to internal pull up connected between Vin and EN pin. The turned off is obtained by Vin removal. Due to the soft start circuitry, NCP340 is able to limit large voltage surges.

Enable input

Enable pin is an active high. The part is off when Vin is not present, limiting current consumption from battery to OUT pin.

In the other side, the part is automatically turned on when V_{IN} is applied.

Blocking Control

The blocking control circuitry switches the bulk of the power NMOS. When the part is off (No $V_{\rm IN}$ or EN tied to GND externally), the body diode limits the leakage current $I_{\rm REV}$ from OUT to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUT pin. In operating condition, anode of the body diode is connected to OUT pin and cathode is connected to IN pin preventing the discharge of the power supply.

Cin Capacitor

A IN capacitor, 1 μ F, at least, capacitor must be placed as close as possible the part to be Compliant with IEC61000-4-2 (Level 4).

Cout Capacitor

Depending on the sinking current during system start up and system turn off, a capacitor must be placed on the output. A $1\,\mu F$ is strongly recommended but can be decreased down to 100 nF if the above two sequences are well controlled and parasitic inductance connected on the Vout line is negligible.

APPLICATION INFORMATION

Power Dissipation

The device's junction temperature depends on different contributor factor such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

 $\mathsf{P}_\mathsf{D} = \mathsf{R}_\mathsf{DS(on)} \times \left(\mathsf{I}_\mathsf{OUT}\right)^2$

 P_D = Power dissipation (W)

 $R_{DS(on)}$ = Power MOSFET on resistance (Ω)

I_{OUT} = Output current (A)

 $T_{J} = P_{D} \times R_{\theta,JA} + T_{A}$

 $T_{\rm J}$ = Junction temperature (°C

 $R_{\theta JA}$ = Package thermal resistance (°C/W)

 T_A = Ambient temperature (°C)

PCB Recommendations

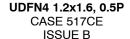
The NCP340 integrates an up to 3 A rated NMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. The μ DFN4 PAD1 must be connected to ground plane to increase the heat transfer if necessary. By increasing PCB area, the R_{0JA} of the package can be decreased, allowing higher power dissipation.

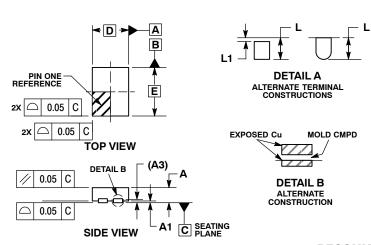
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NCP340MUTBG	34	μDFN4, 1.2x1.6 mm (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS





D2

BOTTOM VIEW

4X b

 \oplus 0.05 M C A B

NOTE 3

DFTAIL A

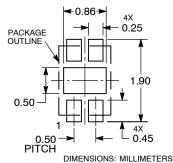
E2

NOTES:

- TES:
 DIMENSIONING AND TOLERANCING PER
 ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION IS APPLIES TO PLATED TERMINAL
 AND IS MEASURED BETWEEN 0.15 AND
 0.20 mm FROM THE TERMINAL TIPS.
 PACKAGE DIMENSIONS EXCLUSIVE OF
- BURRS AND MOLD FLASH.

	MILLIMETERS				
DIM	MIN	NOM	MAX		
Α	0.45	0.50	0.55		
A1	0.00		0.05		
А3	0.13 REF				
b	0.25	0.30	0.35		
D	1	.20 BS0)		
D2	0.76	0.86	0.96		
Е	1.60 BSC				
E2	0.40	0.50	0.60		
е	0.50 BSC				
L	0.20	0.30	0.40		
L1			0.15		

RECOMMENDED MOUNTING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and un are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice on semiconductor and are registered radiations of semiconduction Components industries, Ite (SCILLO). Solitude services are injust of make drainges without further induce to any products herein. SCILLO makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada

Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9