# Quad 16-Bit Rail-to-Rail DACs in 16-Lead SSOP

## FEATURES

- **Smallest Pin Compatible Quad 16-Bit DAC:**
  **LTC2604: 16-Bits**
  **LTC2614: 14-Bits**
  **LTC2624: 12-Bits**
- **Guaranteed 16-Bit Monotonic Over Temperature**
- Separate Reference Inputs for each DAC
- Wide 2.5V to 5.5V Supply Range
- Low Power Operation: 250µA per DAC at 3V
- Individual DAC Power-Down to 1µA, Max
- Ultralow Crosstalk Between DACs (<5µV)
- High Rail-to-Rail Output Drive (±15mA)
- Double Buffered Digital Inputs
- LTC2604-1/LTC2614-1/LTC2624-1: Power-On Reset to Midscale
- 16-Lead Narrow SSOP Package

## APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

## DESCRIPTION

The LTC®2604/LTC2614/LTC2624 are quad 16-,14- and 12-bit 2.5V to 5.5V rail-to-rail voltage output DACs in 16-lead narrow SSOP packages. These parts have separate reference inputs for each DAC. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish advanced performance standards for output drive, crosstalk and load regulation in single-supply, voltage output multiples.

The parts use a simple SPI/MICROWIRE compatible 3-wire serial interface which can be operated at clock rates up to 50MHz. Daisy-chain capability and a hardware $\overline{CLR}$ function are included.

The LTC2604/LTC2614/LTC2624 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale; and after power-up, they stay at zero scale until a valid write and update take place. The power-on reset circuit resets the LTC2604-1/LTC2614-1 /LTC2624-1 to midscale. The voltage outputs stay at midscale until a valid write and update take place.

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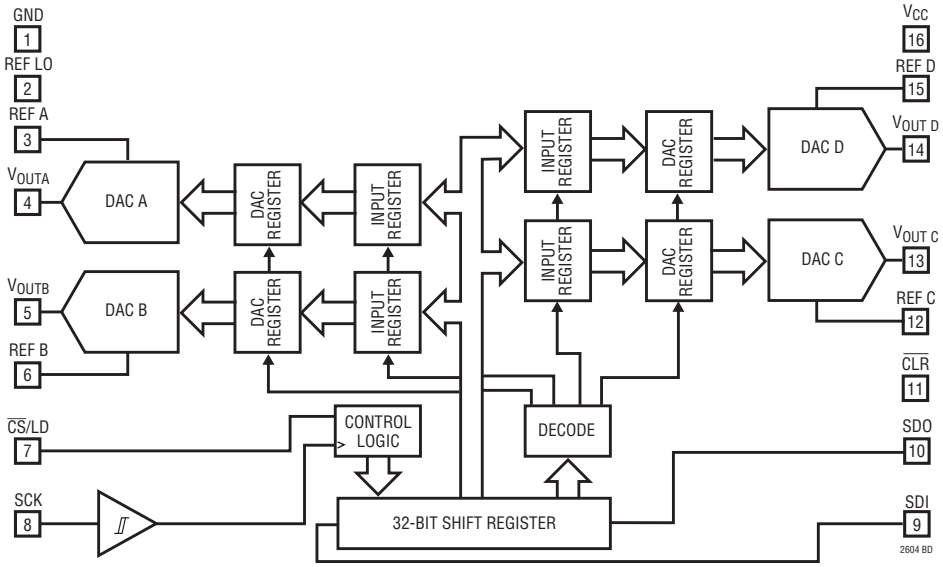
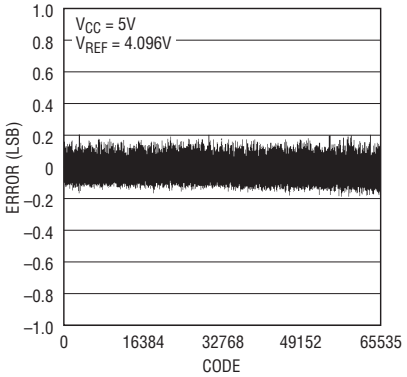
## BLOCK DIAGRAM




**Differential Nonlinearity (LTC2604)**

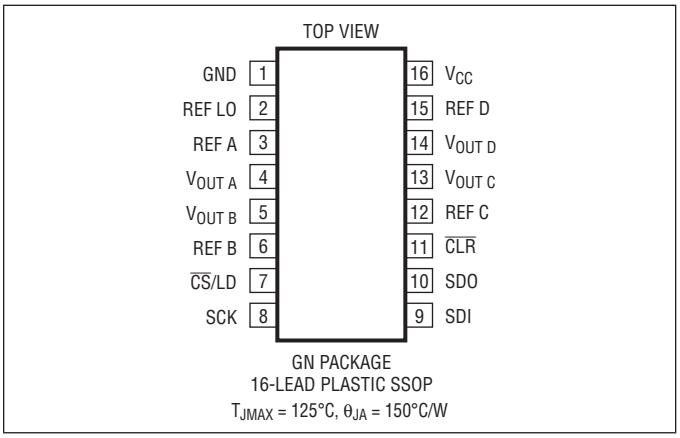


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Any Pin to GND ..... –0.3V to 6V
Any Pin to $V_{CC}$ ..... –6V to 0.3V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC2604C/LTC2614C/LTC2624C ..... 0°C to 70°C
LTC2604C-1/LTC2614C-1/
LTC2624C-1 ..... 0°C to 70°C
LTC2604I/LTC2614I/LTC2624I ..... –40°C to 85°C
LTC2604I-1/LTC2614I-1/
LTC2624I-1 ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION




GN PACKAGE
16-LEAD PLASTIC SSOP
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 150°C/W

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC2604CGN#PBF | LTC2604CGN#TRPBF | 2604 | 16-Lead Narrow SSOP Package | 0°C to 70°C |
| LTC2604CGN-1#PBF | LTC2604CGN-1#TRPBF | 26041 | 16-Lead Narrow SSOP Package | 0°C to 70°C |
| LTC2604IGN#PBF | LTC2604IGN#TRPBF | 2604I | 16-Lead Narrow SSOP Package | –40°C to 85°C |
| LTC2604IGN-1#PBF | LTC2604IGN-1#TRPBF | 2604I1 | 16-Lead Narrow SSOP Package | –40°C to 85°C |
| LTC2614CGN#PBF | LTC2614CGN#TRPBF | 2614 | 16-Lead Narrow SSOP Package | 0°C to 70°C |
| LTC2614CGN-1#PBF | LTC2614CGN-1#TRPBF | 26141 | 16-Lead Narrow SSOP Package | 0°C to 70°C |
| LTC2614IGN#PBF | LTC2614IGN#TRPBF | 2614I | 16-Lead Narrow SSOP Package | –40°C to 85°C |
| LTC2614IGN-1#PBF | LTC2614IGN-1#TRPBF | 2614I1 | 16-Lead Narrow SSOP Package | –40°C to 85°C |
| LTC2624CGN#PBF | LTC2624CGN#TRPBF | 2624 | 16-Lead Narrow SSOP Package | 0°C to 70°C |
| LTC2624CGN-1#PBF | LTC2624CGN-1#TRPBF | 26241 | 16-Lead Narrow SSOP Package | 0°C to 70°C |
| LTC2624IGN#PBF | LTC2624IGN#TRPBF | 2624I | 16-Lead Narrow SSOP Package | –40°C to 85°C |
| LTC2624IGN-1#PBF | LTC2624IGN-1#TRPBF | 2624I1 | 16-Lead Narrow SSOP Package | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. REF A = REF B = REF C = REF D = 4.096V ($V_{CC}$ = 5V), REF A = REF B = REF C = REF D = 2.048V ($V_{CC}$ = 2.5V), REF LO = 0V, $V_{OUT}$ unloaded, unless otherwise noted. (Note 10)**

| SYMBOL | PARAMETER | CONDITIONS | | LTC2624/LTC2624-1 | | | LTC2614/LTC2614-1 | | | LTC2604/LTC2604-1 | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DC Performance** | | | | | | | | | | | | | |
| | Resolution | | ● | 12 | | | 14 | | | 16 | | | Bits |
| | Monotonicity | (Note 2) | ● | 12 | | | 14 | | | 16 | | | Bits |
| DNL | Differential Nonlinearity | (Note 2) | ● | | | ±0.5 | | | ±1 | | | ±1 | LSB |
| INL | Integral Nonlinearity | (Note 2) | ● | | ±0.9 | ±4 | | ±4 | ±16 | | ±14 | ±64 | LSB |

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| SYMBOL | PARAMETER | CONDITIONS | | LTC2624/LTC2624-1 MIN | LTC2624/LTC2624-1 TYP | LTC2624/LTC2624-1 MAX | LTC2614/LTC2614-1 MIN | LTC2614/LTC2614-1 TYP | LTC2614/LTC2614-1 MAX | LTC2604/LTC2604-1 MIN | LTC2604/LTC2604-1 TYP | LTC2604/LTC2604-1 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Load Regulation | $V_{REF}$ = $V_{CC}$ = 5V, Midscale | | | | | | | | | | | |
| | | $I_{OUT}$ = 0mA to 15mA Sourcing | ● | | 0.025 | 0.125 | | 0.1 | 0.5 | | 0.3 | 2 | LSB/mA |
| | | $I_{OUT}$ = 0mA to 15mA Sinking | ● | | 0.025 | 0.125 | | 0.1 | 0.5 | | 0.3 | 2 | LSB/mA |
| | | $V_{REF}$ = $V_{CC}$ = 2.5V, Midscale | | | | | | | | | | | |
| | | $I_{OUT}$ = 0mA to 7.5mA Sourcing | ● | | 0.05 | 0.25 | | 0.2 | 1 | | 0.7 | 4 | LSB/mA |
| | | $I_{OUT}$ = 0mA to 7.5mA Sinking | ● | | 0.05 | 0.25 | | 0.2 | 1 | | 0.7 | 4 | LSB/mA |
| ZSE | Zero-Scale Error | | ● | | 1.5 | 9 | | 1.5 | 9 | | 1.5 | 9 | mV |
| $V_{OS}$ | Offset Error | (Note 7) | ● | | ±1.5 | ±9 | | ±1.5 | ±9 | | ±1.5 | ±9 | mV |
| | $V_{OS}$ Temperature Coefficient | | | | ±5 | | | ±5 | | | ±5 | | µV/°C |
| GE | Gain Error | | ● | | ±0.1 | ±0.7 | | ±0.1 | ±0.7 | | ±0.1 | ±0.7 | %FSR |
| | Gain Temperature Coefficient | | | | ±5 | | | ±5 | | | ±5 | | ppm/°C |

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| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| PSR | Power Supply Rejection | $V_{CC}$ = 5V ±10% | | | –80 | | dB |
| | | $V_{CC}$ = 3V ±10% | | | –80 | | dB |
| $R_{OUT}$ | DC Output Impedance | $V_{REF}$ = $V_{CC}$ = 5V, Midscale; –15mA ≤ $I_{OUT}$ ≤ 15mA | ● | | 0.025 | 0.15 | Ω |
| | | $V_{REF}$ = $V_{CC}$ = 2.5V, Midscale; –7.5mA ≤ $I_{OUT}$ ≤ 7.5mA | ● | | 0.030 | 0.15 | Ω |
| | DC Crosstalk (Note 4) | Due to Full Scale Output Change (Note 5) | | | ±5 | | µV |
| | | Due to Load Current Change | | | ±1 | | µV/mA |
| | | Due to Powering Down (per Channel) | | | ±3.5 | | µV |
| $I_{SC}$ | Short-Circuit Output Current | $V_{CC}$ = 5.5V, $V_{REF}$ = 5.5V | | | | | |
| | | Code: Zero Scale; Forcing Output to $V_{CC}$ | ● | 15 | 34 | 60 | mA |
| | | Code: Full Scale; Forcing Output to GND | ● | 15 | 36 | 60 | mA |
| | | $V_{CC}$ = 2.5V, $V_{REF}$ = 2.5V | | | | | |
| | | Code: Zero Scale; Forcing Output to $V_{CC}$ | ● | 7.5 | 18 | 50 | mA |
| | | Code: Full Scale; Forcing Output to GND | ● | 7.5 | 24 | 50 | mA |
| **Reference Input** | | | | | | | |
| | Input Voltage Range | | ● | 0 | | $V_{CC}$ | µA |
| | Resistance | Normal Mode | ● | 88 | 128 | 160 | kΩ |
| | Capacitance | | | | 14 | | pF |
| $I_{REF}$ | Reference Current, Power Down Mode | All DACs Powered Down | ● | | 0.001 | 1 | µA |
| **Power Supply** | | | | | | | |
| $V_{CC}$ | Positive Supply Voltage | For Specified Performance | ● | 2.5 | | 5.5 | V |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5V (Note 3) | ● | | 1.3 | 2 | mA |
| | | $V_{CC}$ = 3V (Note 3) | ● | | 1 | 1.6 | mA |
| | | All DACs Powered Down (Note 3) $V_{CC}$ = 5V | ● | | 0.35 | 1 | µA |
| | | All DACs Powered Down (Note 3) $V_{CC}$ = 3V | ● | | 0.10 | 1 | µA |
| **Digital I/O** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | $V_{CC}$ = 2.5V to 5.5V | ● | 2.4 | | | V |
| | | $V_{CC}$ = 2.5V to 3.6V | ● | 2.0 | | | V |

## ELECTRICAL CHARACTERISTICS

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| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Digital Input Low Voltage | $V_{CC}$ = 4.5V to 5.5V<br>$V_{CC}$ = 2.5V to 5.5V | ●<br>● | | | 0.8<br>0.6 | V<br>V |
| $V_{OH}$ | Digital Output High Voltage | Load Current = –100µA | ● | $V_{CC}$ – 0.4 | | | V |
| $V_{OL}$ | Digital Output Low Voltage | Load Current = +100µA | ● | | | 0.4 | V |
| $I_{LK}$ | Digital Input Leakage | $V_{IN}$ = GND to $V_{CC}$ | ● | | | ±1 | µA |
| $C_{IN}$ | Digital Input Capacitance | (Note 6) | ● | | | 8 | pF |

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| SYMBOL | PARAMETER | CONDITIONS | | LTC2624/LTC2624-1 | | | LTC2614/LTC2614-1 | | | LTC2604/LTC2604-1 | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **AC Performance** | | | | | | | | | | | | | |
| $t_S$ | Settling Time (Note 8) | ±0.024% (±1LSB at 12 Bits)<br>±0.006% (±1LSB at 14 Bits)<br>±0.0015% (±1LSB at 16 Bits) | | | 7 | | | 7<br>9 | | | 7<br>9<br>10 | | µs<br>µs<br>µs |
| | Settling Time for 1LSB Step (Note 9) | ±0.024% (±1LSB at 12 Bits)<br>±0.006% (±1LSB at 14 Bits)<br>±0.0015% (±1LSB at 16 Bits) | | | 2.7 | | | 2.7<br>4.8 | | | 2.7<br>4.8<br>5.2 | | µs<br>µs<br>µs |
| | Voltage Output Slew Rate | | | | 0.80 | | | 0.80 | | | 0.80 | | V/µs |
| | Capacitive Load Driving | | | | 1000 | | | 1000 | | | 1000 | | pF |
| | Glitch Impulse | At Midscale Transition | | | 12 | | | 12 | | | 12 | | nV • s |
| | Multiplying Bandwidth | | | | 180 | | | 180 | | | 180 | | kHz |
| $e_n$ | Output Voltage Noise Density | At f = 1kHz<br>At f = 10kHz | | | 120<br>100 | | | 120<br>100 | | | 120<br>100 | | nV√Hz<br>nV√Hz |
| | Output Voltage Noise | 0.1Hz to 10Hz | | | 15 | | | 15 | | | 15 | | $\mu V_{P-P}$ |

## TIMING CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. REF A = REF B = REF C = REF D = 4.096V ($V_{CC}$ = 5V), REF A = REF B = REF C = REF D = 2.048V ($V_{CC}$ = 2.5V), REF LO = 0V, $V_{OUT}$ unloaded, unless otherwise noted. (Note 10)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$V_{CC}$ = 2.5V to 5.5V** | | | | | | | |
| $t_1$ | SDI Valid to SCK Setup | | ● | 4 | | | ns |
| $t_2$ | SDI Valid to SCK Hold | | ● | 4 | | | ns |
| $t_3$ | SCK High Time | | ● | 9 | | | ns |
| $t_4$ | SCK Low Time | | ● | 9 | | | ns |
| $t_5$ | $\overline{CS}$/LD Pulse Width | | ● | 10 | | | ns |
| $t_6$ | LSB SCK High to $\overline{CS}$/LD High | | ● | 7 | | | ns |
| $t_7$ | $\overline{CS}$/LD Low to SCK High | | ● | 7 | | | ns |
| $t_8$ | SDO Propagation Delay from SCK Falling Edge | $C_{LOAD}$ = 10pF<br>$V_{CC}$ = 4.5V to 5.5V<br>$V_{CC}$ = 2.5V to 5.5V | <br>●<br>● | | | <br>20<br>45 | <br>ns<br>ns |
| $t_9$ | $\overline{CLR}$ Pulse Width | | ● | 20 | | | ns |

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| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{10}$ | $\overline{CS}$/LD High to SCK Positive Edge | | ● | 7 | | | ns |
| | SCK Frequency | 50% Duty Cycle | ● | | | 50 | MHz |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Linearity and monotonicity are defined from code $k_L$ to code $2^N - 1$, where N is the resolution and $k_L$ is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For $V_{REF}$ = 4.096V and N = 16, $k_L$ = 256, linearity is defined from code 256 to code 65,535.

**Note 3:** Digital inputs at 0V or $V_{CC}$.

**Note 4:** DC crosstalk is measured with $V_{CC}$ = 5V and $V_{REF}$ = 4.096V, with the measured DAC at midscale, unless otherwise noted.

**Note 5:** $R_L$ = 2kΩ to GND or $V_{CC}$.

**Note 6:** Guaranteed by design and not production tested.

**Note 7:** Inferred from measurement at code 256 (LTC2604), code 64 (LTC2614) or code 16 (LTC2624), and at full scale.

**Note 8:** $V_{CC}$ = 5V, $V_{REF}$ = 4.096V. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2k in parallel with 200pF to GND.

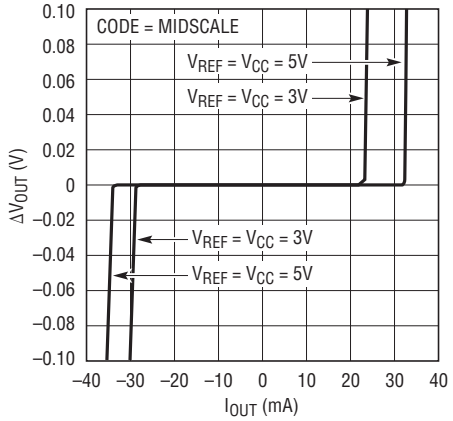
**Note 9:** $V_{CC}$ = 5V, $V_{REF}$ = 4.096V. DAC is stepped 1LSB between half scale and half scale –1. Load is 2k in parallel with 200pF to GND.

**Note 10:** These specifications apply to LTC2604/LTC2604-1, LTC2614/LTC2614-1, LTC2624/LTC2624-1.

## TYPICAL PERFORMANCE CHARACTERISTICS

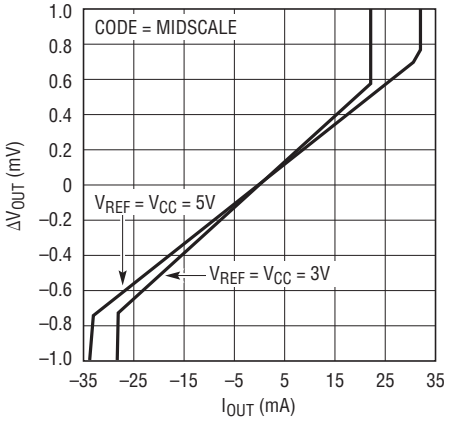
**(LTC2604/LTC2604-1, LTC2614/LTC2614-1, LTC2624/LTC2624-1)**

**Current Limiting**



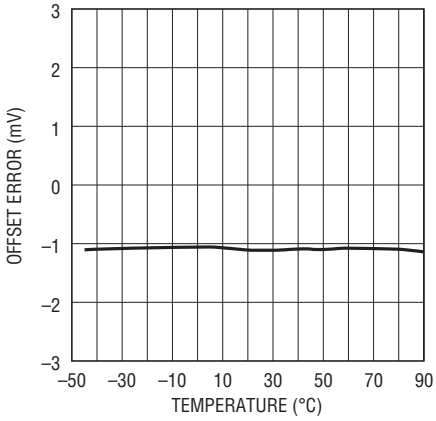

2604 G01

**Load Regulation**



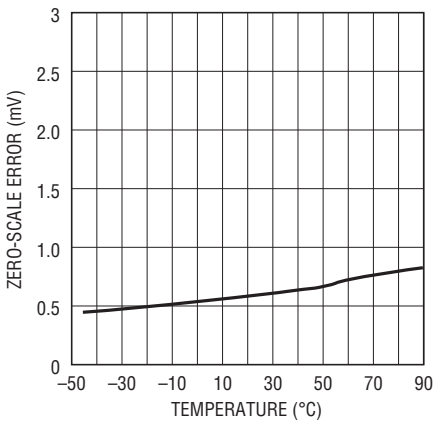

2604 G02

**Offset Error vs Temperature**



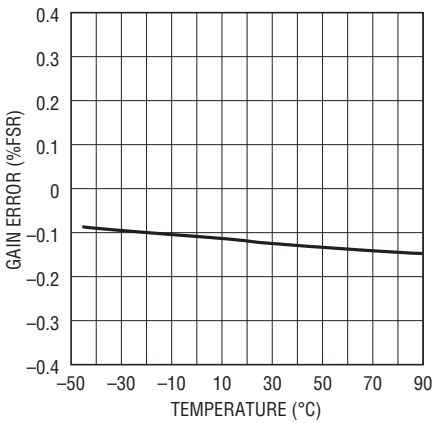

2604 G03

**Zero-Scale Error vs Temperature**



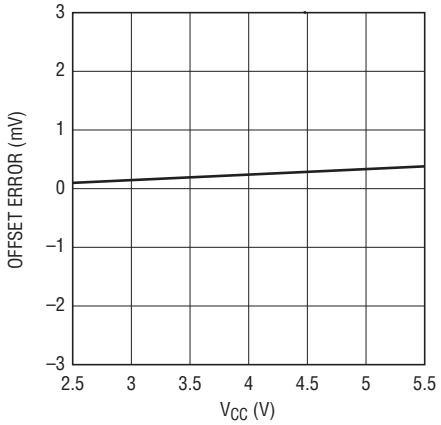

2604 G04

**Gain Error vs Temperature**




2604 G05

**Offset Error vs $V_{CC}$**

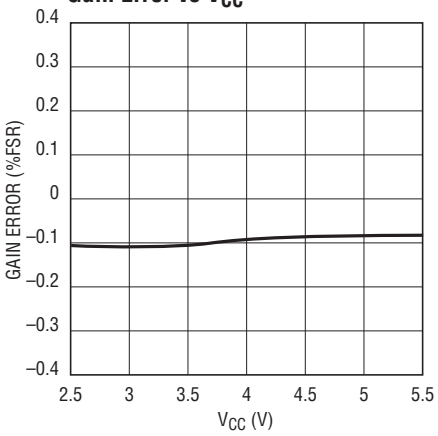



2604 G06

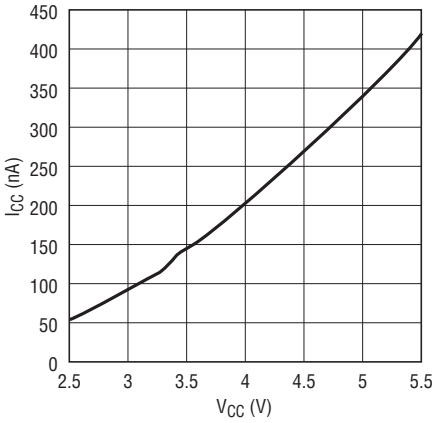
## TYPICAL PERFORMANCE CHARATERISTICS

**(LTC2604/LTC2604-1, LTC2614/LTC2614-1, LTC2624/LTC2624-1)**

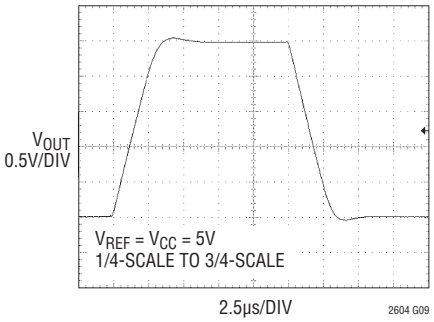
### Gain Error vs $V_{CC}$



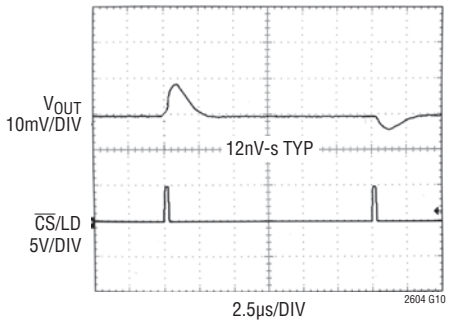

### $I_{CC}$ Shutdown vs $V_{CC}$



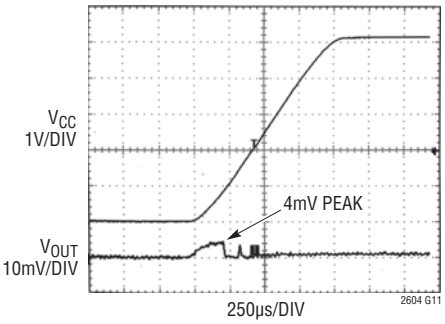

### Large-Signal Settling



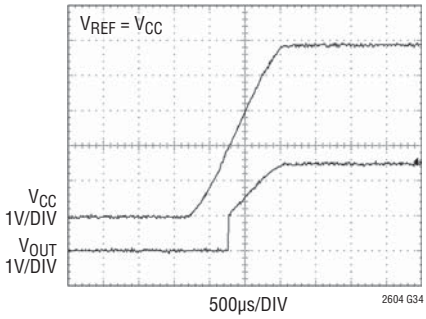

### Midscale Glitch Impulse



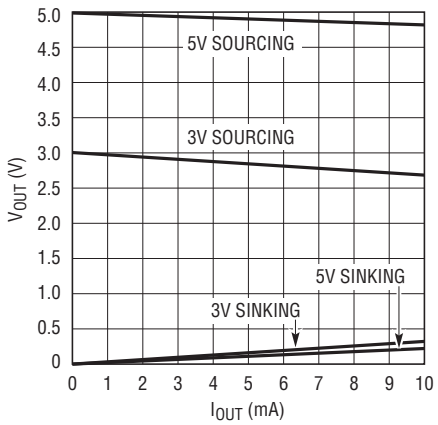

### Power-On Reset Glitch



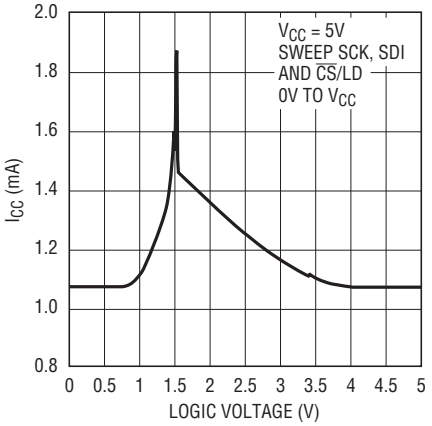

### Power-On Reset to Midscale



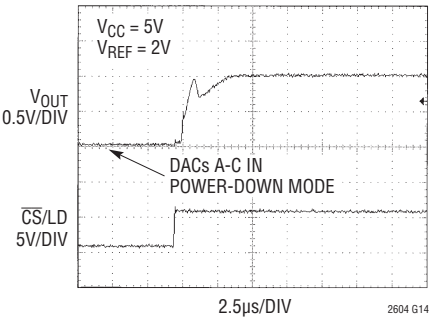

### Headroom at Rails vs Output Current




### Supply Current vs Logic Voltage



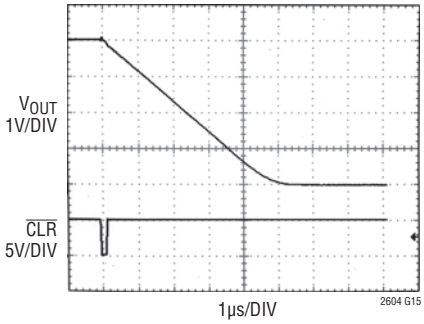

### Exiting Power-Down to Midscale



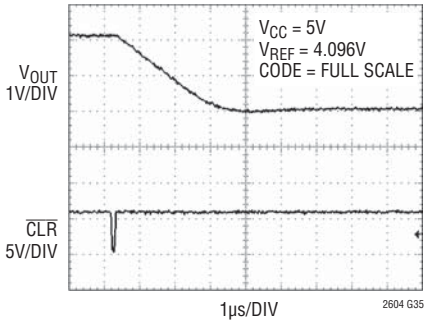
# TYPICAL PERFORMANCE CHARATERISTICS

**(LTC2604/LTC2604-1, LTC2614/LTC2614-1, LTC2624/LTC2624-1)**

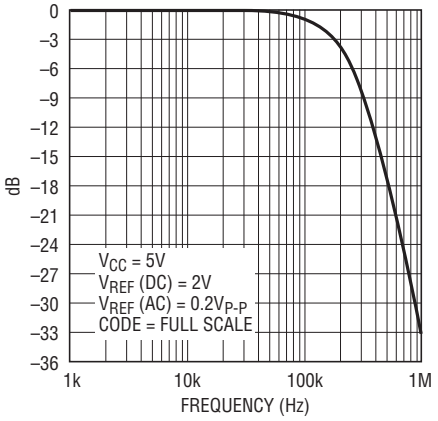
### Hardware $\overline{CLR}$



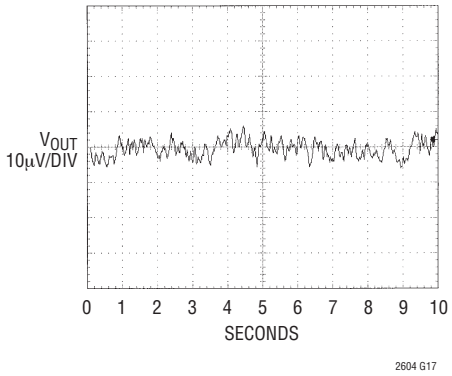

### Hardware $\overline{CLR}$ to Midscale



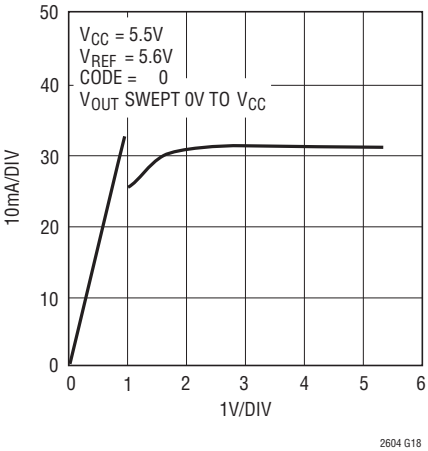

### Multiplying Frequency Response



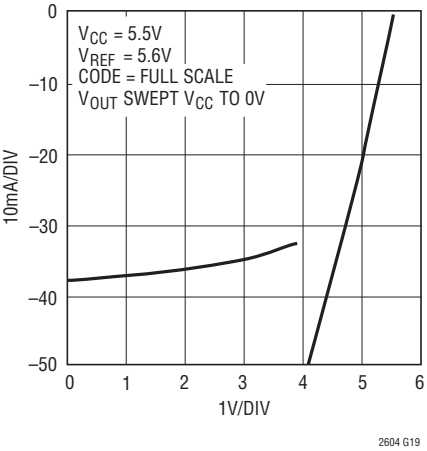

### Output Voltage Noise, 0.1Hz to 10Hz




### Short-Circuit Output Current vs $V_{OUT}$ (Sinking)

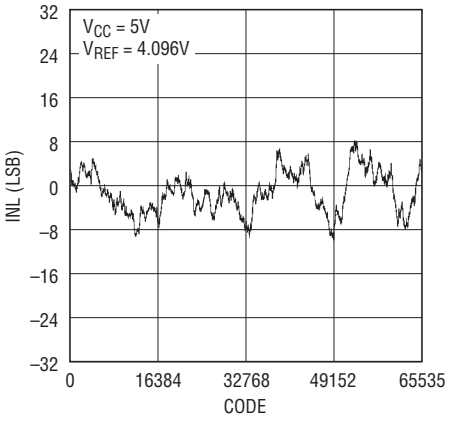



### Short-Circuit Output Current vs $V_{OUT}$ (Sourcing)

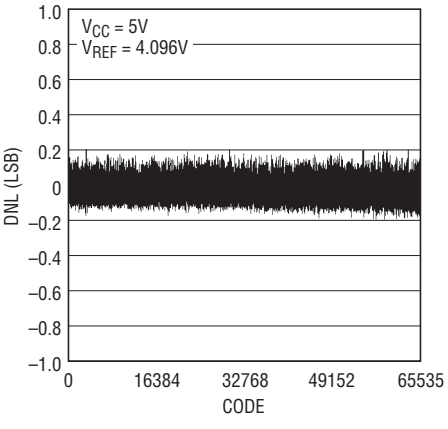



**(LTC2604/LTC2604-1)**

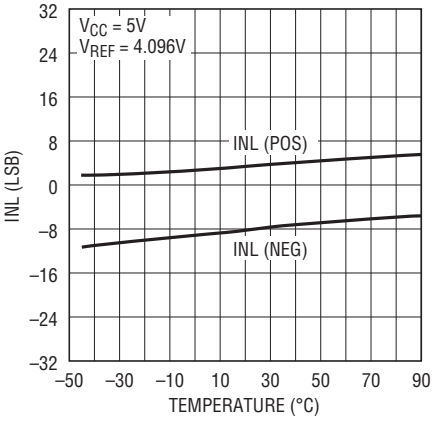
### Integral Nonlinearity (INL)




### Differential Nonlinearity (DNL)



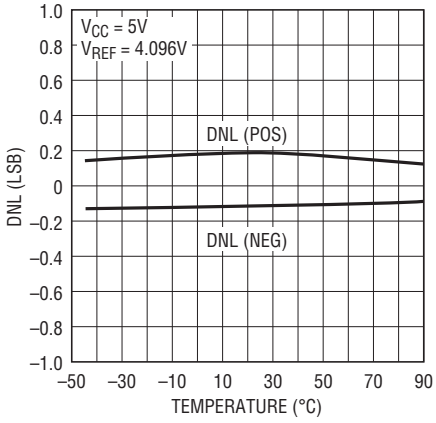

### INL vs Temperature



## TYPICAL PERFORMANCE CHARATERISTICS

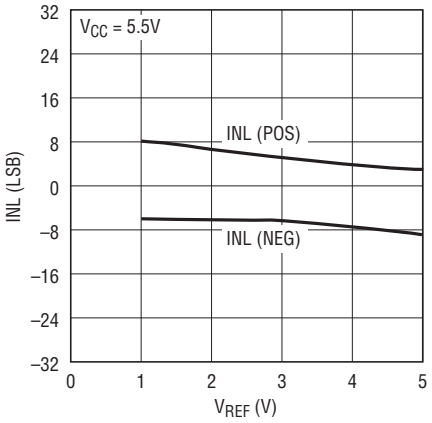
**(LTC2604/LTC2604-1)**

### DNL vs Temperature



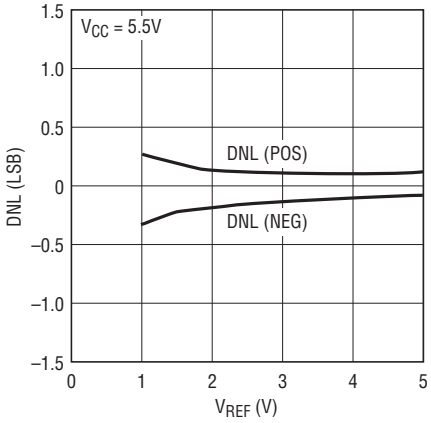

2604 G23

### INL vs $V_{REF}$



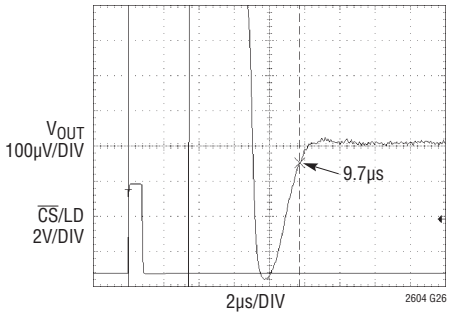

2604 G24

### DNL vs $V_{REF}$




2604 G25

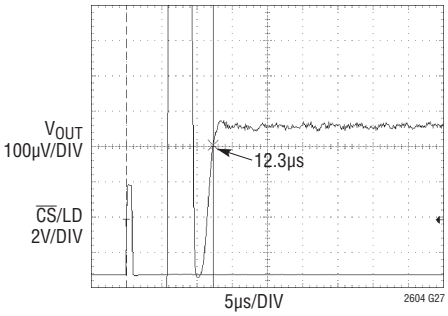
### Settling to ±1LSB




2604 G26

$V_{CC}$ = 5V, $V_{REF}$ = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
$R_L$ = 2k, $C_L$ = 200pF
AVERAGE OF 2048 EVENTS

### Settling of Full-Scale Step

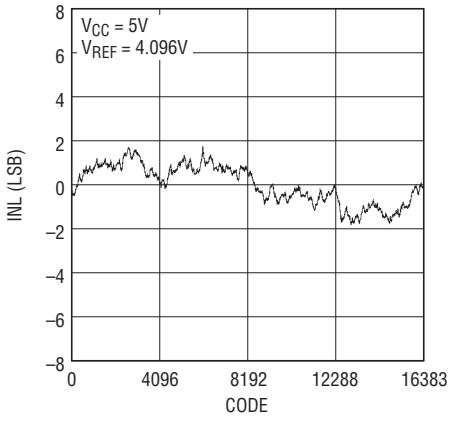



2604 G27

$V_{CC}$ = 5V, $V_{REF}$ = 4.096V
CODE 512 TO 65535 STEP
AVERAGE OF 2048 EVENTS
SETTLING TO ±1LSB

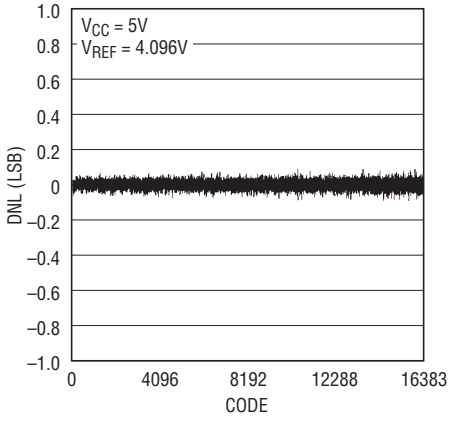
**(LTC2614/LTC2614-1)**

### Integral Nonlinearity (INL)



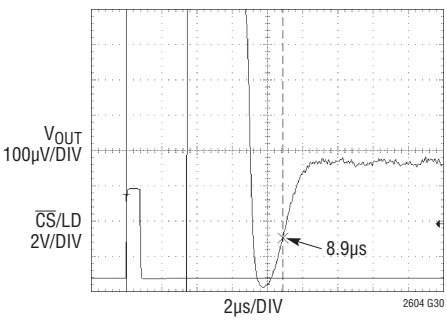

2604 G28

### Differential Nonlinearity (DNL)




2604 G29

### Settling to ±1LSB



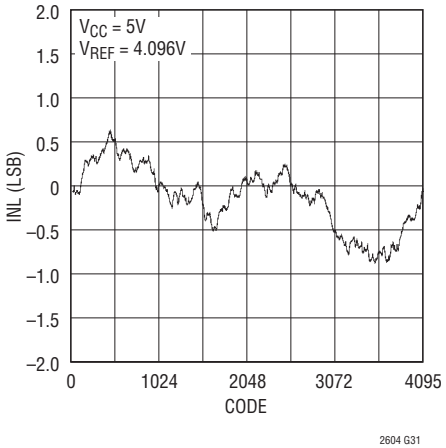

2604 G30

$V_{CC}$ = 5V, $V_{REF}$ = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
$R_L$ = 2k, $C_L$ = 200pF
AVERAGE OF 2048 EVENTS

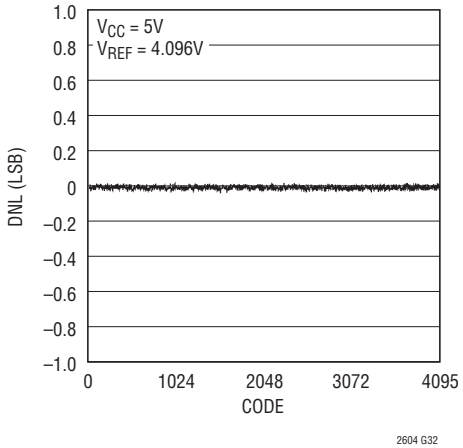
## TYPICAL PERFORMANCE CHARATERISTICS

**(LTC2624/LTC2624-1)**

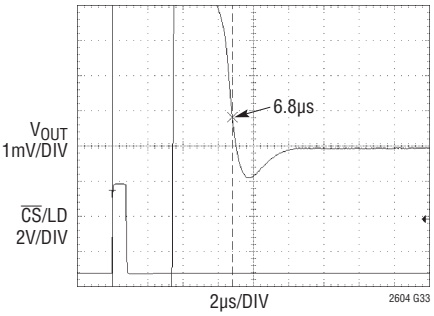
**Integral Nonlinearity (INL)**




**Differential Nonlinearity (DNL)**




**Settling to ±1LSB**




$V_{CC}$ = 5V, $V_{REF}$ = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
$R_L$ = 2k, $C_L$ = 200pF
AVERAGE OF 2048 EVENTS

## PIN FUNCTIONS

**GND (Pin 1):** Analog Ground.

**REF LO (Pin 2):** Reference Low. The voltage at this pin sets the zero scale (ZS) voltage of all DACs. This pin can be raised up to 1V above ground at $V_{CC}$ = 5V or 100mV above ground at $V_{CC}$ = 3V.

**REF A, REF B, REF C, REF D (Pins 3, 6, 12, 15):** Reference Voltage Inputs for each DAC. REF x sets the full scale voltage of the DACs. 0V ≤ REF x ≤ $V_{CC}$.

**$V_{OUT\,A}$ to $V_{OUT\,D}$ (Pins 4, 5, 13, 14):** DAC Analog Voltage Outputs. The output range is from REF LO to REF x.

**$\overline{CS}$/LD (Pin 7):** Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

**SCK (Pin 8):** Serial Interface Clock Input. CMOS and TTL compatible.

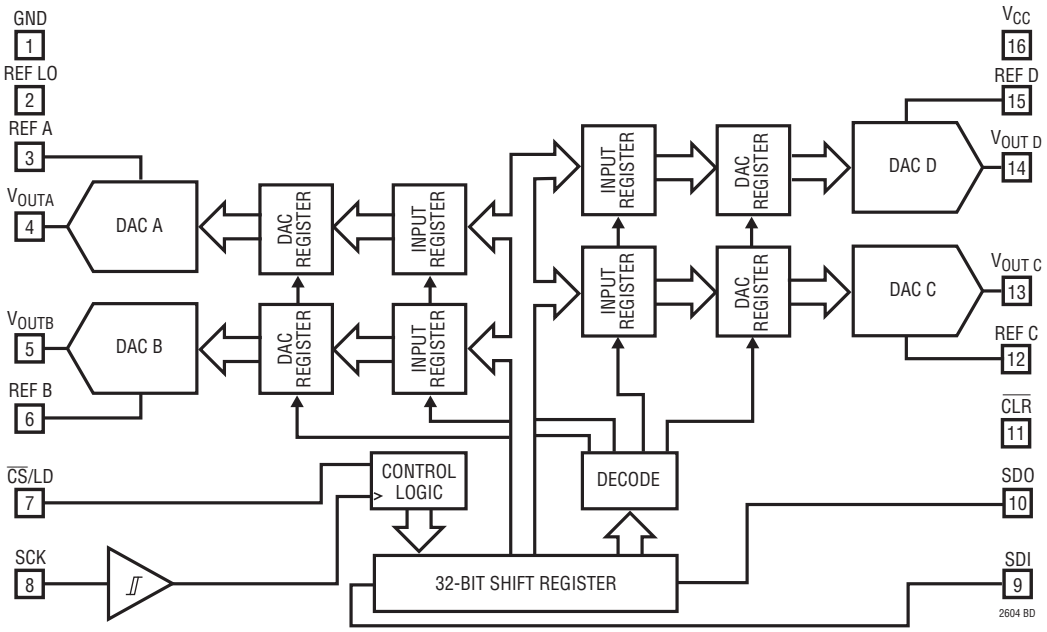
**SDI (Pin 9):** Serial Interface Data Input. Data is applied to SDI for transfer to the device at the rising edge of SCK. The LTC2604/LTC2604-1, LTC2614/LTC2614-1, LTC2624/LTC2624-1 accept input word lengths of either 24 or 32 bits.

**SDO (Pin 10):** Serial Interface Data Output. This pin is used for daisy-chain operation. The serial output of the shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. SDO is an active output and does not go high impedance, even when CS/LD is taken to a logic high level.

**$\overline{CLR}$ (Pin 11):** Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage outputs to drop to 0V for the LTC2604/LTC2614/LTC2624. A logic low at this input sets all registers to midscale code and causes the DAC voltage outputs to go to midscale for the LTC2604-1/LTC2614-1/LTC2624-1. CMOS and TTL compatible.

**$V_{CC}$ (Pin 16):** Supply Voltage Input. 2.5V ≤ $V_{CC}$ ≤ 5.5V.

## BLOCK DIAGRAM




## TIMING DIAGRAM

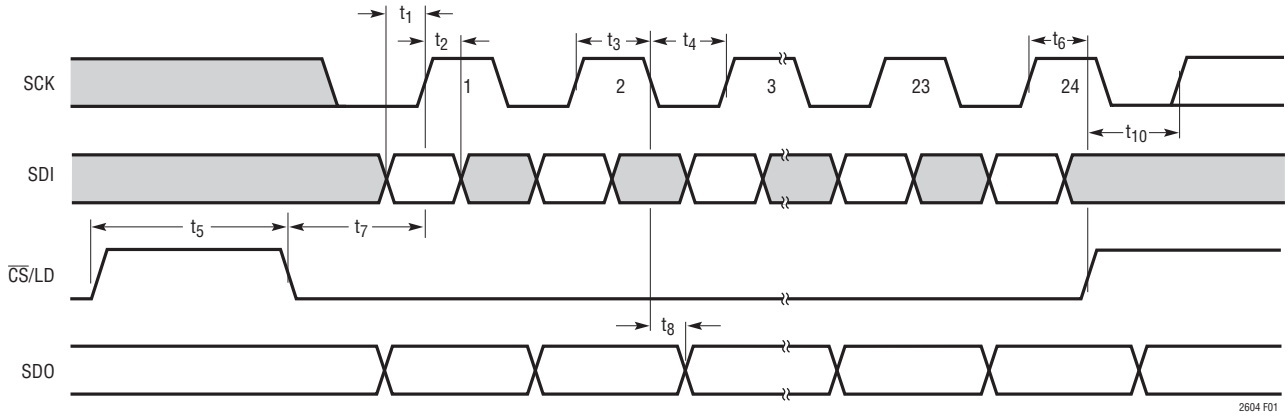



**Figure 1**

## OPERATION

### Power-On Reset

The LTC2604/LTC2614/LTC2624 clear the outputs to zero scale when power is first applied, making system initialization consistent and repeatable. The LTC2604-1/LTC2614-1/LTC2624-1 set the voltage outputs to midscale when power is first applied.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2604/LTC2614/LTC2624 contain circuitry to reduce the power-on glitch; furthermore, the glitch amplitude can be made arbitrarily small by reducing the ramp rate of the power supply. For example, if the power supply is ramped to 5V in 1ms, the analog outputs rise less than 10mV above ground (typ) during power-on. See Power-On Reset Glitch in the Typical Performance Characteristics section.

## OPERATION

### Power Supply Sequencing

The voltage at REF (Pins 3, 6, 12 and 15) should be kept within the range $-0.3V \le REF\,x \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at $V_{CC}$ (Pin 16) is in transition.

### Transfer Function

The digital-to-analog transfer function is

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)[REF\,x - REFLO] + REFLO$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and REF x is the voltage at REF A, REF B, REF C and REF D (Pins 3, 6, 12 and 15).

### Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, powering-on the SDI and SCK buffers and enabling the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 16-, 14- or 12-bit input code, ordered MSB-to-LSB, followed by 0, 2 or 4 don't-care bits (LTC2604, LTC2614 and LTC2624 respectively). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 2a.

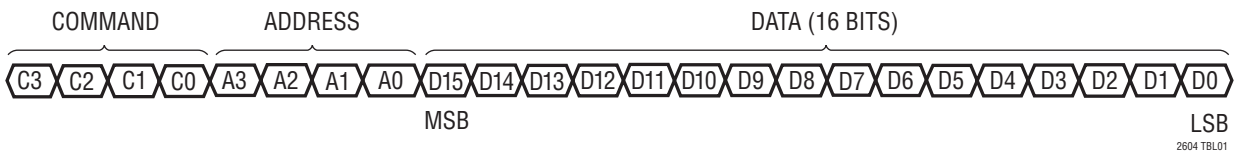
**Table 1.**

| COMMAND* | | | | |
|---|---|---|---|---|
| **C3** | **C2** | **C1** | **C0** | |
| 0 | 0 | 0 | 0 | Write to Input Register n |
| 0 | 0 | 0 | 1 | Update (Power Up) DAC Register n |
| 0 | 0 | 1 | 0 | Write to Input Register n, Update (Power Up) All n |
| 0 | 0 | 1 | 1 | Write to and Update (Power Up) n |
| 0 | 1 | 0 | 0 | Power Down n |
| 1 | 1 | 1 | 1 | No Operation |
| **ADDRESS (n)*** | | | | |
| **A3** | **A2** | **A1** | **A0** | |
| 0 | 0 | 0 | 0 | DAC A |
| 0 | 0 | 0 | 1 | DAC B |
| 0 | 0 | 1 | 0 | DAC C |
| 0 | 0 | 1 | 1 | DAC D |
| 1 | 1 | 1 | 1 | All DACs |

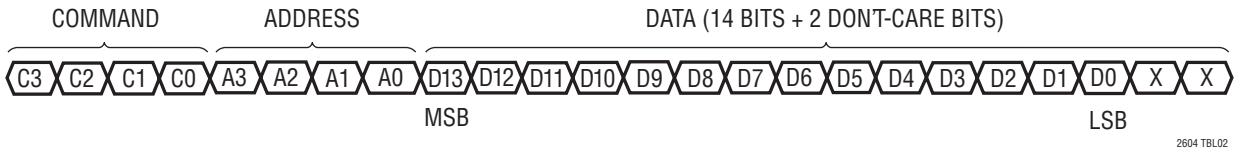
*Command and address codes not shown are reserved and should not be used.

The command (C3-C0) and address (A3-A0) assignments are shown in Table 1. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register of the selected DAC, n. An update

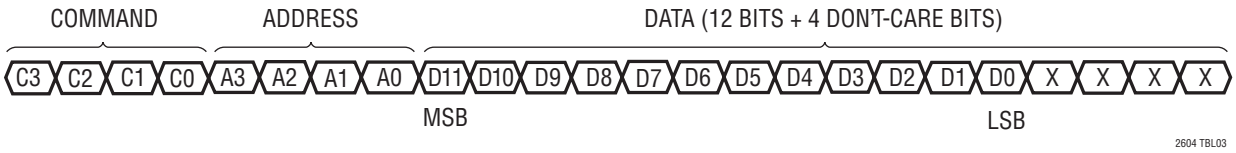
**INPUT WORD (LTC2604)**




**INPUT WORD (LTC2614)**




**INPUT WORD (LTC2624)**



## OPERATION

operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 16-, 14- or 12-bit input code, and is converted to an analog voltage at the DAC output. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the block diagram.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits are transferred to the device first, followed by the 24-bit word as just described. Figure 2b shows the 32-bit sequence. The 32-bit word is required for daisy-chain operation, and is also available to accommodate microprocessors which have a minimum word width of 16 bits (2 bytes).

### Daisy-Chain Operation

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e., SCK, SDI and $\overline{CS}$/LD). Such a "daisy-chain" series is configured by connecting SDO of each upstream device to SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then the concatenated input data is transferred to the chain, using SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the no-operation command (1111) for the other devices in the chain.

### Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than four outputs are needed. When in power-down, the buffer amplifiers, bias circuits and reference inputs are disabled, and draw essentially zero current. The DAC outputs are put into a high-impedance state, and the output pins are passively pulled to ground through individual 90k resistors. Input- and DAC-register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command $0100_b$ in combination with the appropriate DAC address, (n). The 16-bit data word is ignored. The supply current is reduced by approximately 1/4 for each DAC powered down. The effective resistance at REF x (pins 3, 6, 12 and 15) are at high-impedance input (typically > 1GΩ) when the corresponding DACs are powered down.

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 1. The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If less than four DACs are in a powered-down state prior to the update command, the power-up delay time is 5µs. If on the other hand, all four DACs are powered down, then the main bias generation circuit block has been automatically shut down in addition to the individual DAC amplifiers and reference inputs. In this case, the power up delay time is 12µs (for $V_{CC}$ = 5V) or 30µs (for $V_{CC}$ = 3V).

### Voltage Outputs

Each of the four rail-to-rail amplifiers contained in these parts has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

## OPERATION

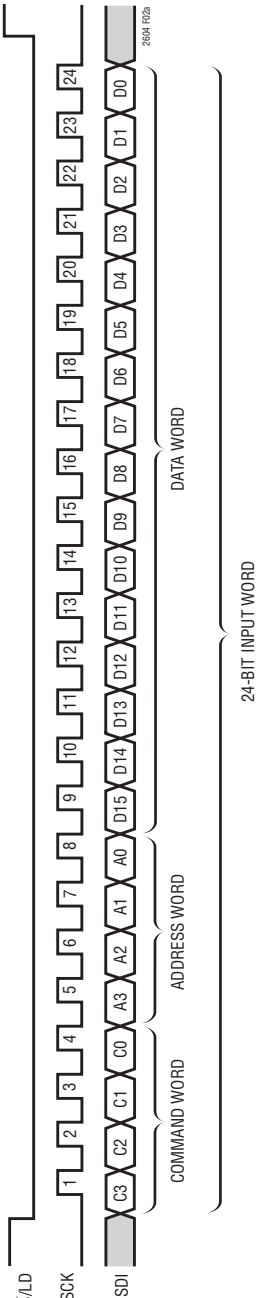



**Figure 2a. LTC2604 24-Bit Load Sequence (Minimum Input Word)**
**LTC2614 SDI Data Word: 14-Bit Input Code + 2 Don't Care Bits**
**LTC2624 SDI Data Word: 12-Bit Input Code + 4 Don't Care Bits**

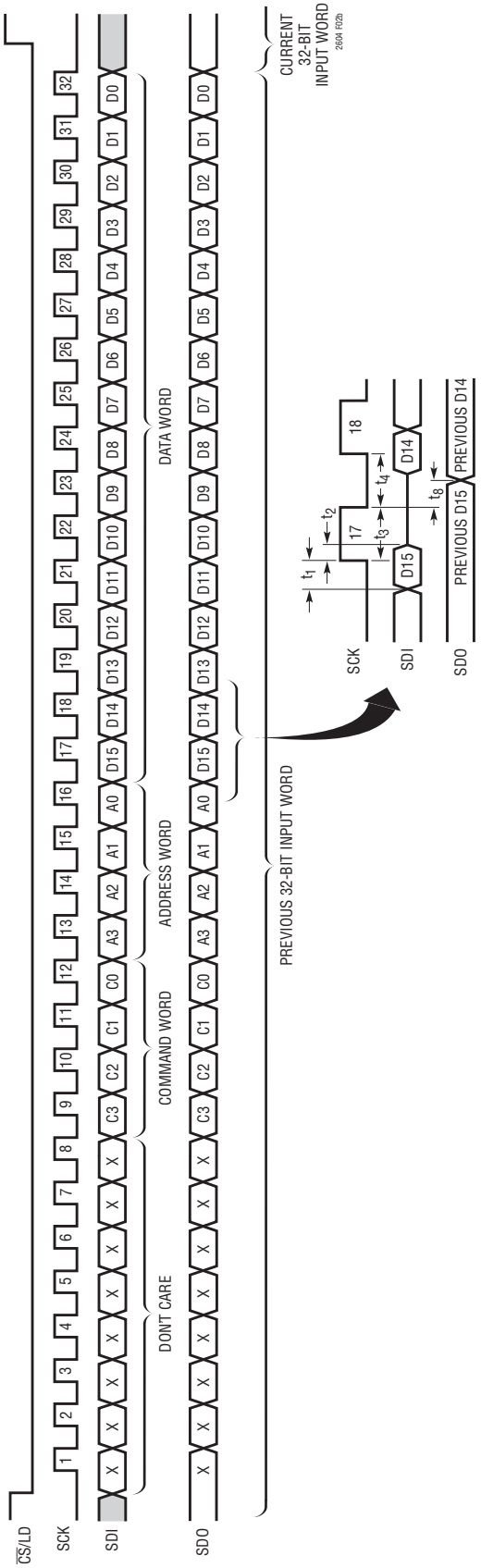



**Figure 2b. LTC2604 32-Bit Load Sequence**
**LTC2614 SDI/SDO Data Word: 14-Bit Input Code + 2 Don't Care Bits**
**LTC2624 SDI/SDO Data Word: 12-Bit Input Code + 4 Don't Care Bits**

## OPERATION

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifiers' DC output impedance is 0.025Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 30Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 30Ω • 1mA = 30mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

### Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by keeping "signal" and "power" grounds separate.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin functions as a return path for power supply currents in the device and should be connected to analog ground. Resistance from the GND pin to system star ground should be as low as possible. When a zero scale DAC output voltage of zero is desired, the REFLO pin (pin 2) should be connected to system star ground.

### Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog outputs of the device cannot go below ground, they may limit for the lowest codes as shown in Figure 3b. Similarly, limiting can occur near full scale when the REF pins are tied to $V_{CC}$. If REF x = $V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at $V_{CC}$ as shown in Figure 3c. No full-scale limiting can occur if REF x is less than $V_{CC}$ – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

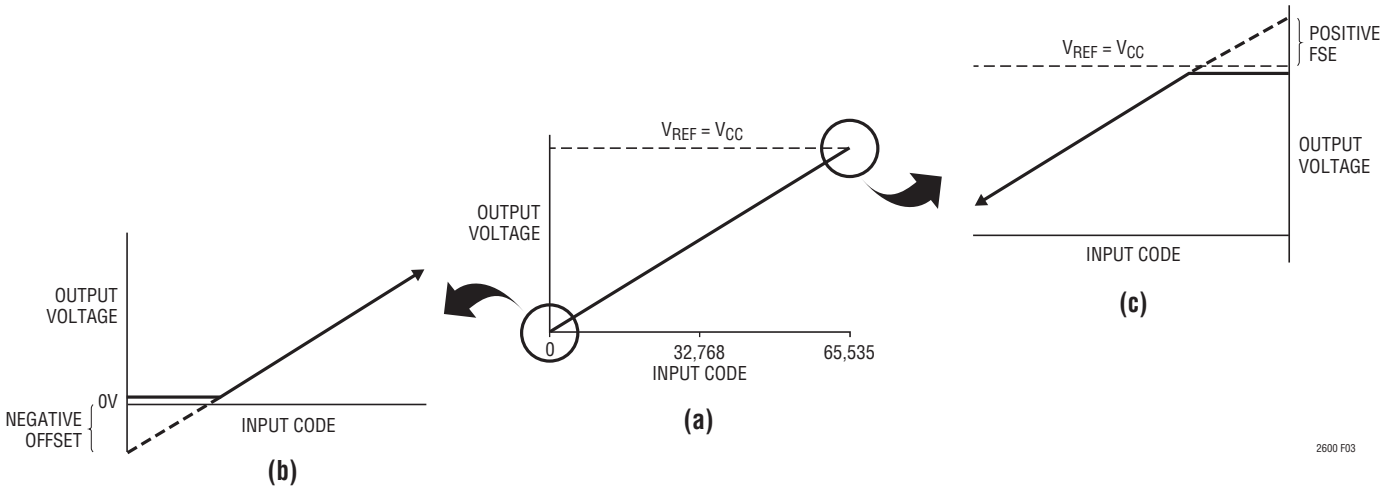
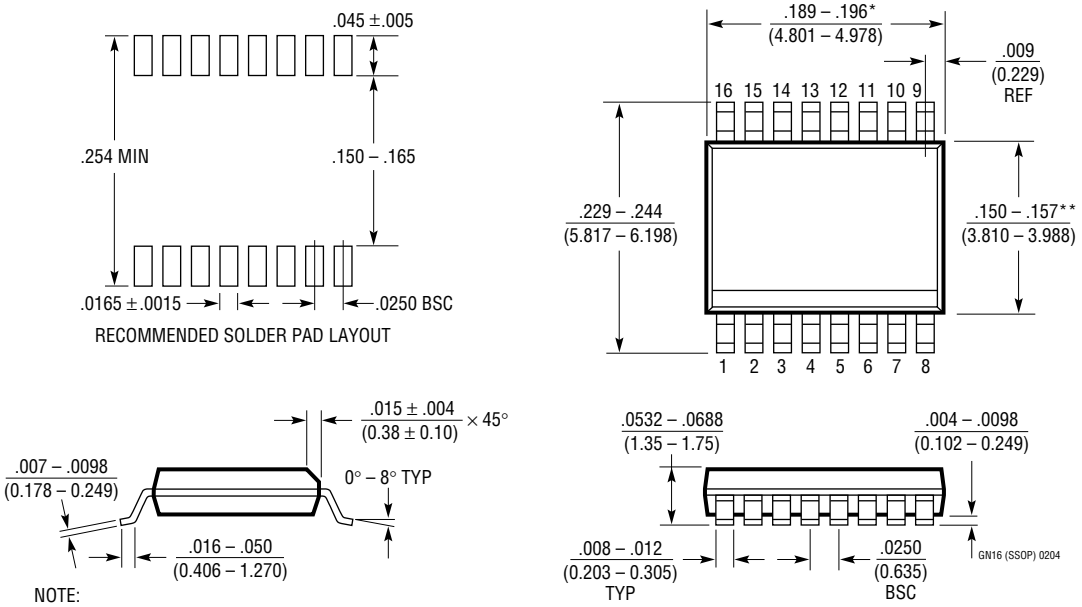



**Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Codes Near Full Scale**

# PACKAGE DESCRIPTION

**GN Package**
**16-Lead Plastic SSOP (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1641)




NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## TYPICAL APPLICATION

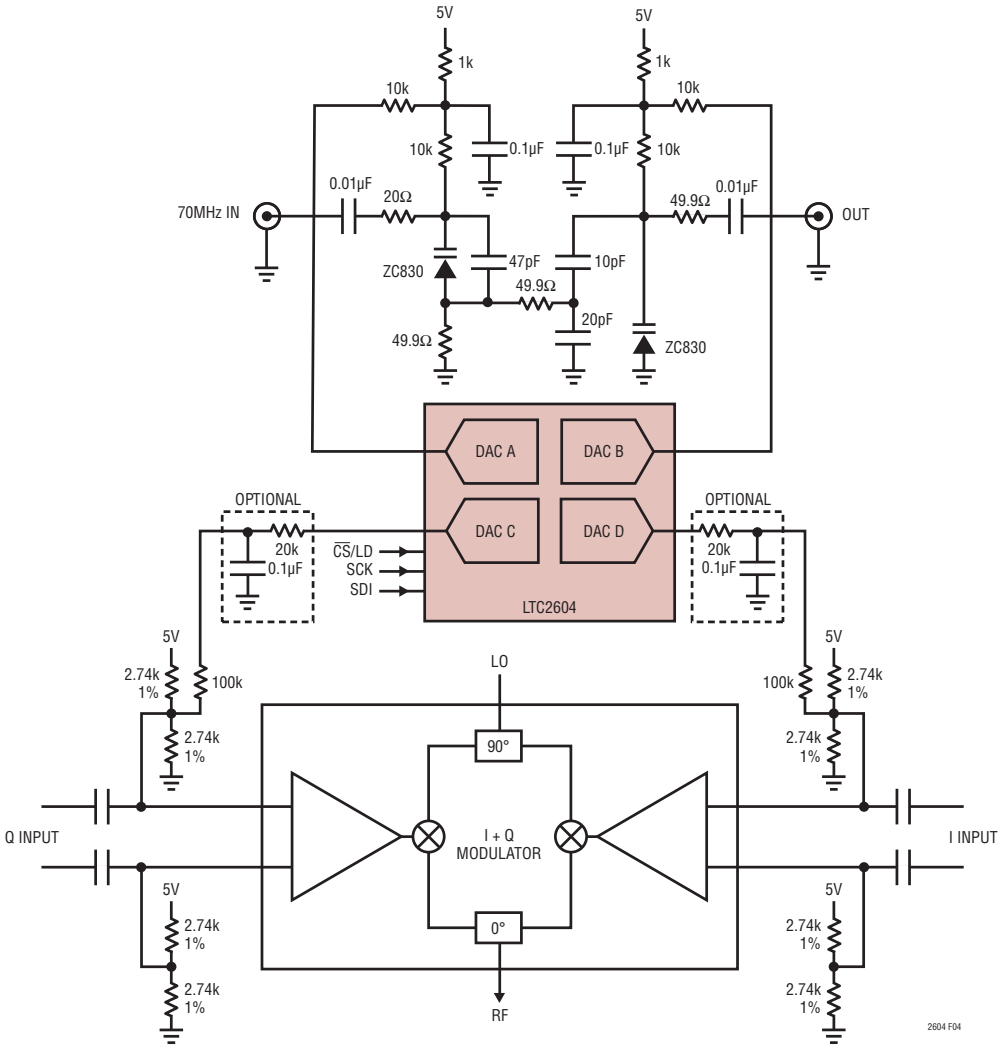



**Figure 4. Using DAC A and DAC B for Nearly Continuous Attenuation Control and DAC C and DAC D to Trim for Minimum LO Feedthrough in a Mixer**

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1458/LTC1458L | Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality | LTC1458: $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ = 0V to 4.096V<br>LTC1458L: $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ = 0V to 2.5V |
| LTC1654 | Dual 14-Bit Rail-to-Rail $V_{OUT}$ DAC | Programmable Speed/Power |
| LTC1655/LTC1655L | Single 16-Bit $V_{OUT}$ DAC with Serial Interface in SO-8 | $V_{CC}$ = 5V(3V), Low Power, Deglitched |
| LTC1657/LTC1657L | Parallel 5V/3V 16-Bit $V_{OUT}$ DAC | Low Power, Deglitched, Rail-to-Rail $V_{OUT}$ |
| LTC1660/LTC1665 | Octal 8-Bit/10-Bit $V_{OUT}$ DAC in 16-Pin Narrow SSOP | $V_{CC}$ = 2.7V to 5.5V, Micropower, Rail-to-Rail Output |
| LTC1821 | Parallel 16-Bit Voltage Output DAC | Precision 16-Bit Settling in 2µs for 10V Step |
| LTC2600/LTC2610/LTC2620 | Octal 16-Bit/14-Bit/12-Bit Rail-to-Rail DACs in 16-Lead SSOP | 250µA per DAC, 2.5V to 5.5V Supply Range |
| LTC2602/LTC2612/LTC2622 | Dual 16-Bit/14-Bit/12-Bit Rail-to-Rail DACs in 8-Lead MSOP | 300µA per DAC, 2.5V to 5.5V Supply Range |


Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9