



AS4C32M16MD1

512M (32M x16 bit) Mobile DDR SDRAM

Confidential

(Rev. 2.0, Feb. /2014)

LPDDR MEMORY

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Revision History

| Revision No | Description | Date |
|-------------|---|------------|
| 1.0 | Initial Release | 2014/02/04 |
| 2.0 | Clock frequency to 200MHz – data rate: 400Mbps – 5ns access speed option update | 2014/02/17 |

512M (32M x16 bit) Mobile DDR SDRAM

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1. FEATURES

- **Density** : 512Mbit
- **Organization**
 - x16 bit : 8M words x 16bits x 4banks
- **Power supply** : VDD, VDDQ = 1.7 to 1.95V
- **Speed**
 - Clock frequency : 200MHz (max.)
 - Data rate : 400Mbps (max.)
- **2KB page size**
 - Row address : A0 to A12
 - Column address : A0 to A9 (x16 bits)
- **Four internal banks for concurrent operation**
- **Interface** : LVCMOS
- **Burst lengths (BL)** : 2, 4, 8, 16
- **Burst type (BT)**
 - Sequential : 2, 4, 8, 16
 - Interleave : 2, 4, 8, 16
- **CAS# latency (CL)** : 3
- **Precharge** : auto precharge option for each burst access
- **Driver strength** : normal, 1/2, 1/4, 1/8
- **Refresh** : auto-refresh, self-refresh
- **Refresh cycles** : 8192 cycles/64ms
 - Average refresh period : 7.8us
- **Operating junction temperature range**
 - Tj= -30°C to +85°C
- **Package**: 60-ball FBGA (8x9mm)
- **All parts are ROHS Compliant**
- Low power consumption
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- Deep power down mode
- Burst termination by burst stop command and precharge command
- DDL is not implemented
- Double-data-rate architecture :
 - Two data transfers per one clock cycle
- The high speed data transfer is realized by the 2bits prefetch pipelined architecture
- Bi-directional data strobe (DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data

2. GENERAL DESCRIPTION

This device is 536,870,912 bits of double data rate synchronous DRAM organized as 4 banks of 8,388,608 words by 16 bits. The synchronous operation with Data Strobe allows extremely high performance. JSC is applied to reduce leakage and refresh currents while achieving very high speed. I/O transactions are possible on both edges of the clock. The ranges of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

Table 1. Speed Grade Information

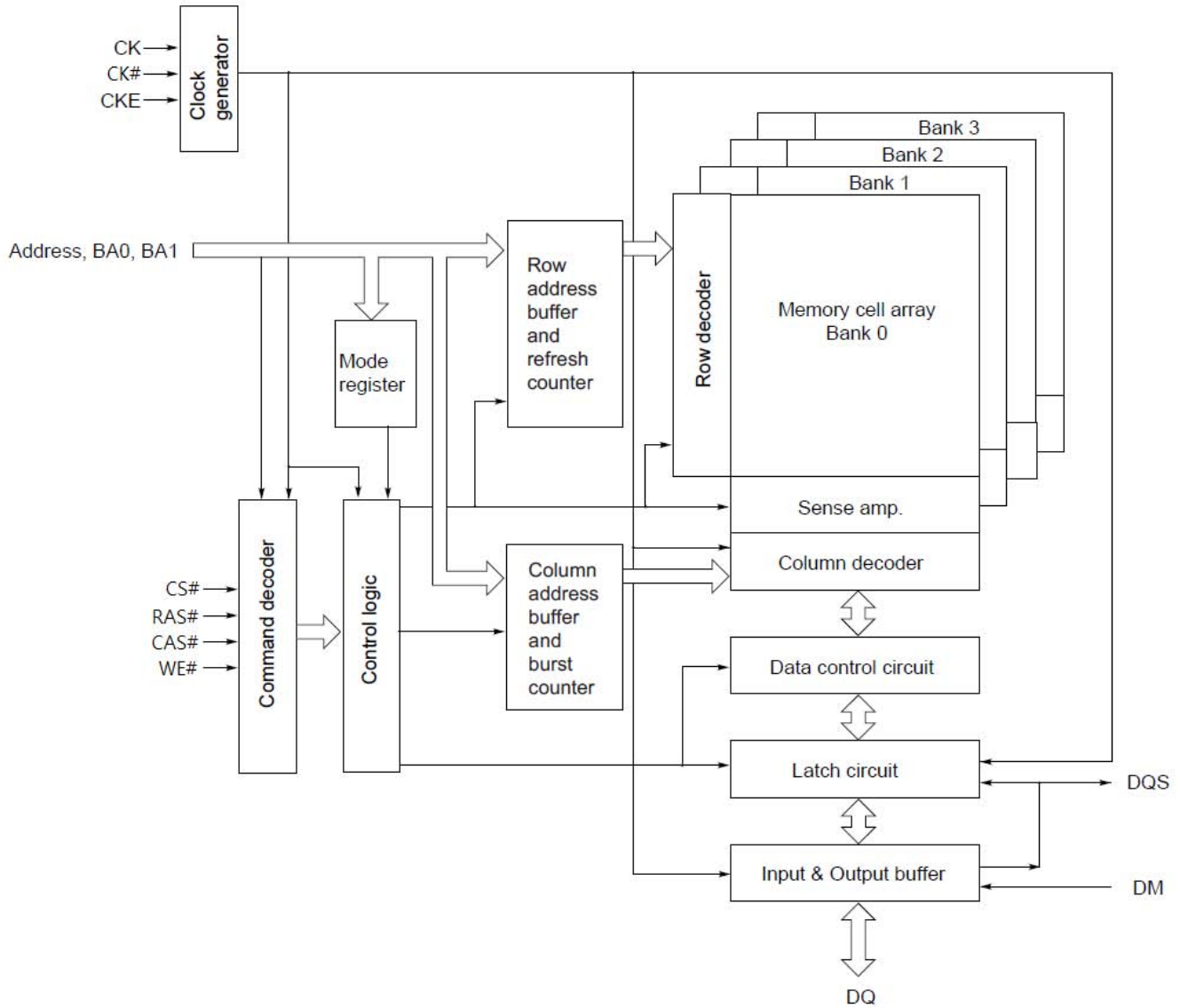
| Speed Grade – Data rate | Clock Frequency | CAS Latency | t _{RCD} (ns) | t _{RP} (ns) |
|-------------------------|-----------------|-------------|-----------------------|----------------------|
| 400Mbps (max) | 200 MHz (max) | 3 | 15 | 15 |

Table 2 – Ordering Information for ROHS Compliant Products

| Product part No | Org | Temperature | Max Clock (MHz) | Package |
|-------------------|---------|---------------|-----------------|--------------|
| AS4C32M16MD1-5BCN | 32 x 16 | -30°C to 85°C | 200 | 60-ball FBGA |

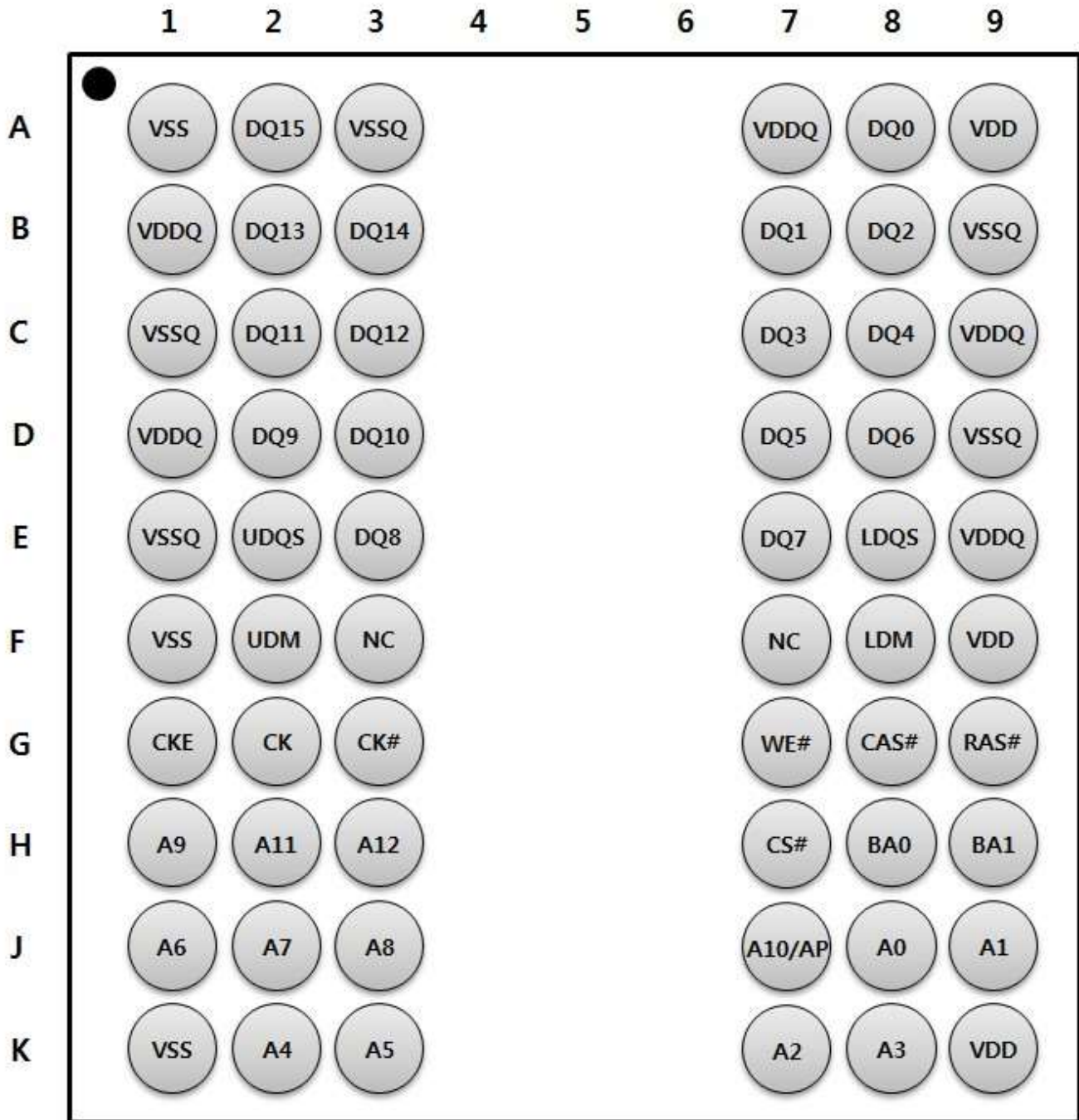
2.1 Block Diagram

Figure 2.1 Block Diagram



2.2 Package Pin Configurations

Figure 2.2 Pin configurations



< Top View >

2.4 Pin Description

CK, CK# (input pins)

The CK and the CK# are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the CK# falling edge. When a read operation, DQSs and DQs are referred to the cross point of the CK and the CK#. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VDDQ/2 level. DQSs for write operation are referred to the cross point of the CK and the CK#. The other input signals are referred at CK rising edge.

CS# (input pin)

When CS# is low, commands and data can be input. When CS# is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

RAS#, CAS#, and WE# (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins)

Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the CK# falling edge in a bank active command cycle. Column address is loaded at the cross point of the CK rising edge and the CK# falling edge in a read or a write command cycle (See Table 2.1). This column address becomes the starting address of a burst operation.

Table 2.1 Address Pins

| Page size | Organization | Address (A0 to A12) | |
|-----------|--------------|-----------------------|----------------|
| | | Row address | Column address |
| 2KB | x16 bits | AX0 to AX12 | AY0 to AY9 |

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = high when a precharge command is issued, all banks are pre-charged. If A10 = low when a precharge command is issued, only the bank that is selected by BA1/BA0 is pre-charged. If A10 = high when read or write command, auto precharge function is enabled.

BA0 and BA1 (input pins)

BA0 and BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Table 2.2)

Table 2.2 Bank Select Signal

| | BA0 | BA1 |
|--------|------------|------------|
| Bank 0 | L | L |
| Bank 1 | H | L |
| Bank 2 | L | H |
| Bank 3 | H | H |

Note : H = VIH , L = VIL

CKE (input pin)

CKE controls power-down mode, self-refresh function and deep power-down function with other command inputs. The CKE level must be kept for 2 clocks at least, that is, if CKE changes at the cross point of the CK rising edge and the CK# falling edge with proper setup time tIS, by the next CK rising edge CKE level must be kept with proper hold time tIH.

DQ0 to DQ15 (input/output pins)

Data are input to and output from these pins.

UDQS and LDQS (input and output pin)

DQS provides the read data strobes (as output) and the write data strobes (as input). Each DQS pin corresponds to eight DQ pins, respectively (See Table 2.3).

UDM and LDM (input pin)

DM is the reference signals of the data input mask function. DM is sampled at the cross point of DQS and VDDQ/2. When DM = high, the data input at the same timing are masked while the internal burst counter will be counting up. Each DM pin corresponds to eight DQ pins, respectively (See Table 2.3).

Table 2.3 DQS and DM Correspondence

| Organization | DQS | Data mask | DQs |
|---------------------|------------|------------------|-------------|
| x16 bits | LDQS | LDM | DQ0 to DQ7 |
| | UDQS | UDM | DQ8 to DQ15 |

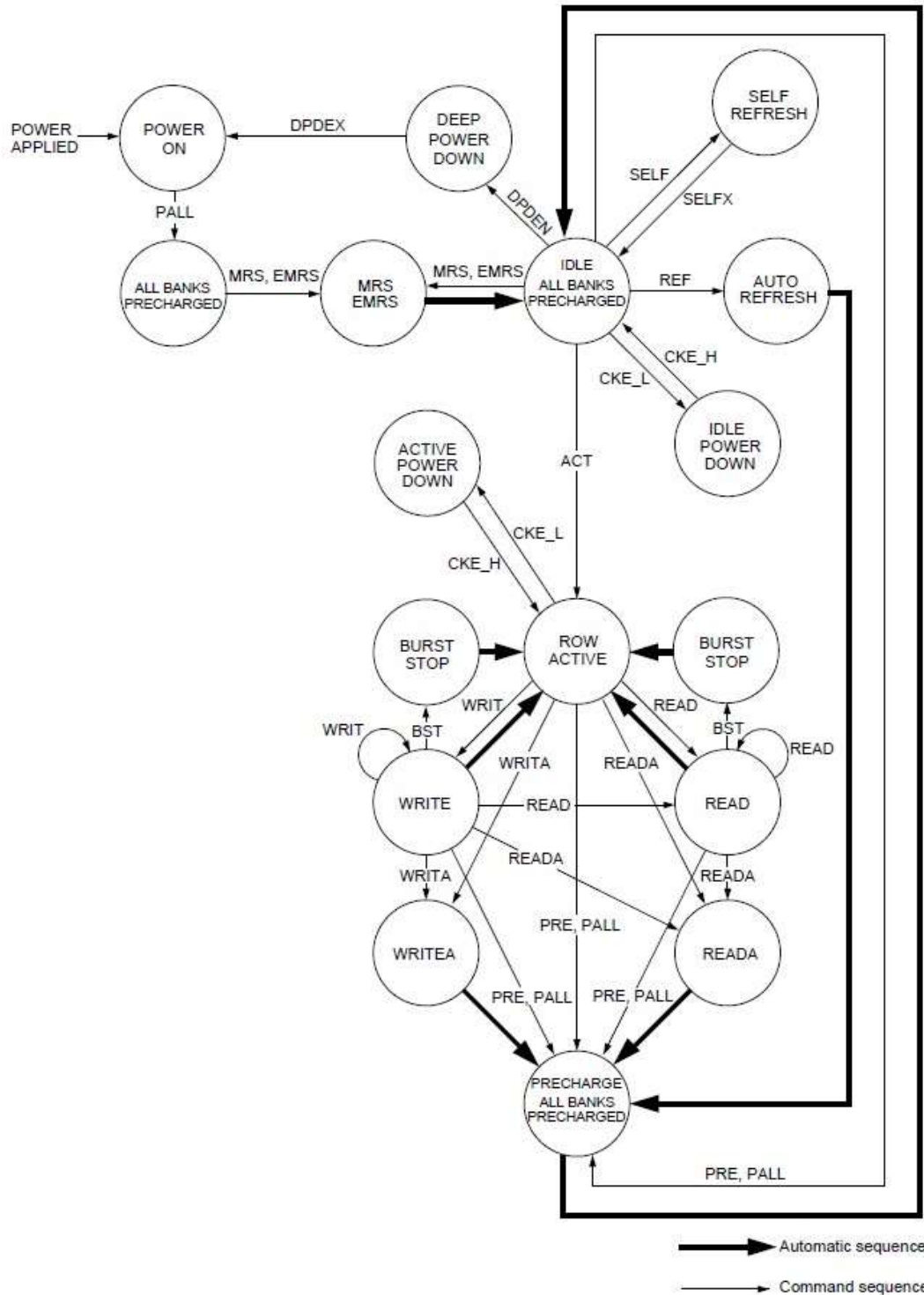
VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers. VDD must be equal to VDDQ.

3. Command Operation

3.1 Simplified State Diagram

Figure 3.1 State Diagram



3.2 Command Truth Table

The DDR Mobile RAM recognizes the following commands specified by the CS#, RAS#, CAS#, WE# and address pins.

Table 3.1 Command Truth Table

| Command | Symbol | CKE | | CS# | RAS# | CAS# | WE# | BA1 | BA0 | AP | Addr. |
|------------------------------------|--------|-----|---|-----|------|------|-----|-----|-----|----|-------|
| | | n-1 | n | | | | | | | | |
| Ignore command | DESL | H | H | H | X | X | X | X | X | X | X |
| No operation | NOP | H | H | L | H | H | H | X | X | X | X |
| Burst stop command | BST | H | H | L | H | H | L | X | X | X | X |
| Column address and read command | READ | H | H | L | H | L | H | V | V | L | V |
| Read with auto precharge | READA | H | H | L | H | L | H | V | V | H | V |
| Column address and write command | WRIT | H | H | L | H | L | L | V | V | L | V |
| Write with auto precharge | WRITA | H | H | L | H | L | L | V | V | H | V |
| Row address strobe and bank active | ACT | H | H | L | L | H | H | V | V | V | V |
| Precharge select bank | PRE | H | H | L | L | H | L | V | V | L | X |
| Precharge all bank | PALL | H | H | L | L | H | L | X | X | H | X |
| Refresh | REF | H | H | L | L | L | H | X | X | X | X |
| | SELF | H | L | L | L | L | H | X | X | X | X |
| Mode register set | MRS | H | H | L | L | L | L | L | L | L | V |
| | EMRS | H | H | L | L | L | L | H | L | L | V |

Note :

1. H : VIH , L : VIL , X : Don't care , V : Valid address input
2. The CKE level must be kept for 1 CK cycle at least.

Ignore command [DESL]

When CS# is high at the cross point of the CK rising edge and the CK# falling edge, all input signals are neglected and internal state is held.

No operation [NOP]

As long as this command is input at the cross point of the CK rising edge and the CK# falling edge, address and data input are neglected and internal state is held.

Burst stop command [BST]

This command stops a current burst operation.

Column address strobe and read command [READ]

This command starts a read operation. The start address of the burst read is determined by the column address (See Table 2.1) and the bank select address. After the completion of the read operation, all output buffers become high-Z.

Read with auto precharge [READA]

This command starts a read operation. After completion of the read operation, precharge is automatically executed.

Column address strobe and write command [WRIT]

This command starts a write operation. The start address of the burst write is determined by the column address (See Table 2.1) and the bank select address.

Write with auto precharge [WRITA]

This command starts a write operation. After completion of the write operation, precharge is automatically executed.

Row address strobe and bank activate [ACT]

This command activates the bank that is selected by BA0 and BA1 (See Table 2.2) and determines the row address (See Table 2.1).

Precharge selected bank [PRE]

This command starts precharge operation for the bank selected by BA0 and BA1. (See Table 2.2)

Precharge all banks [PALL]

This command starts a precharge operation for all banks.

Refresh [REF/SELF]

This command starts a refresh operation. There are two types of refresh operation, one is auto-refresh, and another is self-refresh. For details, refer to the CKE truth table section.

Mode register set/Extended mode register set [MRS/EMRS]

The DDR Mobile RAM has the two mode registers, the mode register and the extended mode register, to define how it works. The both mode registers are set through the address pins in the mode register set cycle. For details, refer to "Mode register and extended mode register set"

3.3 Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR Mobile RAM.

Table 3.2 Command Truth Table

| Current state | CS# | RAS# | CAS# | WE# | Address | Command | Operation |
|--------------------------------------|-----|------|------|-----|-----------|------------|---------------------------------------|
| Pre-charging* ¹ | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | ILLEGAL* ¹¹ |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL* ¹¹ |
| | L | H | L | L | | WRIT/WRITA | ILLEGAL* ¹¹ |
| | L | L | H | H | | ACT | ILLEGAL* ¹¹ |
| | L | L | H | L | | PRE,PALL | NOP |
| | L | L | L | X | X | | ILLEGAL |
| Idle* ² | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | NOP |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL* ¹¹ |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL* ¹¹ |
| | L | L | H | H | BA,RA | ACT | Activating |
| | L | L | H | L | BA,A10 | PRE,PALL | NOP |
| | L | L | L | H | X | REF,SELF | Refresh / Self-refresh* ¹² |
| | L | L | L | L | MODE | MRS | Mode register set* ¹² |
| Refresh (auto refresh)* ³ | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | H | H | H | L | X | BST | ILLEGAL |
| | L | H | L | X | X | | ILLEGAL |
| | L | L | X | X | X | | ILLEGAL |

| Current state | CS# | RAS# | CAS# | WE# | Address | Command | Operation |
|--------------------------|-----|------|------|-----|-----------|------------|---|
| Activating* ⁴ | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | ILLEGAL* ¹¹ |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL* ¹¹ |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL* ¹¹ |
| | L | L | H | H | BA,RA | ACT | ILLEGAL* ¹¹ |
| | L | L | H | L | BA,A10 | PRE,PALL | ILLEGAL* ¹¹ |
| | L | L | L | X | X | | ILLEGAL |
| Active* ⁵ | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | NOP |
| | L | H | L | H | BA,CA,A10 | READ/READA | Starting read operation |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | Starting read operation |
| | L | L | H | H | BA,RA | ACT | ILLEGAL* ¹¹ |
| | L | L | H | L | BA,A10 | PRE,PALL | Pre-charge |
| | L | L | L | X | X | | ILLEGAL |
| Read* ⁶ | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | Burst stop |
| | L | H | L | H | BA,CA,A10 | READ/READA | Interrupting burst read operation to start new read |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL* ¹³ |
| | L | L | H | H | BA,RA | ACT | ILLEGAL* ¹¹ |
| | L | L | H | L | BA,A10 | PRE,PALL | Interrupting burst read operation to start pre-charge |
| | L | L | L | X | X | | ILLEGAL |

| Current state | CS# | RAS# | CAS# | WE# | Address | Command | Operation |
|---|-----|------|------|-----|-----------|------------|---|
| Read with auto pre-charge ^{*7} | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ^{*11} |
| | L | L | H | L | BA,A10 | PRE,PALL | ILLEGAL ^{*11} |
| | L | L | L | X | X | | ILLEGAL |
| Write ^{*8} | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | Burst stop |
| | L | H | L | H | BA,CA,A10 | READ/READA | Interrupting burst write operation to start read operation |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | Interrupting burst write operation to start new write operation |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ^{*11} |
| | L | L | H | L | BA,A10 | PRE,PALL | Interrupting write operation to start pre-charge |
| | L | L | L | X | X | | ILLEGAL |
| Write recovering ^{*9} | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | Starting read operation |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | Starting new write operation |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ^{*11} |
| | L | L | H | L | BA,A10 | PRE,PALL | ILLEGAL ^{*11} |
| | L | L | L | X | X | | ILLEGAL |

| Current state | CS# | RAS# | CAS# | WE# | Address | Command | Operation |
|---|-----|------|------|-----|-----------|------------|------------------------|
| Write with auto pre-charge ^{*10} | H | X | X | X | X | DESL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ^{*11} |
| | L | L | H | L | BA,A10 | PRE,PALL | ILLEGAL ^{*11} |
| | L | L | L | X | X | | ILLEGAL |

Note :

1. The DDR Mobile RAM is in "Pre-charging" state for tRP after precharge command is issued.
2. The DDR Mobile RAM reaches "IDLE" state tRP after precharge command is issued.
3. The DDR Mobile RAM is in "Refresh" state for tRFC after auto-refresh command is issued.
4. The DDR Mobile RAM is in "Activating" state for tRCD after ACT command is issued.
5. The DDR Mobile RAM is in "Active" state after "Activating" is completed.
6. The DDR Mobile RAM is in "READ" state until burst data have been output and DQ output circuits are turned off.
7. The DDR Mobile RAM is in "READ with auto precharge" from READA command until burst data has been output and DQ output circuits are turned off.
8. The DDR Mobile RAM is in "WRITE" state from WRIT command to the last burst data are input.
9. The DDR Mobile RAM is in "Write recovering" for tWR after the last data are input.
10. The DDR Mobile RAM is in "Write with auto precharge" until tWR after the last data has been input.
11. This command may be issued for other banks, depending on the state of the banks.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. Before executing a write command to stop the preceding burst read operation, BST command must be issued.
14. H : VIH , L : VIL , X : **Don't care**

3.4 CKE Truth Table

Table 3.3 CKE Truth Table

| Current state | Command | CKE | | CS# | RAS# | CAS# | WE# | Address | Note |
|-----------------|-------------------------------|-----|---|-----|------|------|-----|---------|------|
| | | n-1 | n | | | | | | |
| Idle | Auto refresh command (REF) | H | H | L | L | L | H | X | 2 |
| Idle | Self refresh entry (SELF) | H | L | L | L | L | H | X | 2 |
| Active / Idle | Power down entry (PDEN) | H | L | L | H | H | H | X | |
| | | H | L | H | X | X | X | X | |
| Idle | Deep power down entry (DPDEN) | H | L | L | H | H | L | X | 2 |
| Self refresh | Self refresh exit (SELFX) | L | H | L | H | H | H | X | |
| | | L | H | H | X | X | X | X | |
| Power down | Power down exit (PDEX) | L | H | L | H | H | H | X | |
| | | L | H | H | X | X | X | X | |
| Deep power down | Power down exit (DPDEX) | L | H | X | X | X | X | X | |

Note :

1. H : VIH , L : VIL , X : Don't care.
2. All the banks must be in IDLE and no bursts in progress before executing this command.
3. The CKE level must be kept for 1 CK cycle at least.

Auto-refresh command [REF]

This command executes auto-refresh. The bank and the ROW addresses to be refreshed are internally determined by the internal refresh controller. The output buffer becomes high-Z after auto-refresh start. Precharge has been completed automatically after the auto-refresh. The ACT or MRS command can be issued tRFC after the last auto-refresh command.

The average refresh interval is 7.8 μ s. To allow for improved efficiency in scheduling, some flexibility in the absolute refresh interval is provided. A maximum of eight auto-refresh commands can be posted to the DDR Mobile RAM or the maximum absolute interval between any auto-refresh command and the next auto-refresh command is 8 \times tREFI.

Self-refresh entry [SELF]

This command starts self-refresh. The self-refresh operation continues as long as CKE is held low. During the self-refresh operation, all ROW addresses are repeated refreshing by the internal refresh controller. A self-refresh is terminated by a self-refresh exit command.

Power-down mode entry [PDEN]

tPDEN (= 2 clocks) after the cycle when [PDEN] is issued, the DDR Mobile RAM enters into power-down mode. In power-down mode, power consumption is suppressed by deactivating the input initial circuit. Power-down mode continues while CKE is held low. No internal refresh operation occurs during the power-down mode.

Deep power-down entry [DPDEN]

After the command execution, deep power-down mode continues while CKE remains low. Before executing deep power-down, all banks must be pre-charged or in idle state.

Self-refresh exit [SELFX]

This command is executed to exit from self-refresh mode. tSREX after [SELFX], the device will be into idle state.

Power-down exit [PDEX]

The DDR Mobile RAM can exit from power-down mode tPDEX (1 cycle min.) after the cycle when [PDEX] is issued.

Deep power-down exit [DPDEX]

As CKE goes high in the deep power-down mode, the DDR Mobile RAM exit from the deep power-down mode through deep power-down exiting sequence.

4. DEVICE OPERATION

4.1 Initialization

The DDR Mobile RAM is initialized in the power-on sequence according to the following.

1. Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also assert and hold Clock Enable (CKE) to a LV-CMOS logic high level.
2. Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.
3. There must be at least **200µs** of valid clocks before any command may be given to the DRAM. During this time NOP or deselect (DESL) commands must be issued on the command bus.
4. Issue a precharge all command.
5. Provide NOPs or DESL commands for at least tRP time.
6. Issue an auto-refresh command followed by NOPs or DESL command for at least tRFC time. Issue the second auto-refresh command followed by NOPs or DESL command for at least tRFC time. Note as part of the initialization sequence there must be two auto-refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.
7. Using the MRS command, load the base mode register. Set the desired operating modes.
8. Provide NOPs or DESL commands for at least tMRD time.
9. Using the MRS command, program the extended mode register for the desired operating modes.
10. Provide NOP or DESL commands for at least tMRD time.
11. The DRAM has been properly initialized and is ready for any valid command.

4.2 Mode Register and Extended Mode Register Set

There are two mode registers, the mode register and the extended mode register so as to define the operating mode. Parameters are set to both through the A0 to the A12 and BA0 and BA1 pins by the mode register set command [MRS] or the extended mode register set command [EMRS]. The mode register and the extended mode register are set by inputting signal via the A0 to the A12 and BA0 and BA1 pins during mode register set cycles.

BA0 and BA1 determine which one of the mode register or the extended mode register are set. Prior to a read or a write operation, the mode register must be set.

4.2.1 Mode Register

The mode register has four fields;

| | |
|--------------|------------------|
| Reserved | : A12 through A7 |
| CAS latency | : A6 through A4 |
| Wrap type | : A3 |
| Burst length | : A2 through A0 |

Following mode register programming, no command can be issued before at least 2 clocks have elapsed.

CAS# Latency

CAS# latency must be set to 3.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become high-Z. The burst length is programmable as 2, 4, 8 and 16.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either "Sequential" or "Interleave". "Burst Operation" shows the addressing sequence for each burst length for each wrap type.

4.2.2 Extended Mode Register

The extended mode register has three fields;

| | |
|----------------------------|--------------------------|
| Reserved | : A12 through A7, A4, A3 |
| Driver Strength | : A6 through A5 |
| Partial Array Self-Refresh | : A2 through A0 |

Following extended mode register programming, no command can be issued before at least 2 clocks have elapsed.

Driver Strength

By setting specific parameter on A6 and A5, driving capability of data output drivers is selected.

Auto Temperature Compensated Self-Refresh (ATCSR)

The DDR Mobile RAM automatically changes the self-refresh cycle by on die temperature sensor. No extended mode register program is required. Manual TCSR (Temperature Compensated Self-Refresh) is not implemented.

Partial Array Self-Refresh

Memory array size to be refreshed during self-refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self-refresh.

4.3 Power Down & Deep Power Down

4.3.1 Deep Power Down Exit Sequence

In order to exit from the deep power-down mode and enter into the idle mode, the following sequence is needed, which is similar to the power-on sequence.

1. A **200µs** or longer pause must precede any command other than ignore command (DESL).
2. After the pause, all banks must be pre-charged using the precharge command (the precharge all banks command is convenient).
3. Once the precharge is completed and the minimum tRP is satisfied, two or more Auto-refresh must be performed.
4. Both the mode register and the extended mode register must be programmed. After the mode register set cycle or the extended mode register set cycle, tMRD (2 clocks minimum) pause must be satisfied.

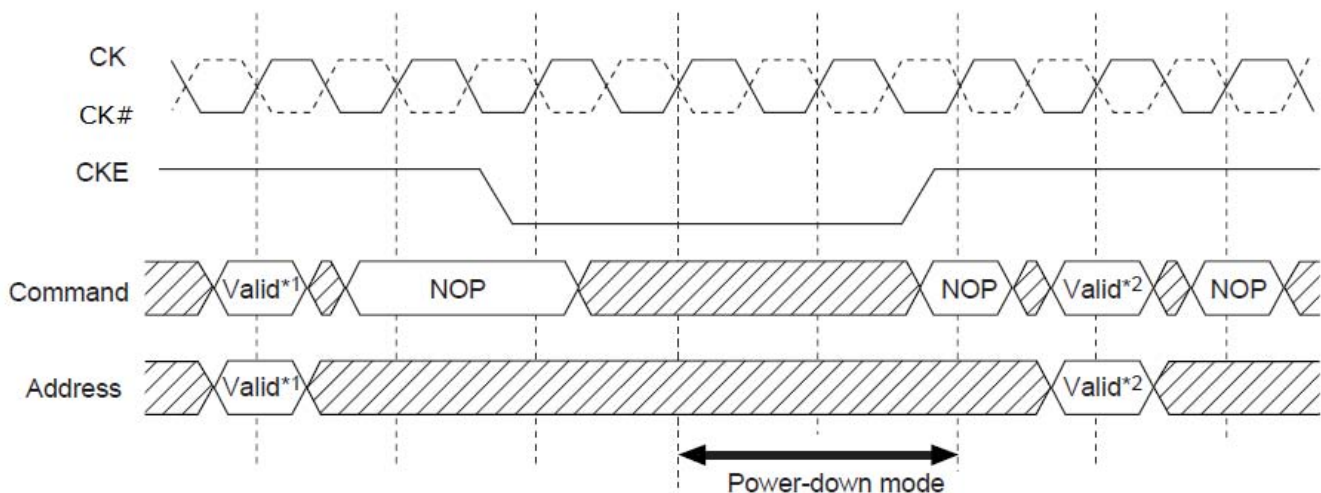
Remarks:

1. The sequence of Auto-refresh, mode register programming and extended mode register programming above may be transposed.
2. CKE must be held high.

4.3.2 Power Down Mode and CKE Control

DDR Mobile RAM will be into power-down mode at the second CK rising edge after CKE to be low level with NOP or DESL command at first CK rising edge after CKE signal to be low.

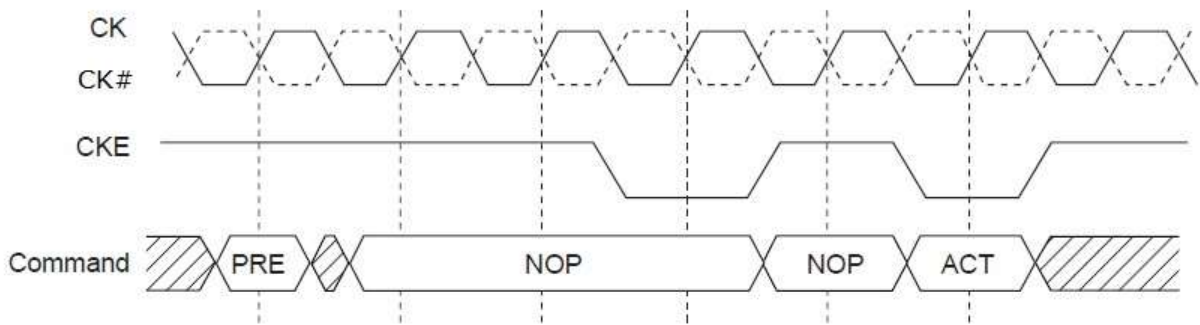
Figure 4.1 Power Down Entry and Exit



Notes:

1. Valid*1 can be either Activate command or Precharge command, When Valid*1 is Activate command, power-down mode will be active power-down mode, while it will be precharge power down mode, if Valid*1 will be Precharge command.
2. Valid*2 can be any command as long as all of specified AC parameters are satisfied.
 However, if the CKE has one clock cycle high and on clock cycle low just as below, even DDR Mobile RAM will not enter power-down mode, this command flow does not hurt any data and can be done.

Figure 4.2 CKE Control



Note: Assume PRE and ACT command is closing and activating same bank.

4.5 Burst Operation

The burst type (BT) and the first three bits of the column address determine the order of a data out.

Table 4.1 Burst length = 2

| Starting Address | | Addressing (decimal) | |
|------------------|--|----------------------|------------|
| A0 | | Sequence | Interleave |
| 0 | | 0, 1 | 0, 1 |
| 1 | | 1, 0 | 1, 0 |

Table 4.2 Burst length = 4

| Starting Address | | Addressing (decimal) | |
|------------------|----|----------------------|------------|
| A1 | A0 | Sequence | Interleave |
| 0 | 0 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| 0 | 1 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| 1 | 0 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| 1 | 1 | 3, 0, 1, 2 | 3, 2, 1, 0 |

Table 4.3 Burst length = 8

| Starting Address | | | Addressing (decimal) | |
|------------------|----|----|------------------------|------------------------|
| A2 | A1 | A0 | Sequence | Interleave |
| 0 | 0 | 0 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| 0 | 0 | 1 | 1, 2, 3, 4, 5, 6, 7, 0 | 1, 0, 3, 2, 5, 4, 7, 6 |
| 0 | 1 | 0 | 2, 3, 4, 5, 6, 7, 0, 1 | 2, 3, 0, 1, 6, 7, 4, 5 |
| 0 | 1 | 1 | 3, 4, 5, 6, 7, 0, 1, 2 | 3, 2, 1, 0, 7, 6, 5, 4 |
| 1 | 0 | 0 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| 1 | 0 | 1 | 5, 6, 7, 0, 1, 2, 3, 4 | 5, 4, 7, 6, 1, 0, 3, 2 |
| 1 | 1 | 0 | 6, 7, 0, 1, 2, 3, 4, 5 | 6, 7, 4, 5, 2, 3, 0, 1 |
| 1 | 1 | 1 | 7, 0, 1, 2, 3, 4, 5, 6 | 7, 6, 5, 4, 3, 2, 1, 0 |

Table 4.4 Burst length = 16

| Starting Address | | | | Addressing (decimal) | |
|------------------|----|----|----|---------------------------------------|---------------------------------------|
| A3 | A2 | A1 | A0 | Sequence | Interleave |
| 0 | 0 | 0 | 0 | 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 | 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 |
| 0 | 0 | 0 | 1 | 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,0 | 1,0,3,2,5,4,7,6,9,8,11,10,13,12,15,14 |
| 0 | 0 | 1 | 0 | 2,3,4,5,6,7,8,9,10,11,12,13,14,15,0,1 | 2,3,0,1,6,7,4,5,10,11,8,9,14,15,12,13 |
| 0- | 0 | 1 | 1 | 3,4,5,6,7,8,9,10,11,12,13,14,15,0,1,2 | 3,2,1,0,7,6,5,4,11,10,9,8,15,14,13,12 |
| 0 | 1 | 0 | 0 | 4,5,6,7,8,9,10,11,12,13,14,15,0,1,2,3 | 4,5,6,7,0,1,2,3,12,13,14,15,8,9,10,11 |
| 0 | 1 | 0 | 1 | 5,6,7,8,9,10,11,12,13,14,15,0,1,2,3,4 | 5,4,7,6,1,0,3,2,13,12,15,14,9,8,11,10 |
| 0 | 1 | 1 | 0 | 6,7,8,9,10,11,12,13,14,15,0,1,2,3,4,5 | 6,7,4,5,2,3,0,1,14,15,12,13,10,11,8,9 |
| 0 | 1 | 1 | 1 | 7,8,9,10,11,12,13,14,15,0,1,2,3,4,5,6 | 7,6,5,4,3,2,1,0,15,14,13,12,11,10,9,8 |
| 1 | 0 | 0 | 0 | 8,9,10,11,12,13,14,15,0,1,2,3,4,5,6,7 | 8,9,10,11,12,13,14,15,0,1,2,3,4,5,6,7 |
| 1 | 0 | 0 | 1 | 9,10,11,12,13,14,15,0,1,2,3,4,5,6,7,8 | 9,8,11,10,13,12,15,14,1,0,3,2,5,4,7,6 |
| 1 | 0 | 1 | 0 | 10,11,12,13,14,15,0,1,2,3,4,5,6,7,8,9 | 10,11,8,9,14,15,12,13,2,3,0,1,6,7,4,5 |
| 1 | 0 | 1 | 1 | 11,12,13,14,15,0,1,2,3,4,5,6,7,8,9,10 | 11,10,9,8,15,14,13,12,3,2,1,0,7,6,5,4 |
| 1 | 1 | 0 | 0 | 12,13,14,15,0,1,2,3,4,5,6,7,8,9,10,11 | 12,13,14,15,8,9,10,11,4,5,6,7,0,1,2,3 |
| 1 | 1 | 0 | 1 | 13,14,15,0,1,2,3,4,5,6,7,8,9,10,11,12 | 13,12,15,14,9,8,11,10,5,4,7,6,1,0,3,2 |
| 1 | 1 | 1 | 0 | 14,15,0,1,2,3,4,5,6,7,8,9,10,11,12,13 | 14,15,12,13,10,11,8,9,6,7,4,5,2,3,0,1 |
| 1 | 1 | 1 | 1 | 15,0,1,2,3,4,5,6,7,8,9,10,11,12,13,14 | 15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0 |

4.6 Read / Write Operation

Bank Active

A read or a write operation begins with the bank active command [ACT]. The bank active command determines a bank address and a row address. For the bank and the row, a read or a write command can be issued t_{RCD} after the ACT is issued.

Read operation

The burst length (BL), the CAS# latency (CL) and the burst type (BT) of the mode register are referred when a read command is issued. The burst length (BL) determines the length of a sequential output data by the read command that can be set to 2, 4, 8 or 16. The starting address of the burst read is defined by the column address, the bank select address (See 2.4 Pin Description) in the cycle when the read command is latched. The data output timing is characterized by CL and t_{AC} . The read burst start $(CL-1) \times t_{CK} + t_{AC}$ (ns) after the clock rising edge where the read command is latched. The DDR Mobile RAM outputs the data strobe through DQS pins simultaneously with data. t_{RPRE} prior to the first rising edge of the data strobe, the DQS pins are driven low from high-Z state. This low period of DQS is referred as read preamble. The burst data are output coincidentally at both the rising and falling edge of the data strobe. The DQ pins become high-Z in the next cycle after the burst read operation completed. t_{RPST} from the last falling edge of the data strobe, the DQS pins become high-Z. This low period of DQS is referred as read postamble.

Figure 4.4 Read Operation (Burst Length)

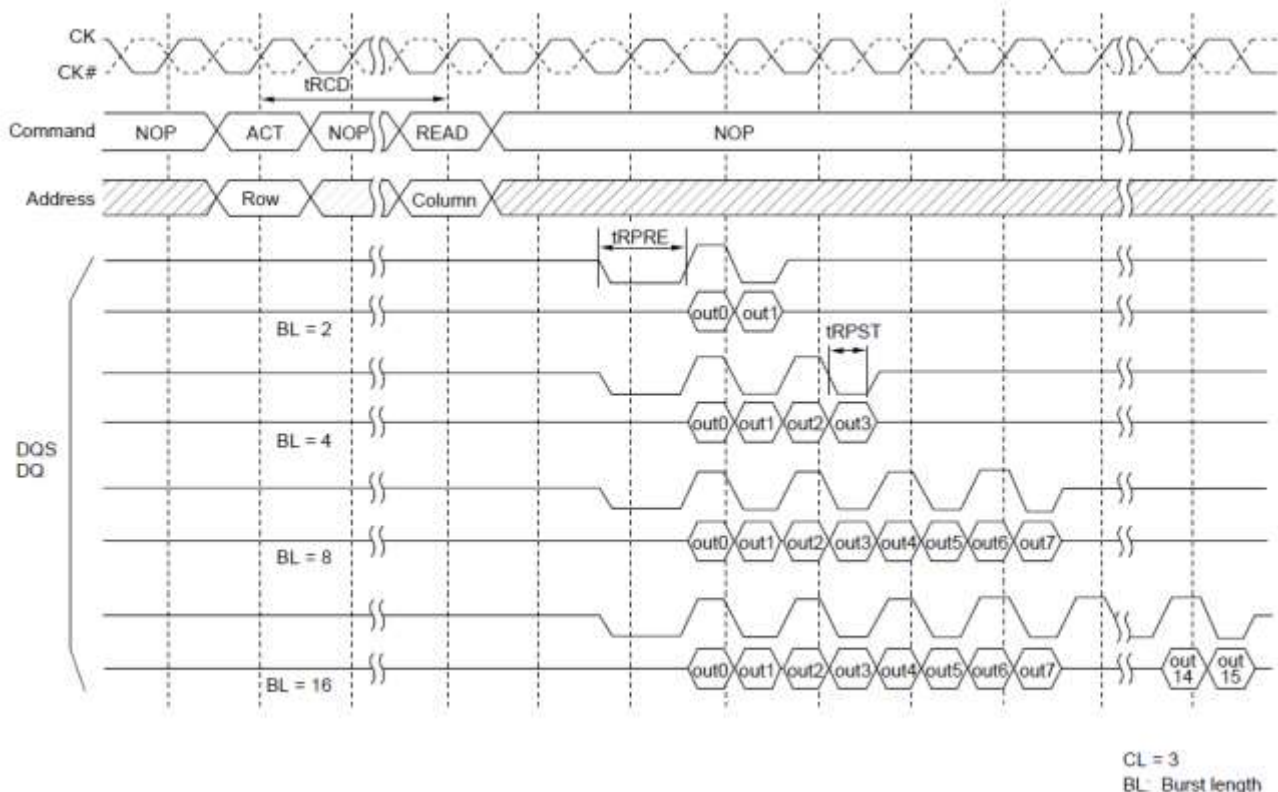
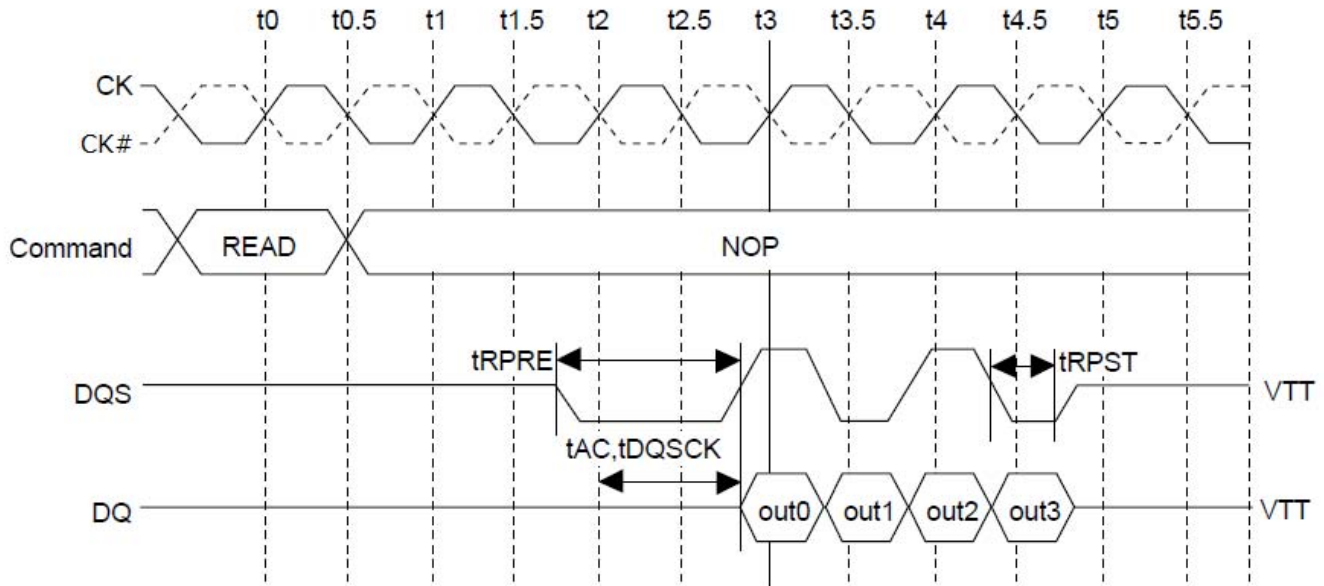


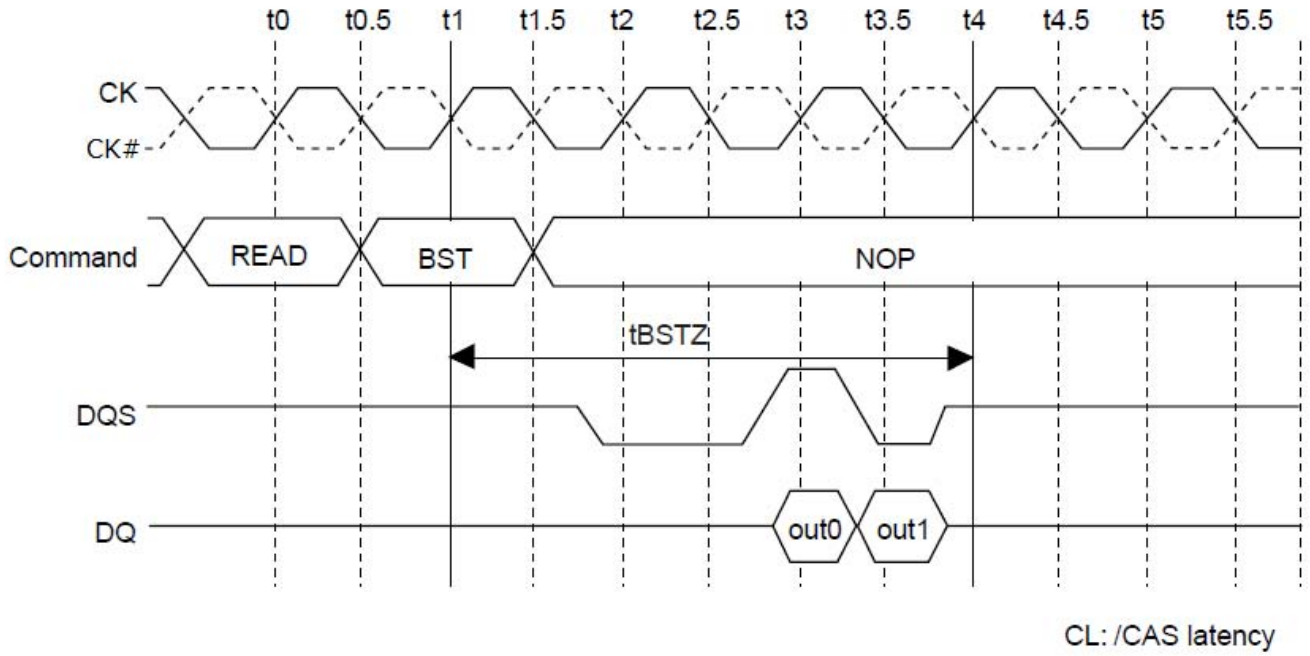
Figure 4.4 Read Operation (CAS# Length)

Burst stop command during burst operation

The burst stop (BST) command stops the burst read and sets all output buffers to high-Z. t_{BSTZ} (= CL) cycles after a BST command issued, all DQ and DQS pins become high-Z.

The BST command is also supported for the burst write operation. No data will be written in subsequent cycles.

Note that bank address is not referred when this command is executed.

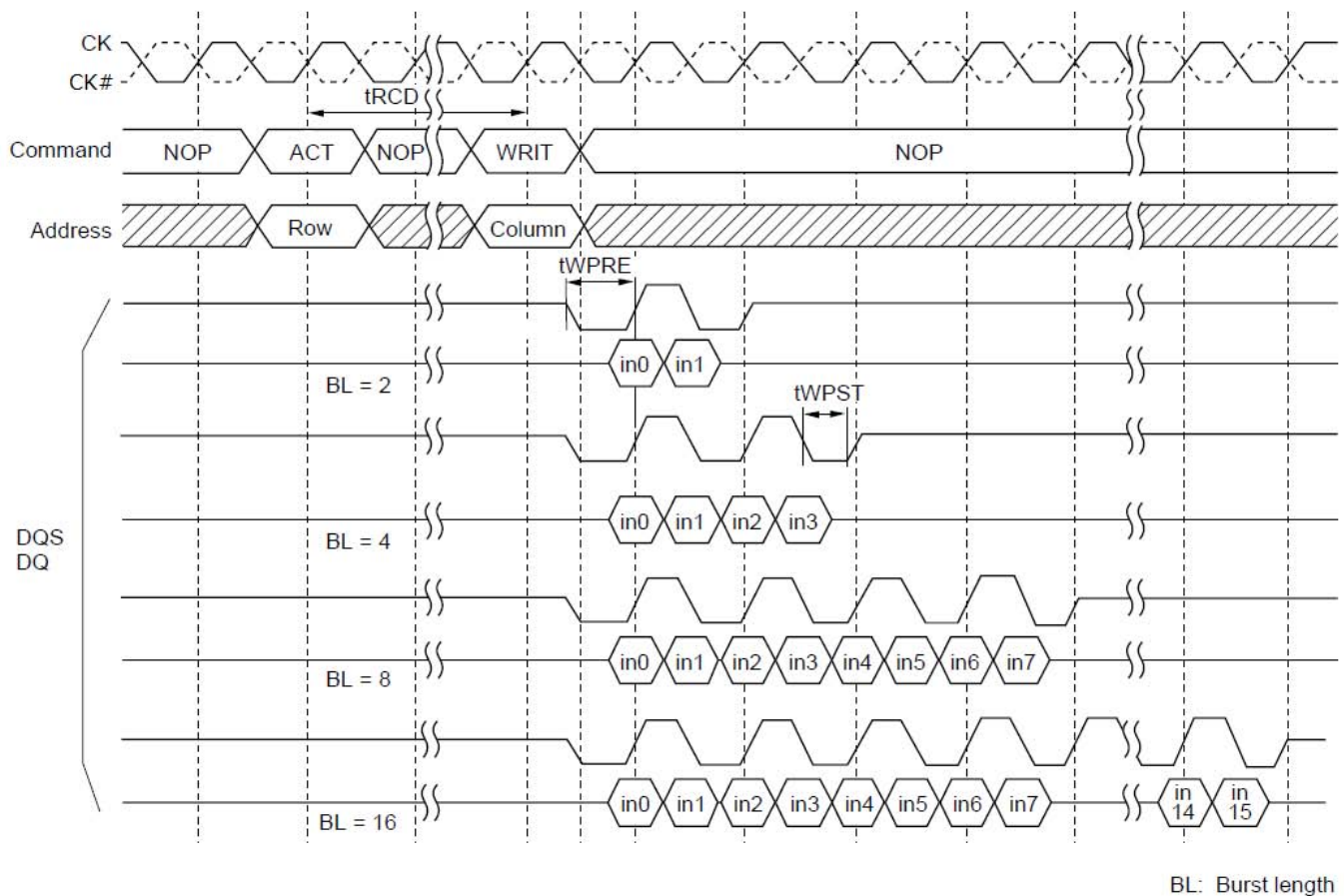
Figure 4.5 Burst Stop during a Read Operation



Write operation

The burst length (BL) and the burst type (BT) of the mode register are referred when a write command is issued. The burst length (BL) determines the length of a sequential data input by the write command that can be set to 2, 4, 8 or 16. The latency from write command to data input is fixed to 1. The starting address of the burst write is defined by the column address, the bank select address (See 2.4 Pin Description) in the cycle when the write command is issued. DQS should be input as the strobe for the input-data and DM as well during burst operation. t_{WPRE} prior to the first rising edge of DQS, DQS must be set to low. t_{WPST} after the last falling edge of DQS, the DQS pins can be changed to high-Z. The leading low period of DQS is referred as write preamble. The last low period of DQS is referred as write post-amble.

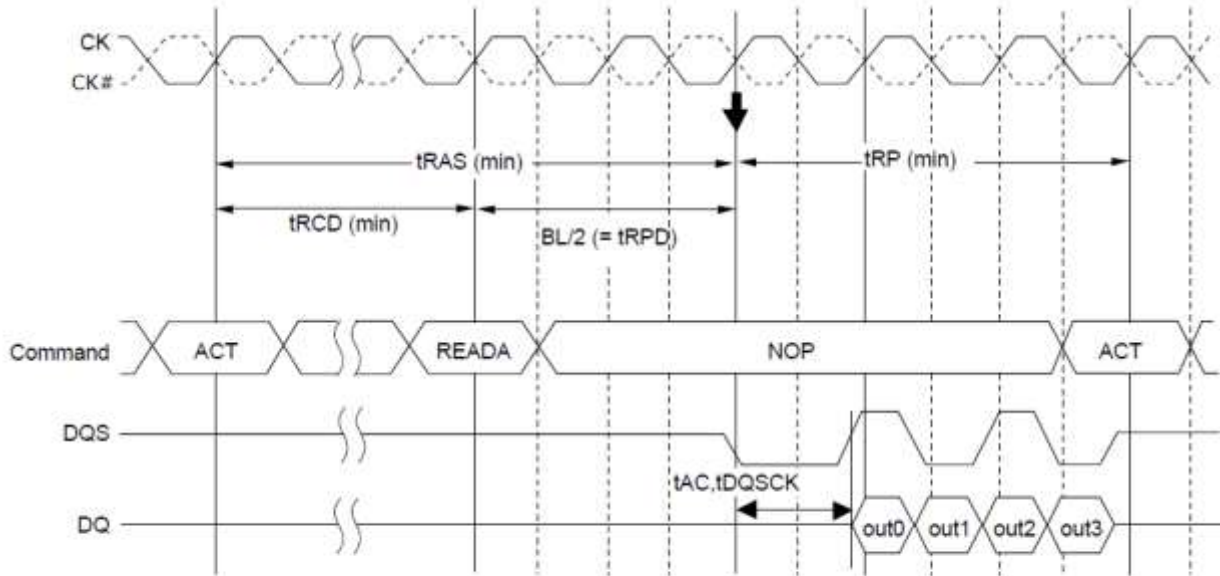
Figure 4.6 Write Operation



Read with auto precharge

The precharge is automatically performed after completing a read operation. The precharge starts BL/2 (= tRPD) clocks after READA command input. tRAS lock out mechanism for READA allows a read command with auto precharge to be issued to a bank that has been activated (opened) but has not yet satisfied the tRAS (min) specification. A column command to the other active bank can be issued the next cycle after the last data output.

Read with auto precharge command does not limit row commands execution for other bank.

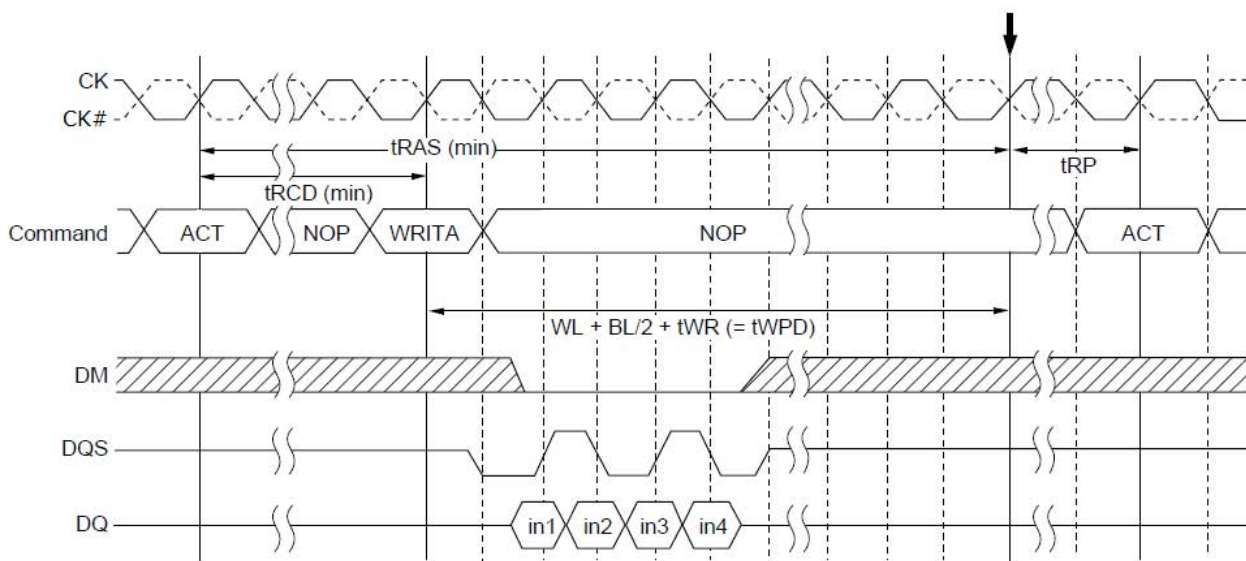
Figure 4.7 Read with auto precharge


Note: Internal auto-precharge starts at the timing indicated by "↓".

Write with auto precharge

The precharge is automatically performed after completing a burst write operation. The precharge operation is started Write latency (WL) + BL/2 + tWR (= tWPD) clocks after WRITA command issued. A column command to the other banks can be issued the next cycle after the internal precharge command issued.

Write with auto precharge command does not limit row commands execution for other bank.

Figure 4.8 Burst Write (BL = 4)


Note: Internal auto-precharge starts at the timing indicated by "↓".

BL = 4

The Concurrent Auto Precharge

The DDR Mobile RAM supports the concurrent auto precharge feature, a read with auto precharge or a write with auto precharge, can be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided.) The minimum delay from a read or write command with auto precharge, to a command to a different bank, is summarized below.

Table 4.5 The minimum delay from a read or write command with auto precharge

| From Command | To command (different bank, non-interrupting command) | Minimum delay (Concurrent AP supported) | Unit |
|---------------------------|---|---|------|
| Read with Auto Precharge | Read or Read w/AP | $BL / 2$ | tCK |
| | Write or Write w/AP | $CL \text{ (rounded up)} + (BL/2)$ | |
| | Precharge or Activate | 1 | |
| Write with Auto Precharge | Read or Read w/AP | $1 + (BL/2) + tWTR$ | |
| | Write or Write w/AP | $BL / 2$ | |
| | Precharge or Activate | 1 | |

4.7 Command Intervals

4.7.1 Read command to the consecutive Read command Interval

Table 4.6 A Read command to the consecutive Read command Interval

| | Destination row of the consecutive read command | | | Operation |
|---|---|-------------|--------|---|
| | Bank address | Row address | State | |
| 1 | Same | Same | ACTIVE | The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation. |
| 2 | Same | Different | - | Precharge the bank to interrupt the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section. |
| 3 | Different | Any | ACTIVE | The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation. |
| | | | IDLE | Precharge the bank without interrupting the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. |

Figure 4.9 READ to READ Command Interval (same ROW address in the same bank)

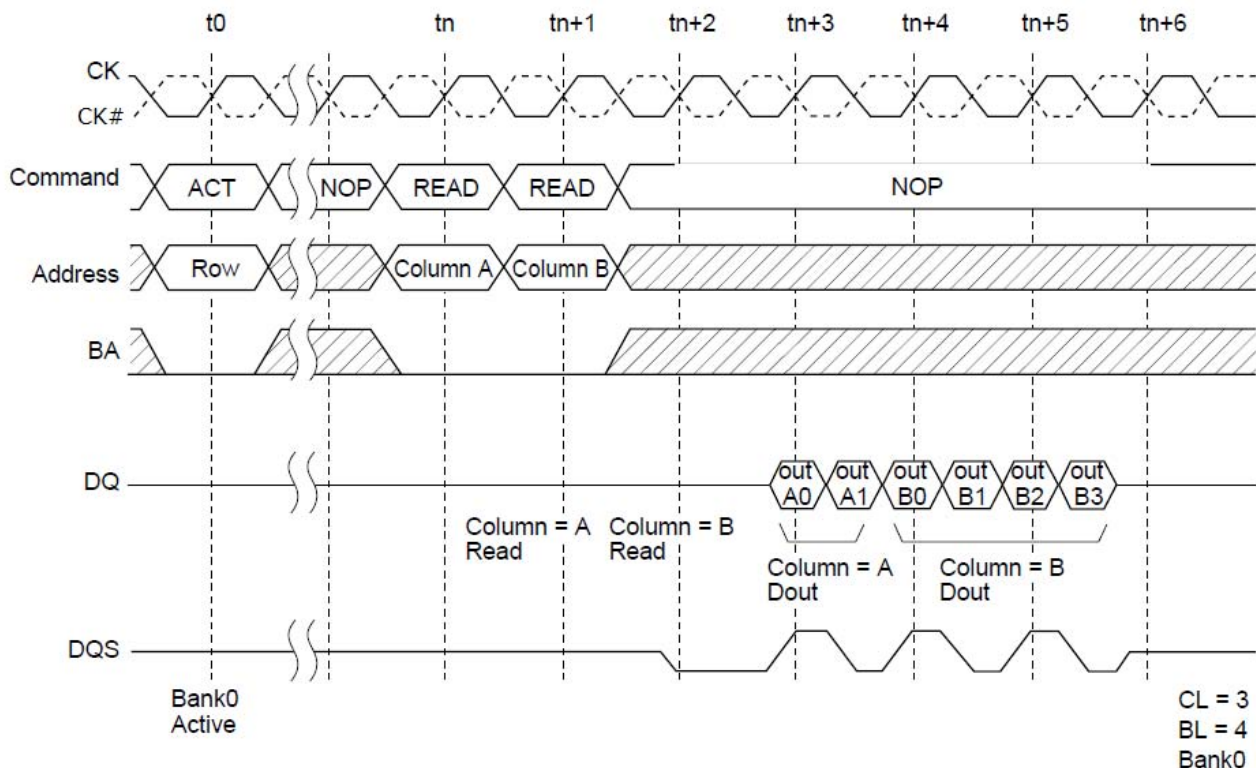
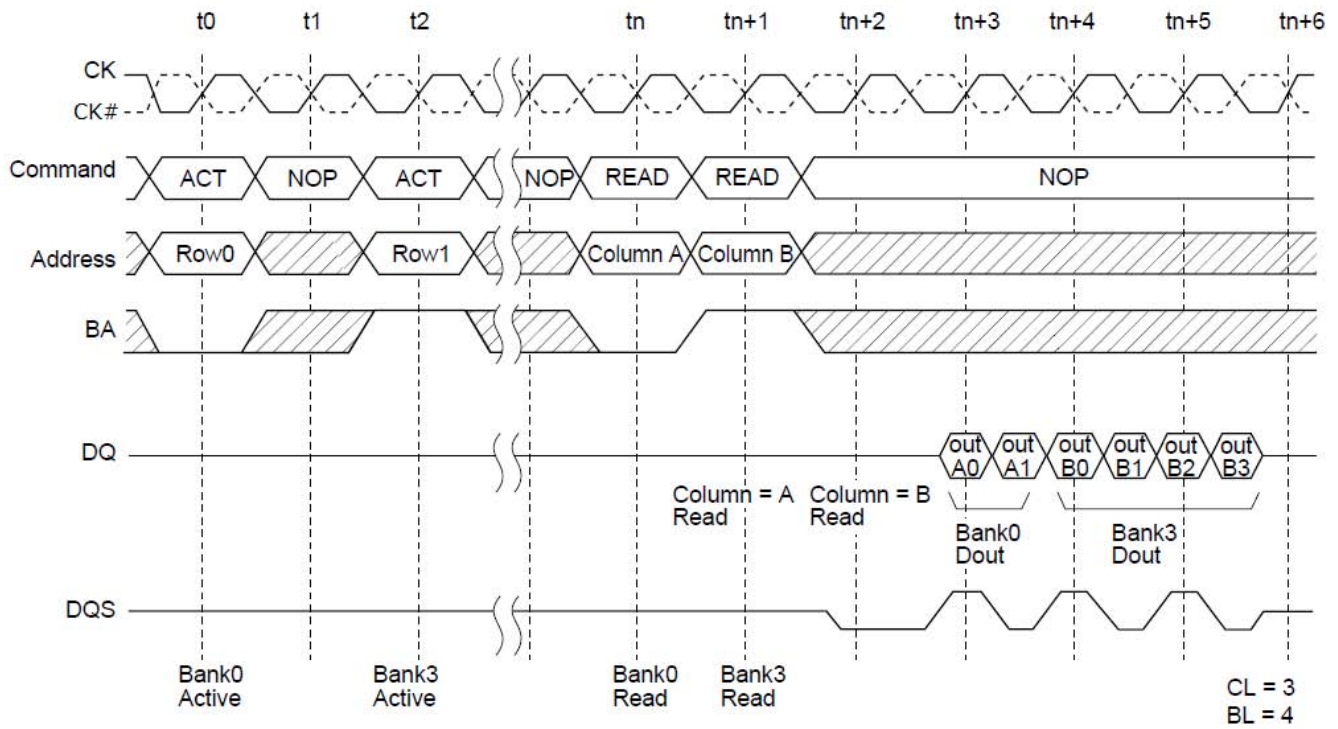


Figure 4.10 READ to READ Command Interval (different bank)



4.7.2 A Write command to the consecutive Write command Interval
Table 4.7 A Write command to the consecutive Write command Interval

| | Destination row of the consecutive write command | | | Operation |
|---|--|-------------|--------|--|
| | Bank address | Row address | State | |
| 1 | Same | Same | ACTIVE | The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation. |
| 2 | Same | Different | - | Precharge the bank to interrupt the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued. See ' A write command to the consecutive precharge interval' section. |
| 3 | Different | Any | ACTIVE | The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation. |
| | | | IDLE | Precharge the bank without interrupting the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued. |

Figure 4.11 WRITE to WRITE Command Interval (same ROW address in the same bank)

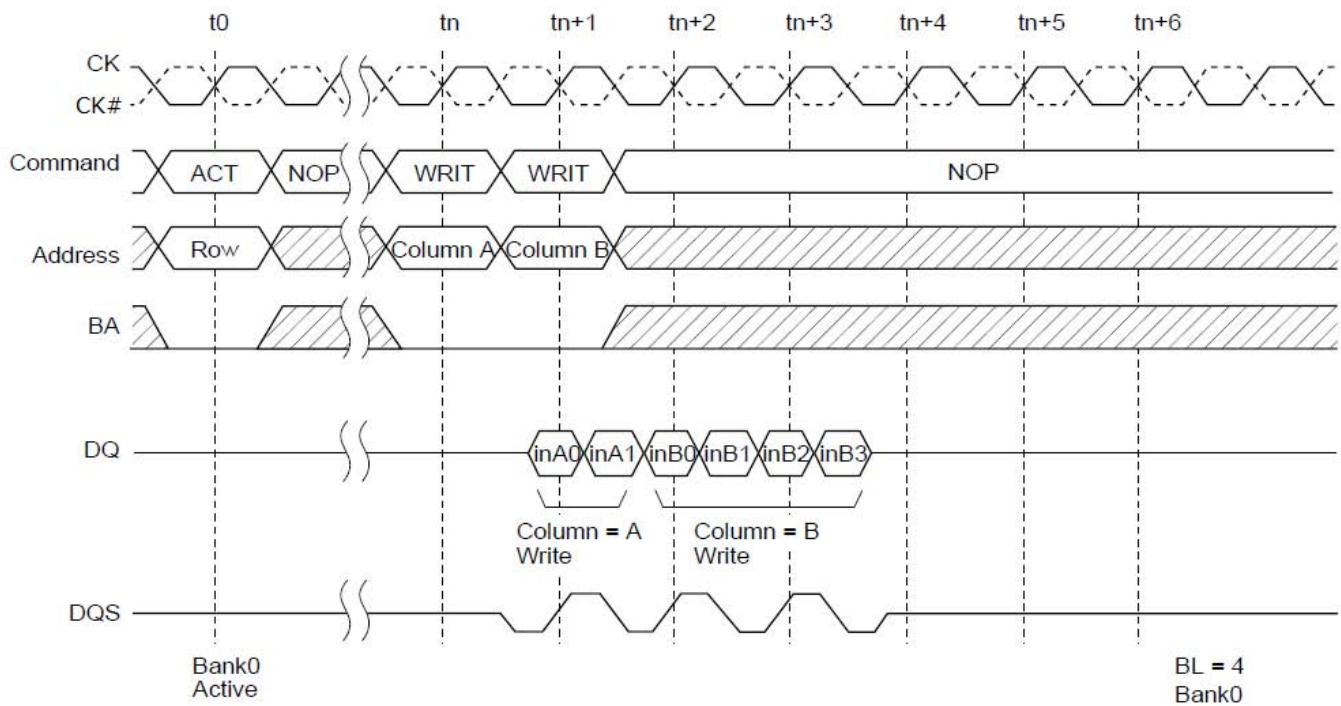
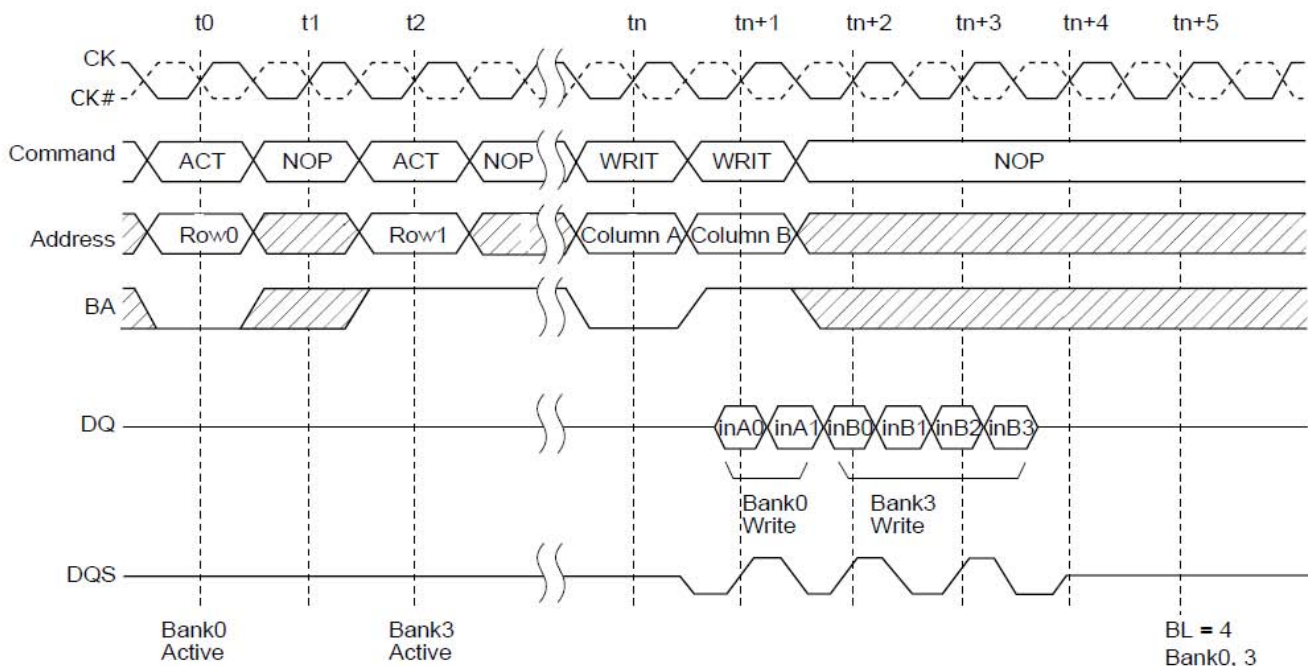


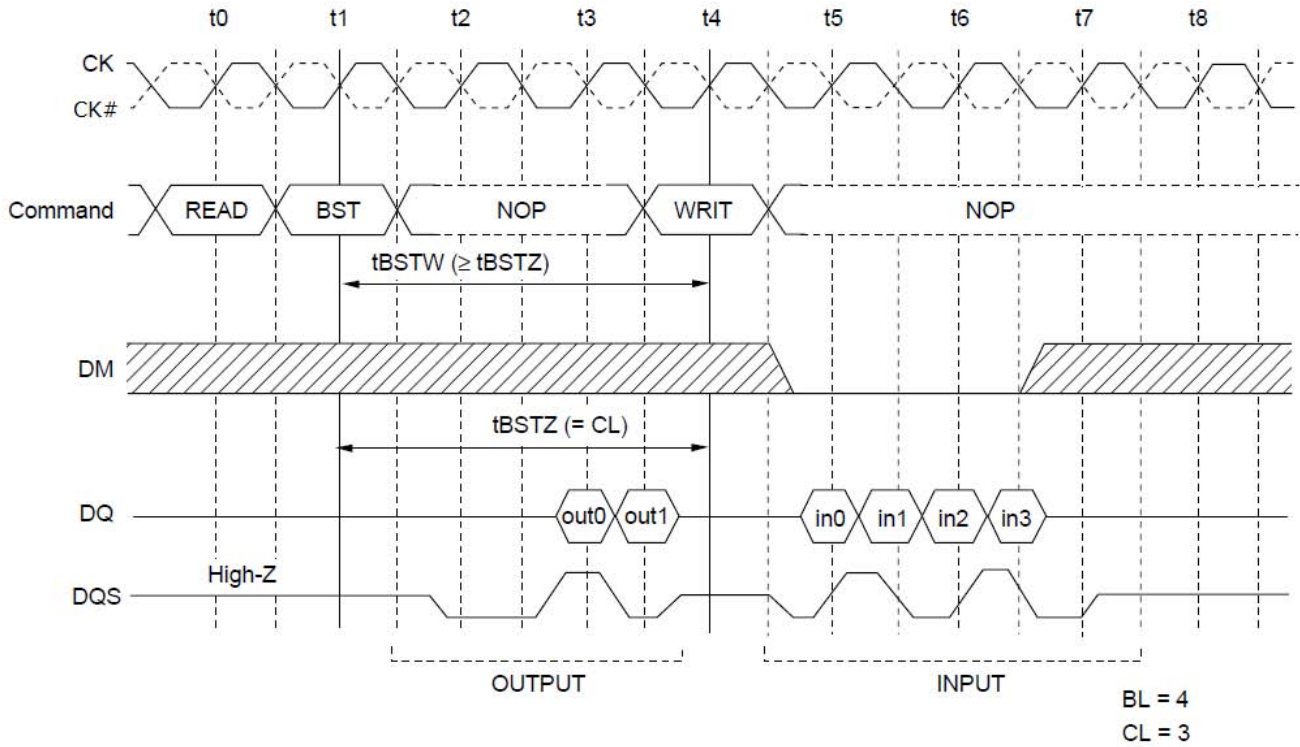
Figure 4.12 WRITE to WRITE Command Interval (different bank)



4.7.3 A Read command to the consecutive Write command interval with BST command
Table 4.8 A Read command to the consecutive Write command interval with BST command

| | Destination row of the consecutive write command | | | Operation |
|---|--|-------------|--------|--|
| | Bank address | Row address | State | |
| 1 | Same | Same | ACTIVE | Issue the BST command. $t_{BSTW} (\geq t_{BSTZ})$ after the BST command, the consecutive write command can be issued. |
| 2 | Same | Different | - | Precharge the bank to interrupt the preceding read operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive write command can be issued. See 'A read command to the consecutive precharge interval' section. |
| 3 | Different | Any | ACTIVE | Issue the BST command. $t_{BSTW} (\geq t_{BSTZ})$ after the BST command, the consecutive write command can be issued. |
| | | | IDLE | Precharge the bank independently of the preceding read operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive write command can be issued. |

Figure 4.13 READ to WRITE Command Interval

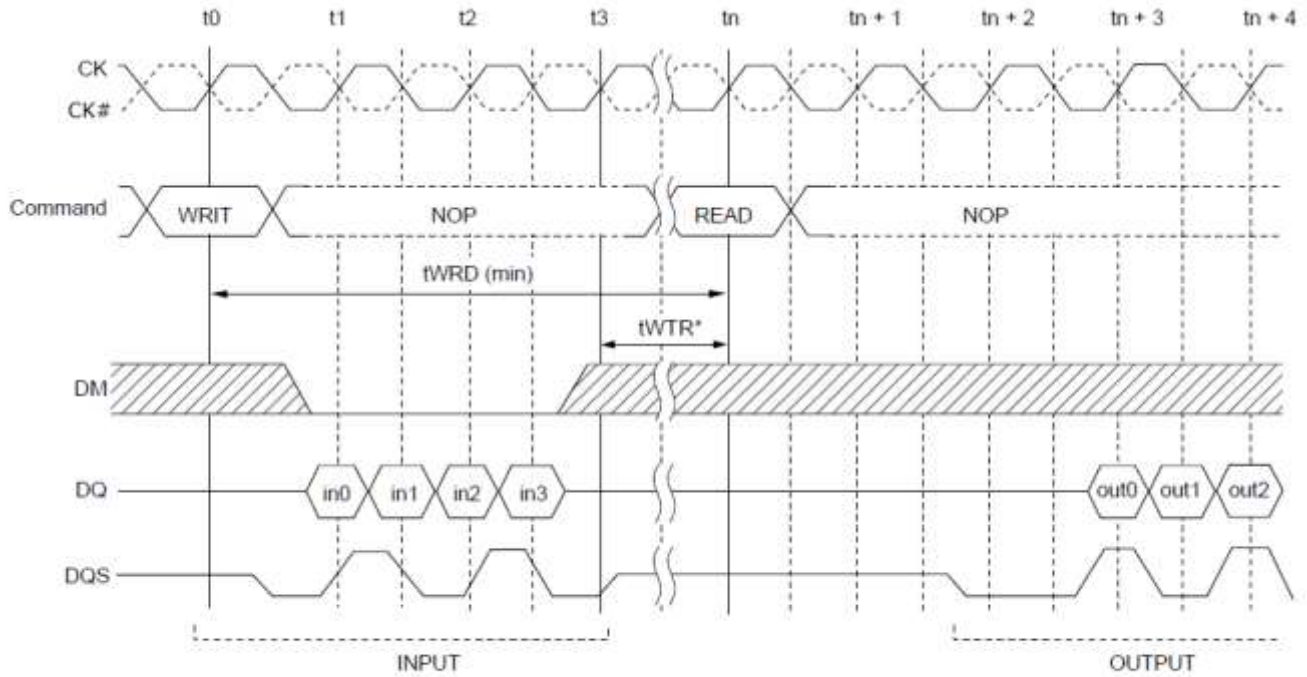


4.7.4 A Write command to the consecutive Read command interval :
To complete the burst operation

Table 4.9 A Write command to the consecutive Read command interval :
To complete the burst operation

| | Destination row of the consecutive read command | | | Operation |
|---|---|-------------|--------|--|
| | Bank address | Row address | State | |
| 1 | Same | Same | ACTIVE | To complete the burst operation, the consecutive read command should be performed tWRD after the write command. |
| 2 | Same | Different | - | Precharge the bank tWPD after the preceding write command. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. See ' A read command to the consecutive precharge interval' section. |
| 3 | Different | Any | ACTIVE | To complete a burst operation, the consecutive read command should be performed tWRD after the write command. |
| | | | IDLE | Precharge the bank independently of the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. |

Figure 4.14 WRITE to READ Command Interval



Note: t_{WTR} is referenced from the first positive CK edge after the last desired data in pair t_{WTR} .

BL = 4
CL = 3

4.7.5 A Write command to the consecutive Read command interval : To interrupt the write operation

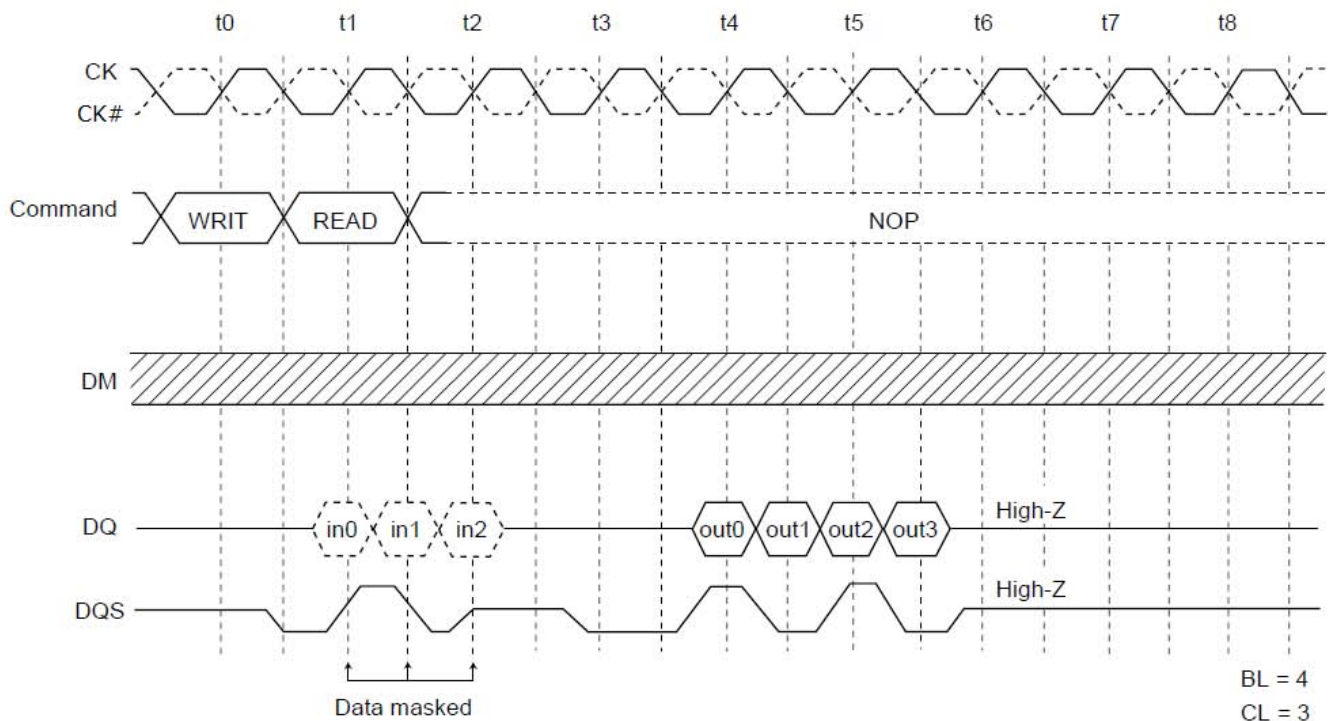
**Table 4.10 A Write command to the consecutive Read command interval :
To interrupt the write operation**

| | Destination row of the consecutive read command | | | Operation |
|---|---|-------------|--------|--|
| | Bank address | Row address | State | |
| 1 | Same | Same | ACTIVE | DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary. |
| 2 | Same | Different | - | Note 1 |
| 3 | Different | Any | ACTIVE | DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary. |
| | | | IDLE | Note 1 |

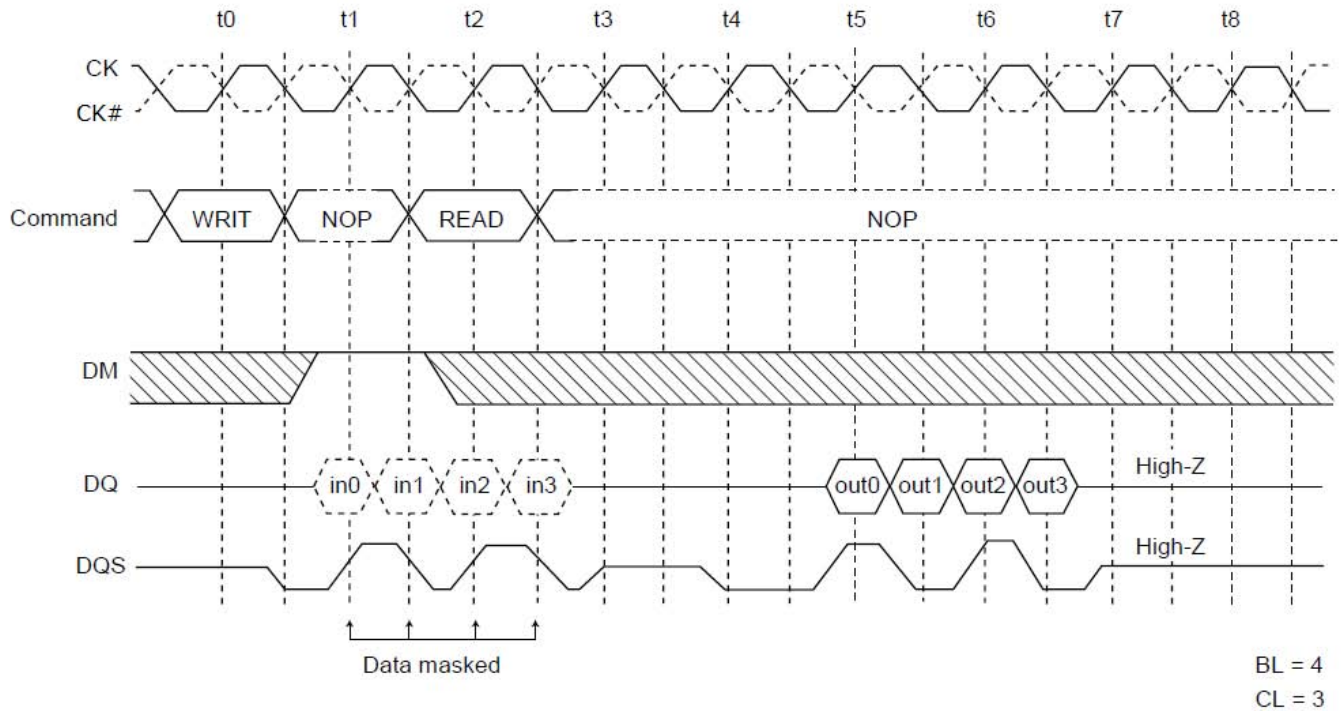
Note :

1. Precharge must be preceded to read command. Therefore read command cannot interrupt the write operation in this case.

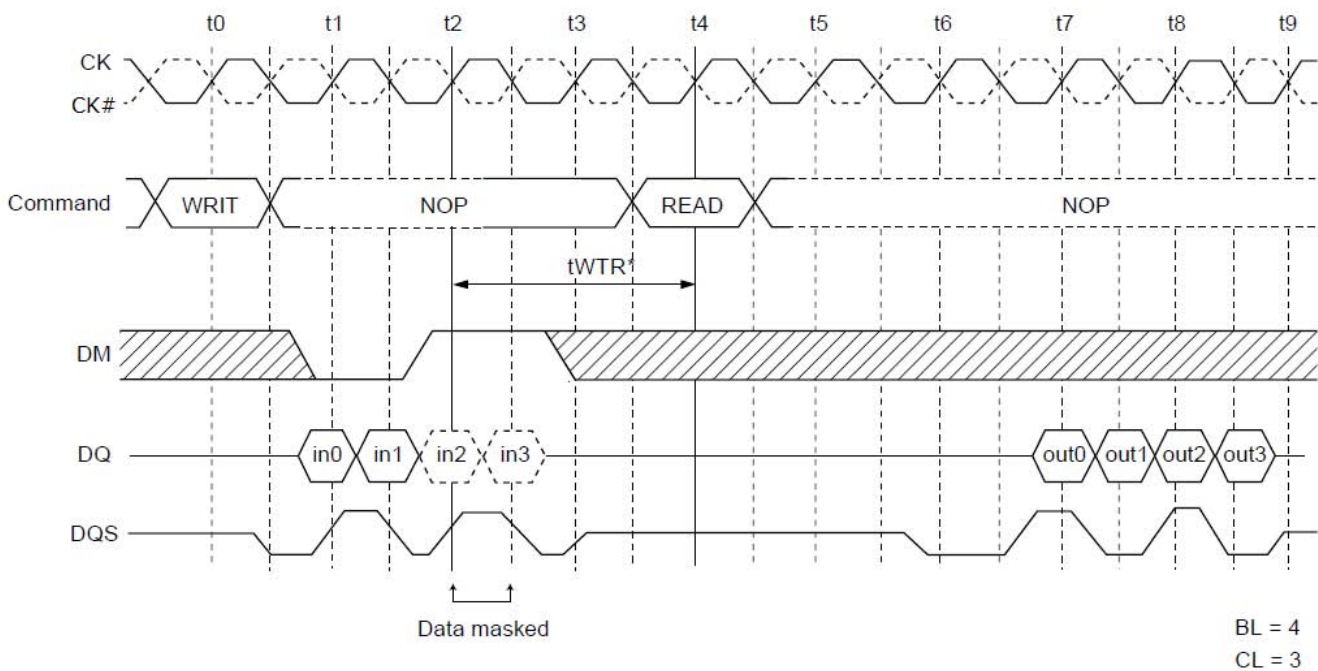
**Figure 4.15 WRITE to READ Command Interval (same bank, same ROW address)
[WRITE to READ delay = 1 clock cycle]**



**Figure 4.16 WRITE to READ Command Interval (same bank, same ROW address)
[WRITE to READ delay = 2 clock cycle]**



**Figure 4.17 WRITE to READ Command Interval (same bank, same ROW address)
[WRITE to READ delay = 4 clock cycle]**



Note : tWTR is referenced from the first positive CK edge after the last desired data in pair tWTR.

4.7.6 A Write command to the Burst stop command interval :
To interrupt the write operation

Figure 4.18 WRITE to BST Command Interval (same bank, same ROW address)
[WRITE to BST delay = 1 clock cycle]

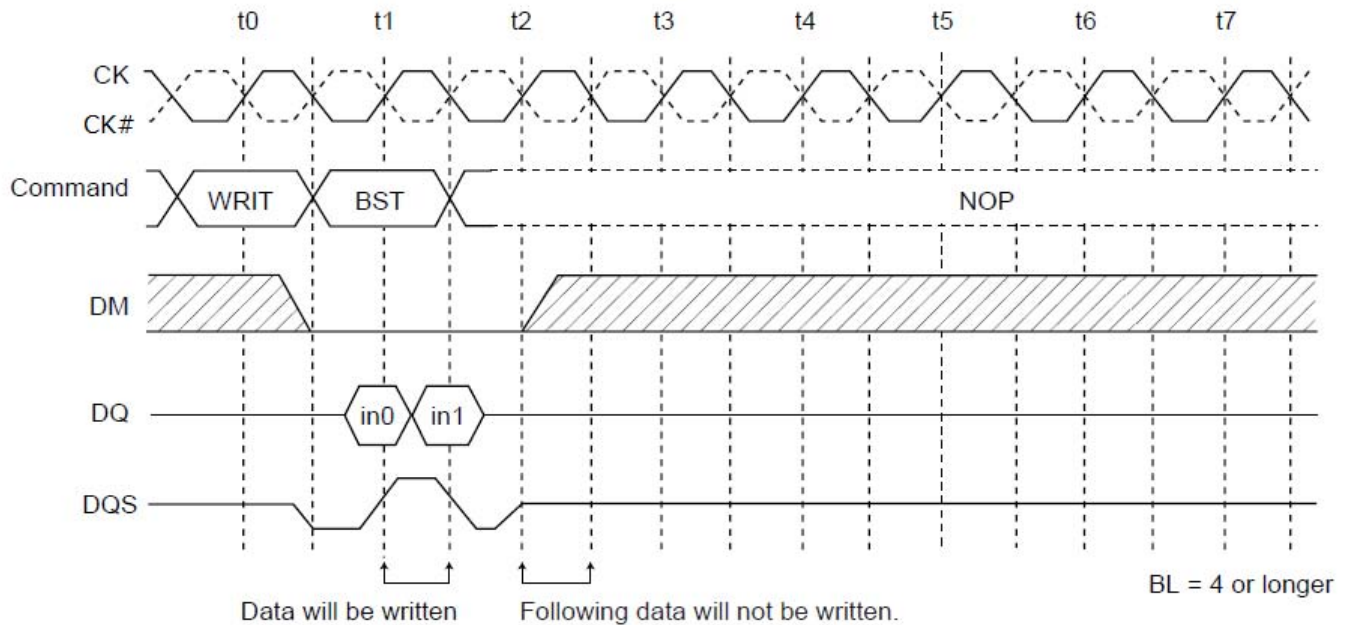
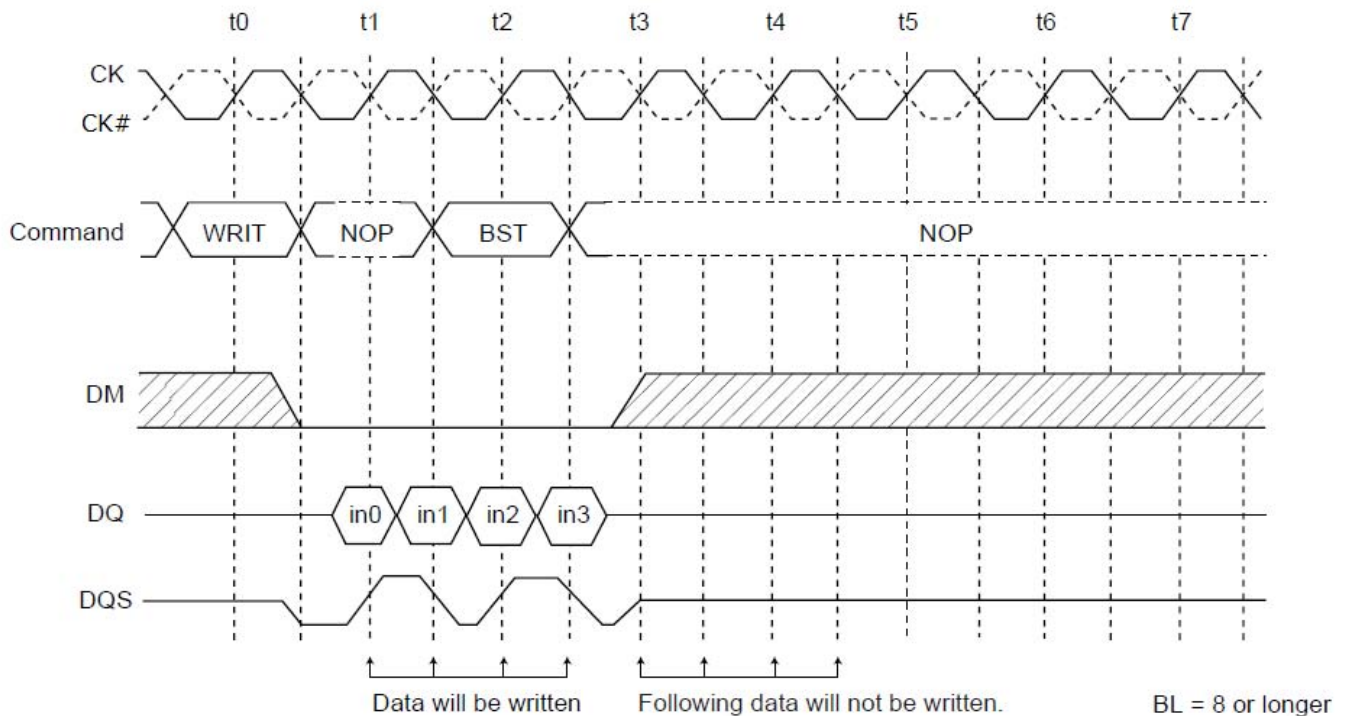


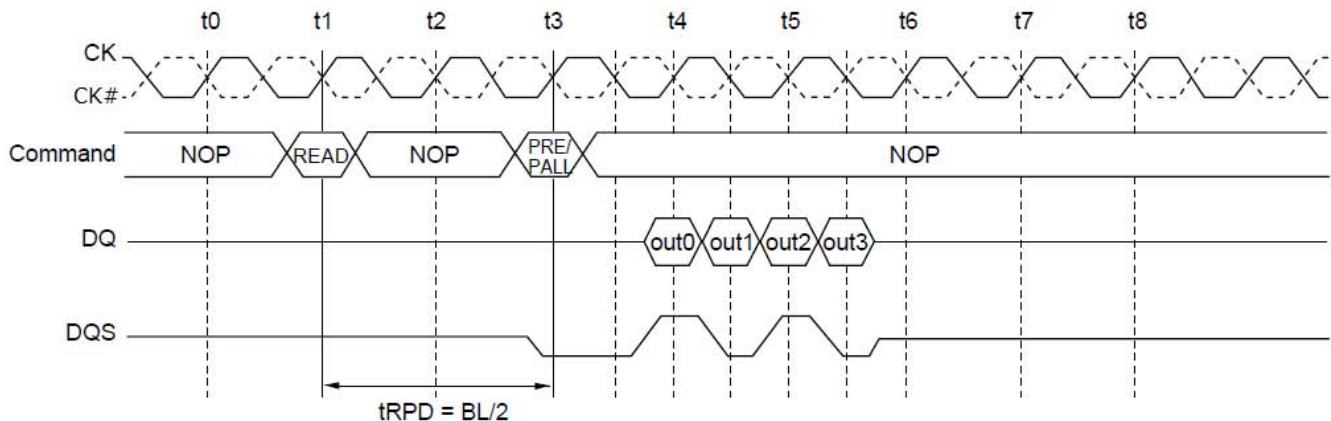
Figure 4.19 WRITE to BST Command Interval (same bank, same ROW address)
[WRITE to BST delay = 2 clock cycle]



READ to PRECHARGE Command Interval (same bank) : To output all data

To complete a burst read operation and get a burst length of data, the consecutive precharge command must be issued $tRPD$ ($= BL/2$ cycles) after the read command is issued.

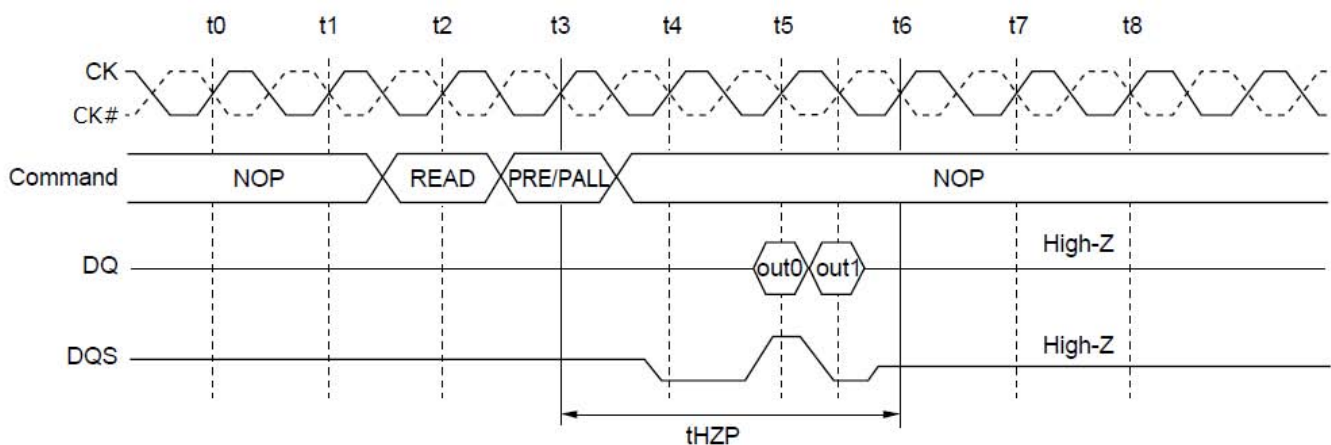
Figure 4.21 READ to PRECHARGE Command Interval (same bank) :
[To output all data (CL=3, BL=4)]



READ to PRECHARGE Command Interval (same bank): To stop output data

A burst data output can be interrupted with a precharge command. All DQ pins and DQS pins become high-Z $tHZP$ ($= CL$) after the precharge command.

Figure 4.22 READ to PRECHARGE Command Interval (same bank) :
[To stop output data (CL=3, BL=4, 8)]



4.7.8 A Write command to the consecutive Precharge command interval (same bank)

Operation by each case of destination bank of the consecutive Precharge command.

Table 4.12 A Write command to the consecutive Precharge command interval (same bank)

| | Bank address | Operation |
|---|--------------|---|
| 1 | Same | The PRE and PALL command can interrupt a write operation. To complete a burst write operation, t_{WPD} is required between the write and the precharge command. Please refer to the following timing chart. |
| 2 | Different | The PRE command does not interrupt a write command. No interval timing is required between the write and the precharge command. |

WRITE to PRECHARGE Command Interval (same bank)

The minimum interval t_{WPD} is necessary between the write command and the precharge command.

Figure 4.23 WRITE to PRECHARGE Command Interval (same bank) : BL=4

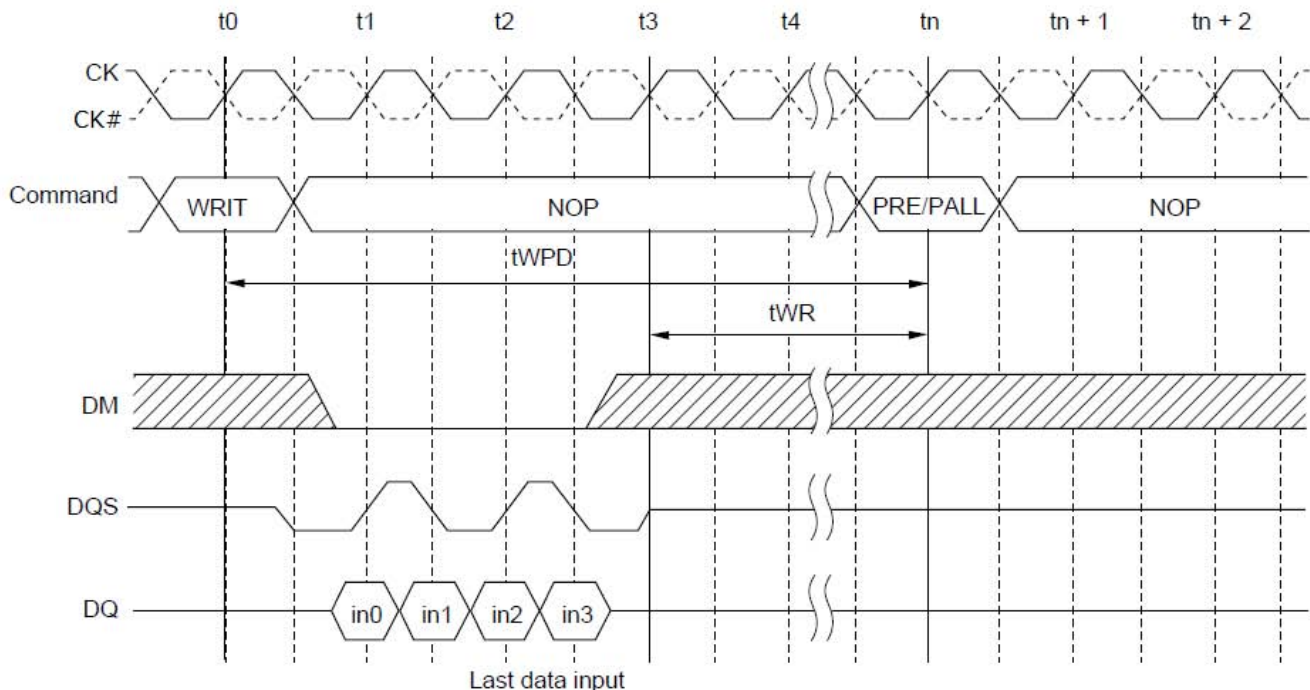
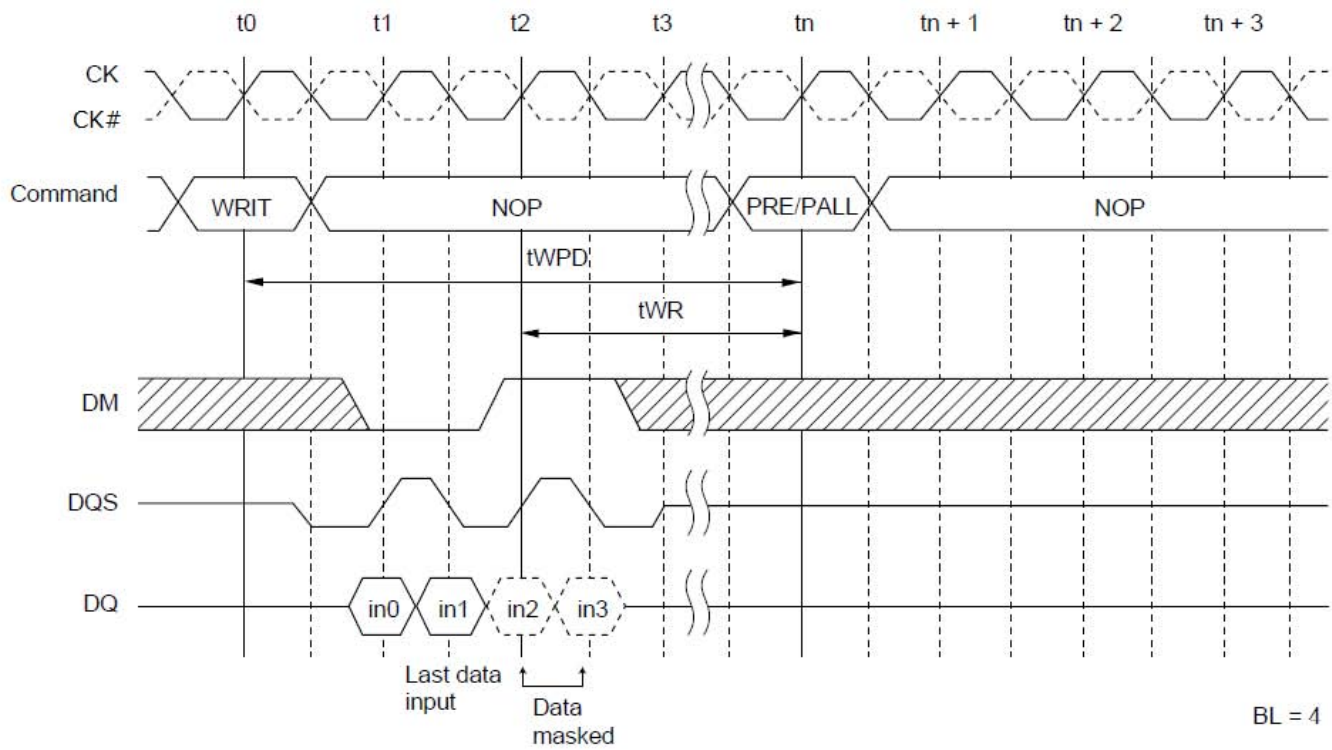
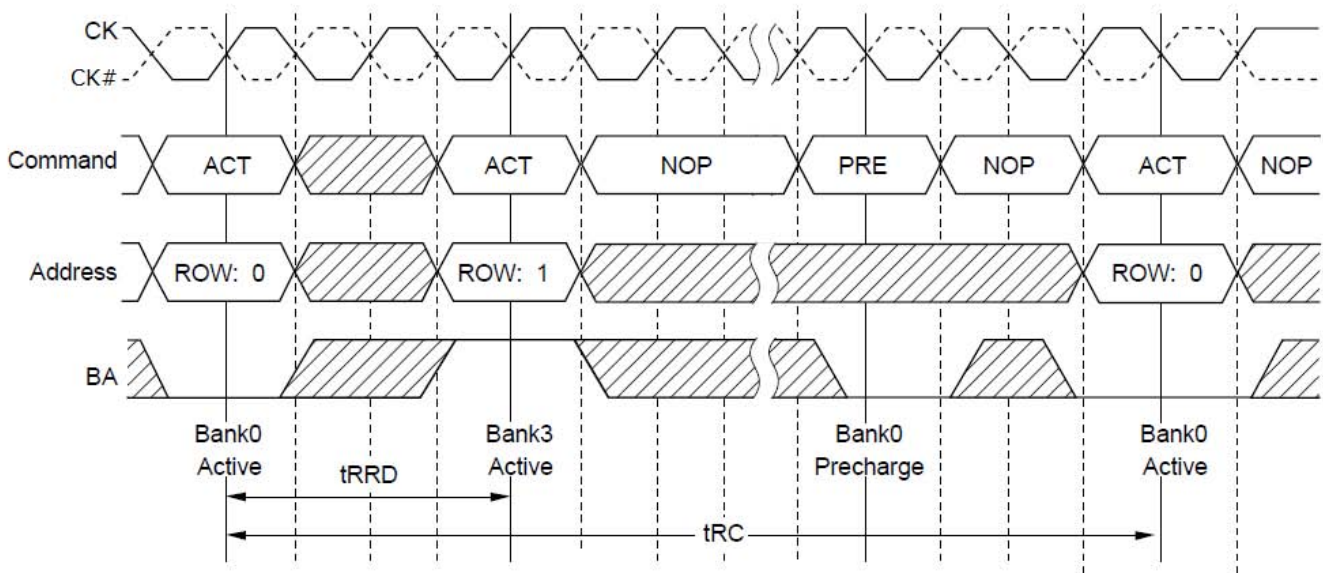


Figure 4.24 WRITE to PRECHARGE Command Interval(same bank):BL=4, DM to mask data


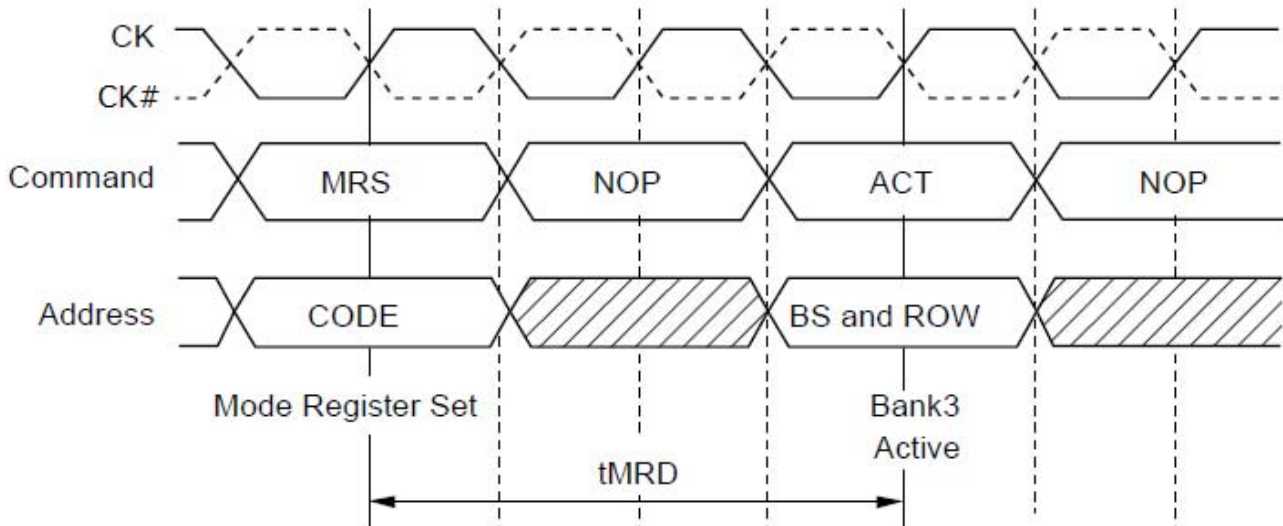
4.7.9 Bank active command interval

Table 4.13 Bank active command interval

| | Destination row of the consecutive ACT command | | | Operation |
|---|--|-------------|--------|--|
| | Bank address | Row address | State | |
| 1 | Same | Any | ACTIVE | Two successive ACT commands can be issued at tRC interval. In between two successive ACT operations, precharge command should be executed. |
| 2 | Different | Any | ACTIVE | Precharge the bank. tRP after the precharge command, the consecutive ACT command can be issued. |
| | | | IDLE | tRRD after an ACT command, the next ACT command can be issued. |

Figure 4.25 Bank Active

Mode register set to Bank-active command interval

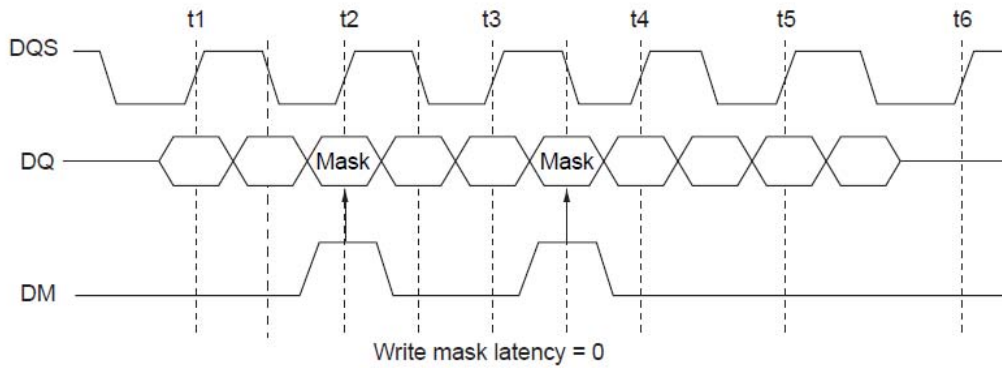
The interval between setting the mode register and executing a bank-active command must be no less than tMRD.

Figure 4.26 Mode Register Set to Bank Active


4.7.10 DM Control

DM can mask input data. By setting DM to low, data can be written. UDM and LDM can mask the upper and lower byte of input data, respectively. When DM is set to high, the corresponding data is not written, and the previous data is held. The latency between DM input and enabling/disabling mask function is 0.

Figure 4.27 DM Control



5. Timing Waveforms

Figure 5.1 Command and Address Input Timing Definition

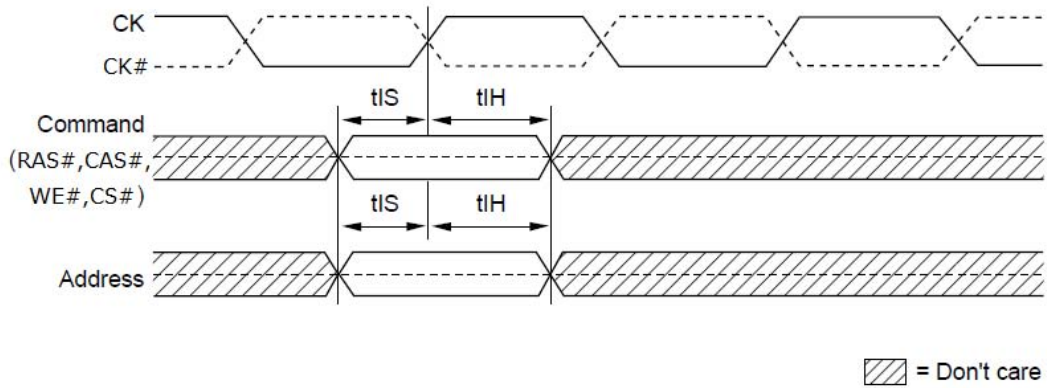


Figure 5.2 Read Timing Definition - 1

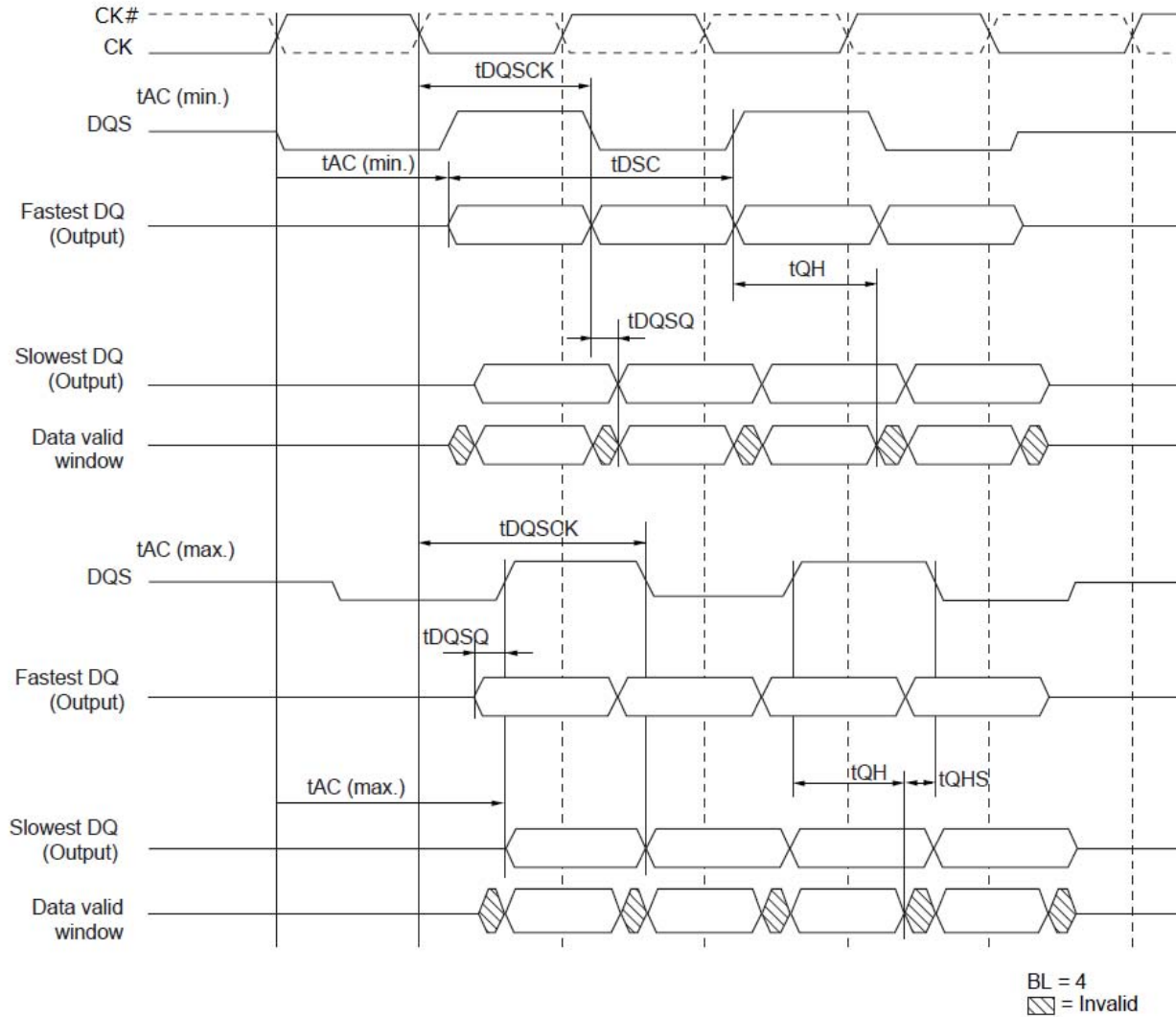


Figure 5.2 Read Timing Definition – 2

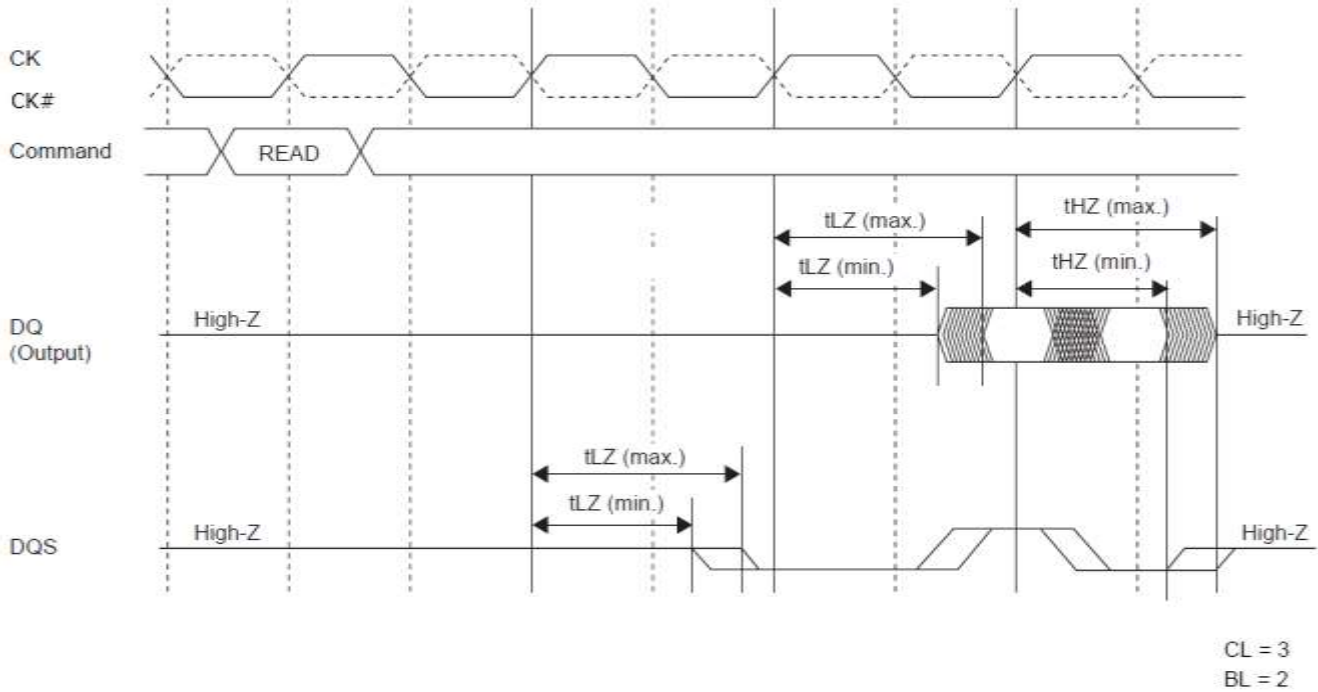


Figure 5.3 Write Timing Definition

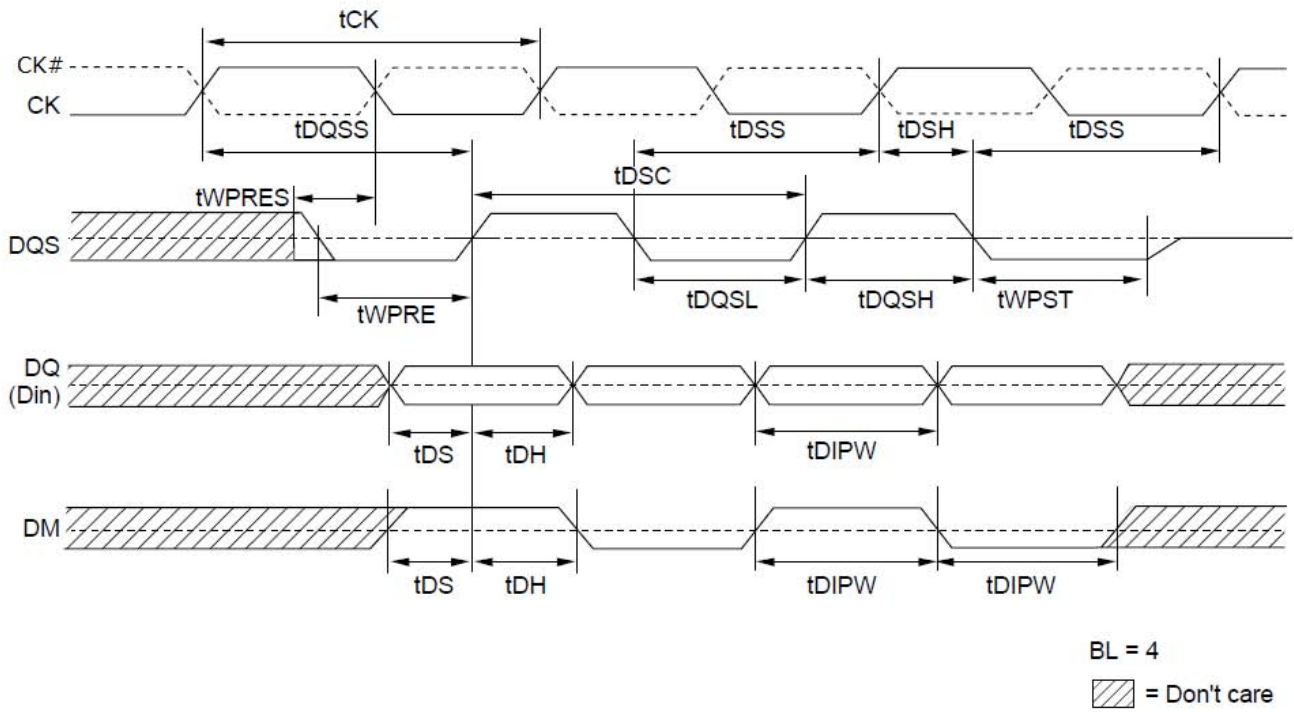


Figure 5.4 Initialize Sequence

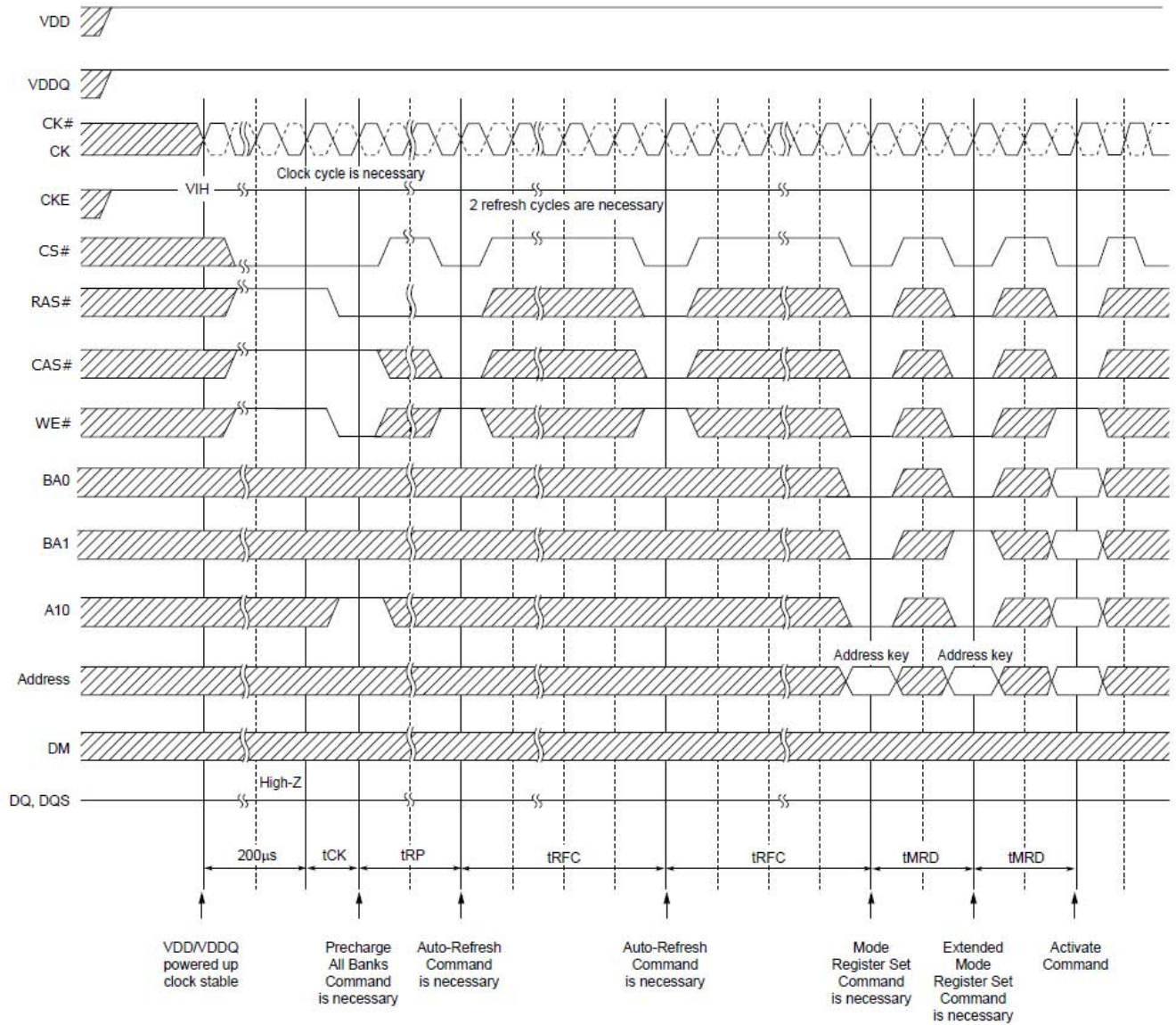


Figure 5.5 Read Cycle

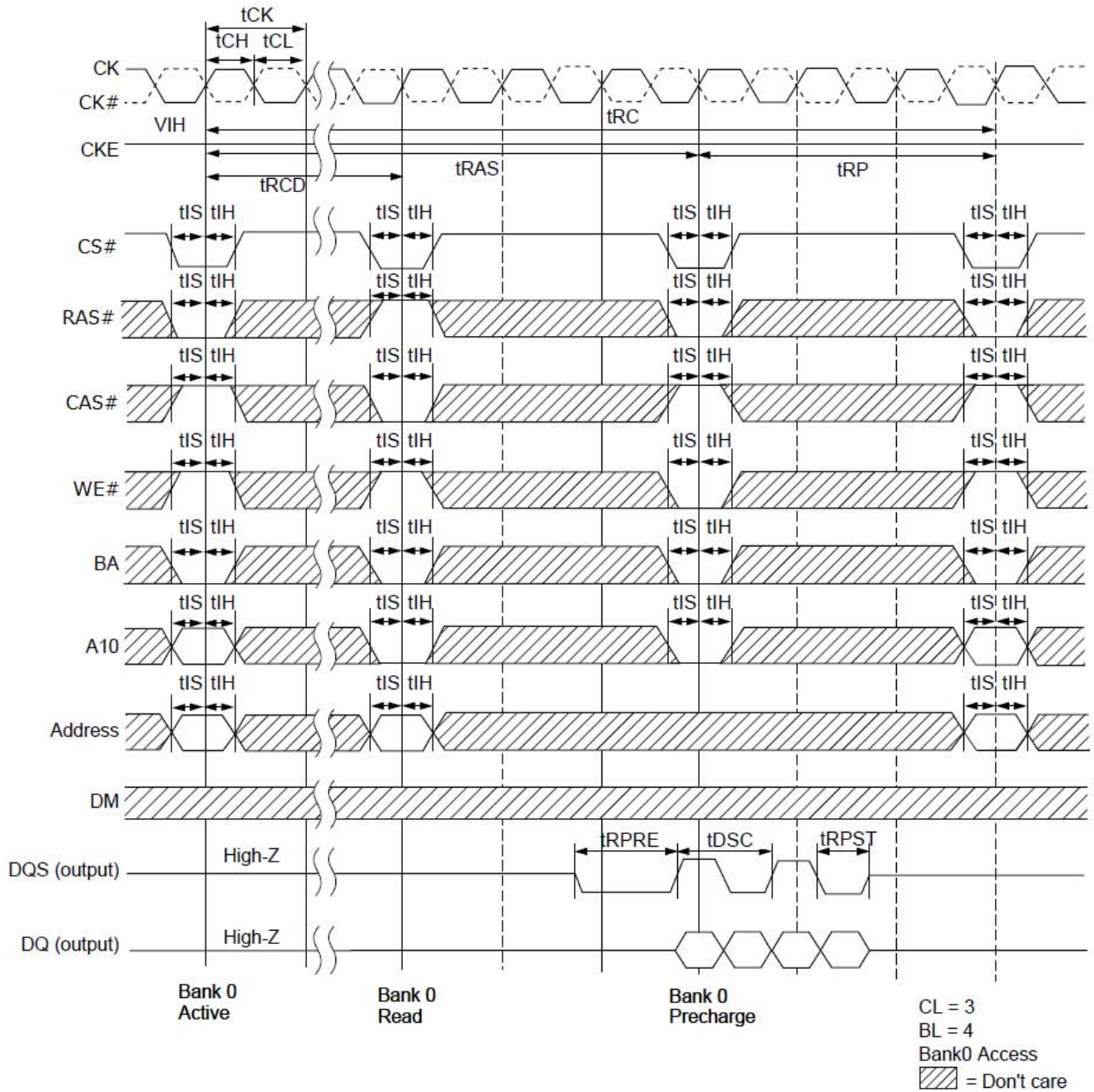


Figure 5.6 Write Cycle

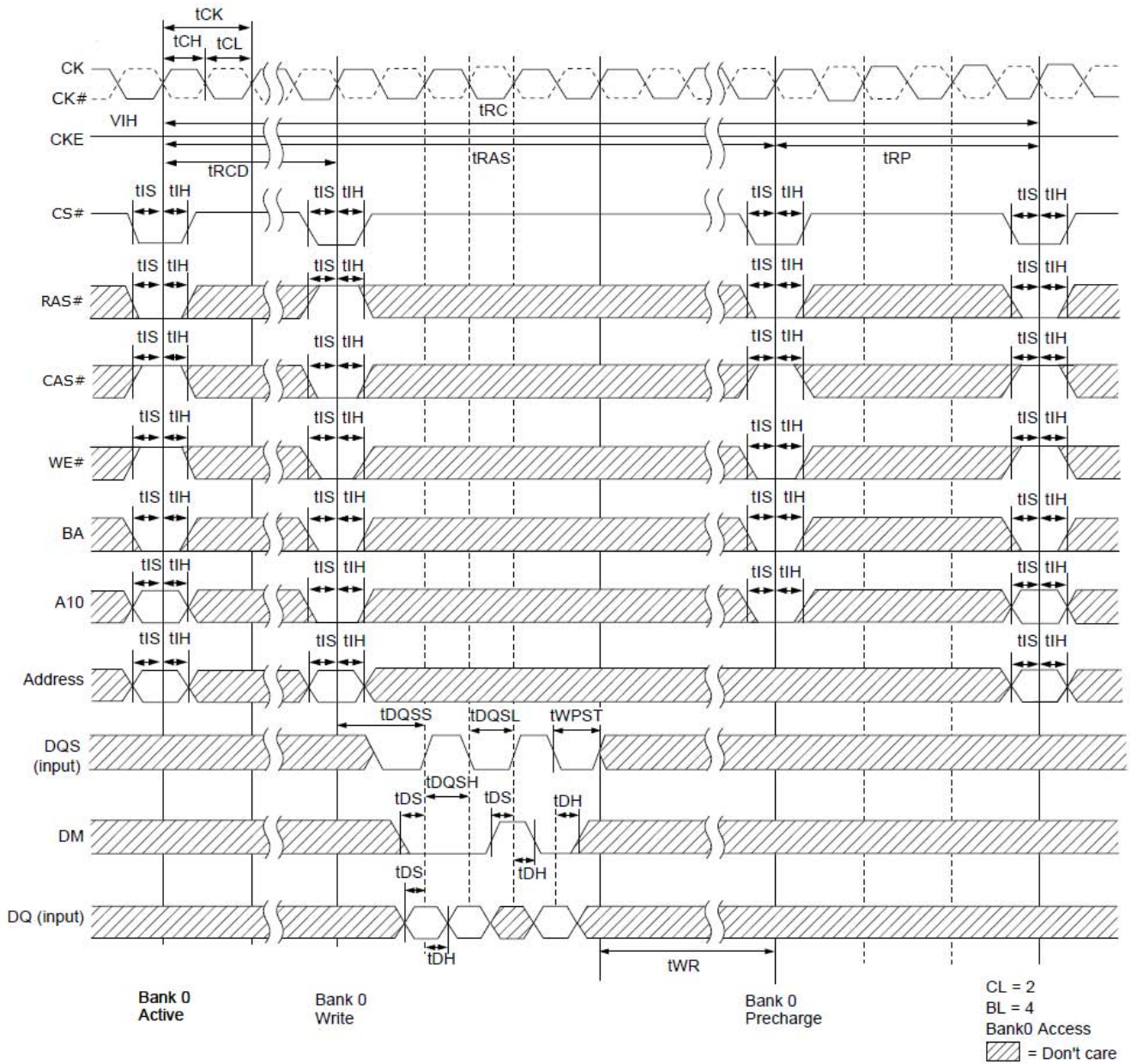


Figure 5.7 Mode Register Set Cycle

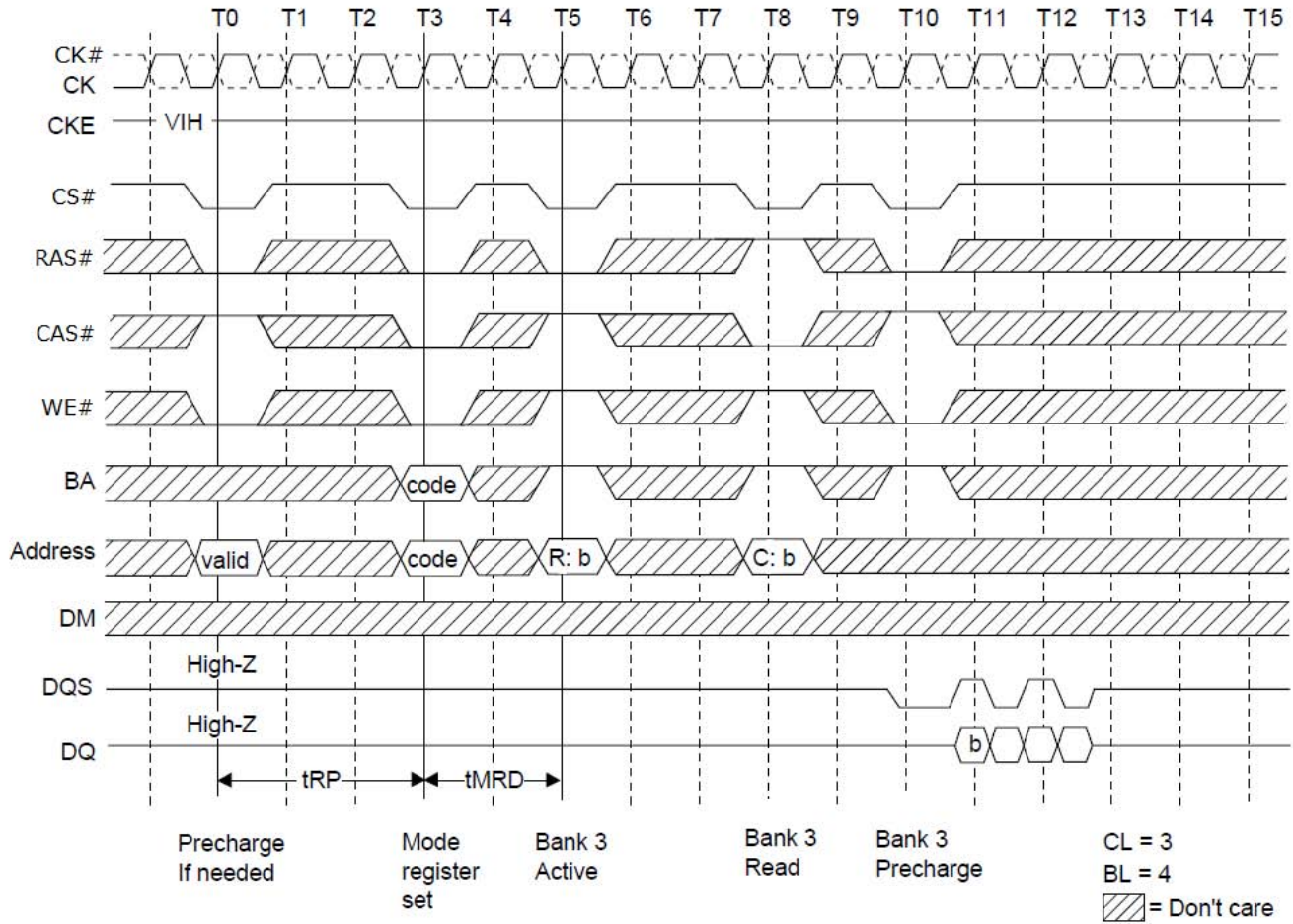


Figure 5.8 Read / Write Cycle

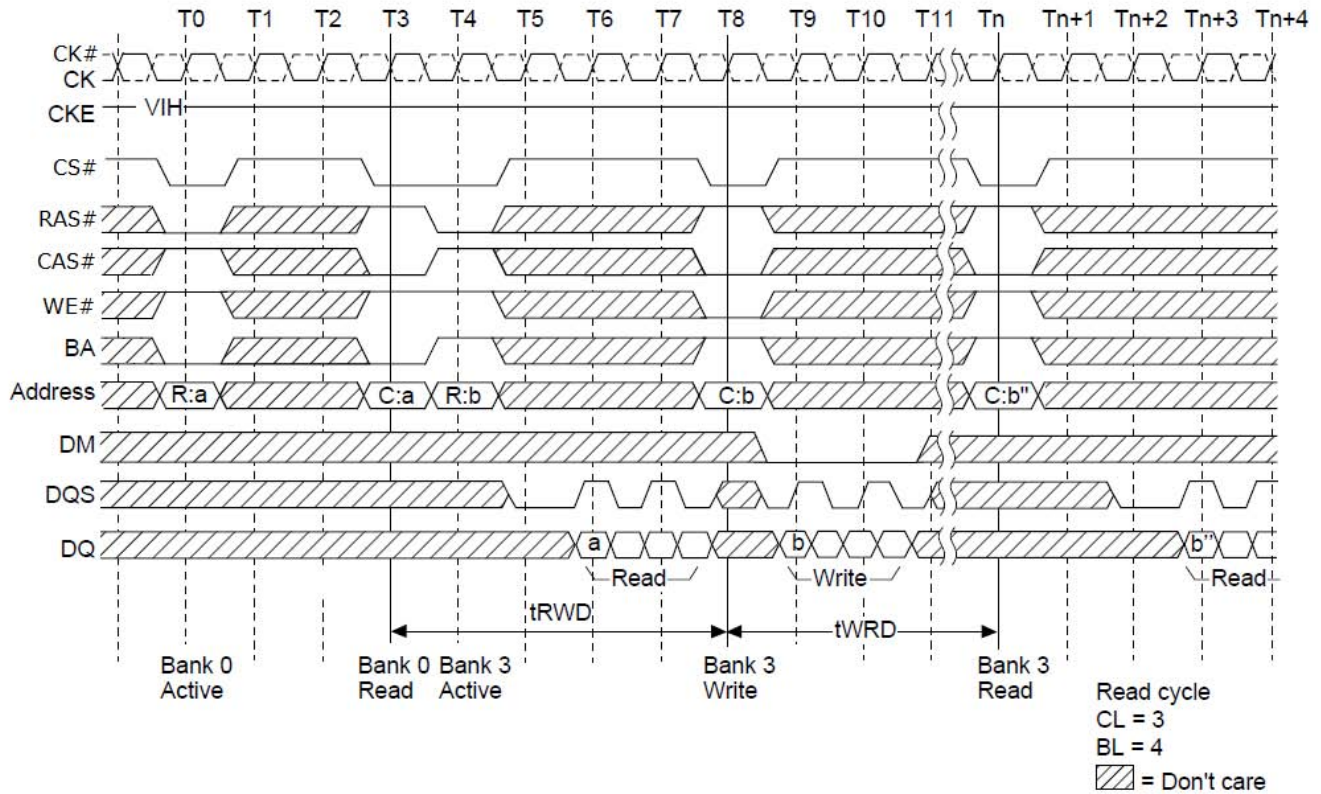


Figure 5.9 Auto Refresh Cycle

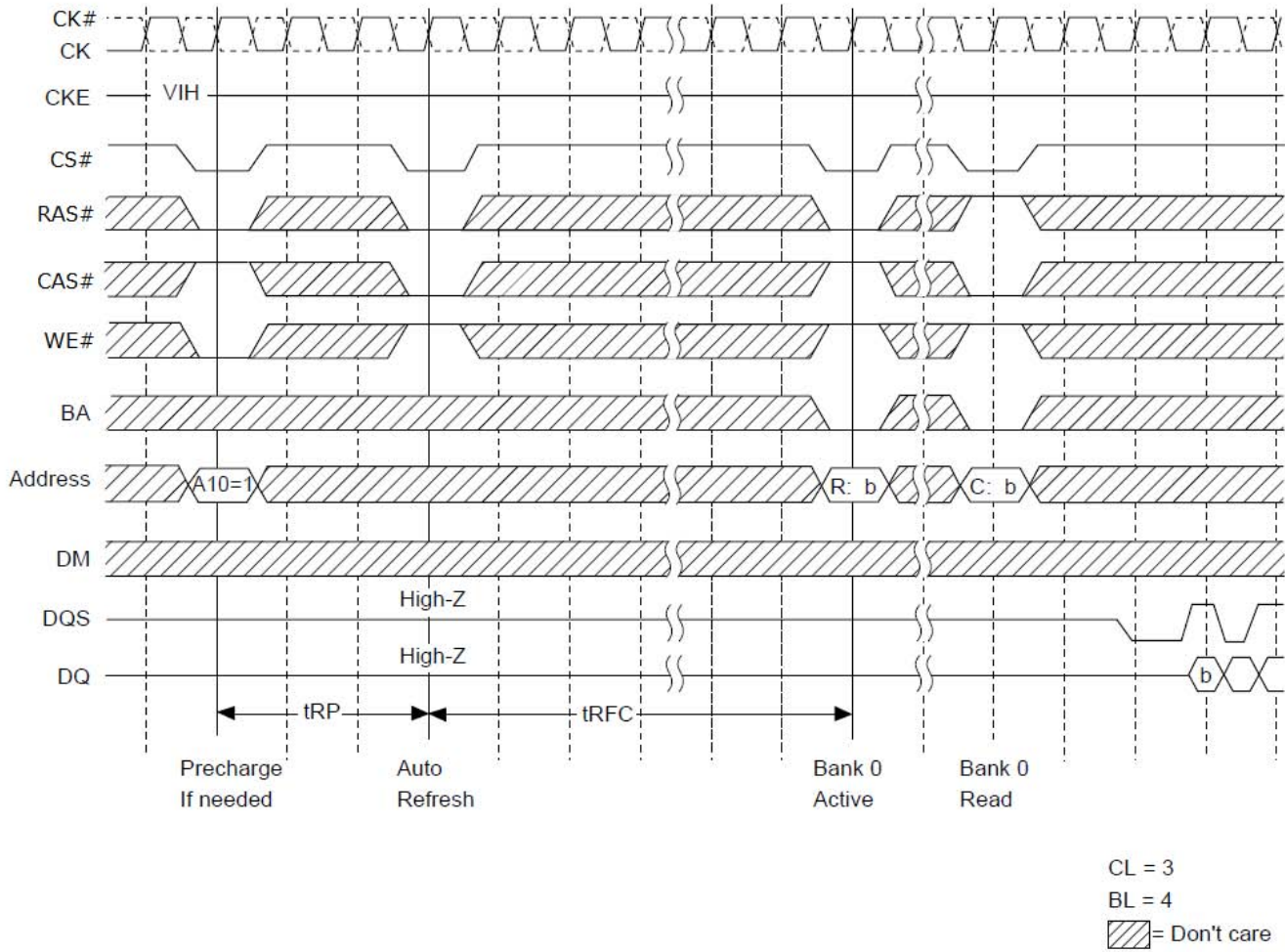


Figure 5.10 Self Refresh Cycle

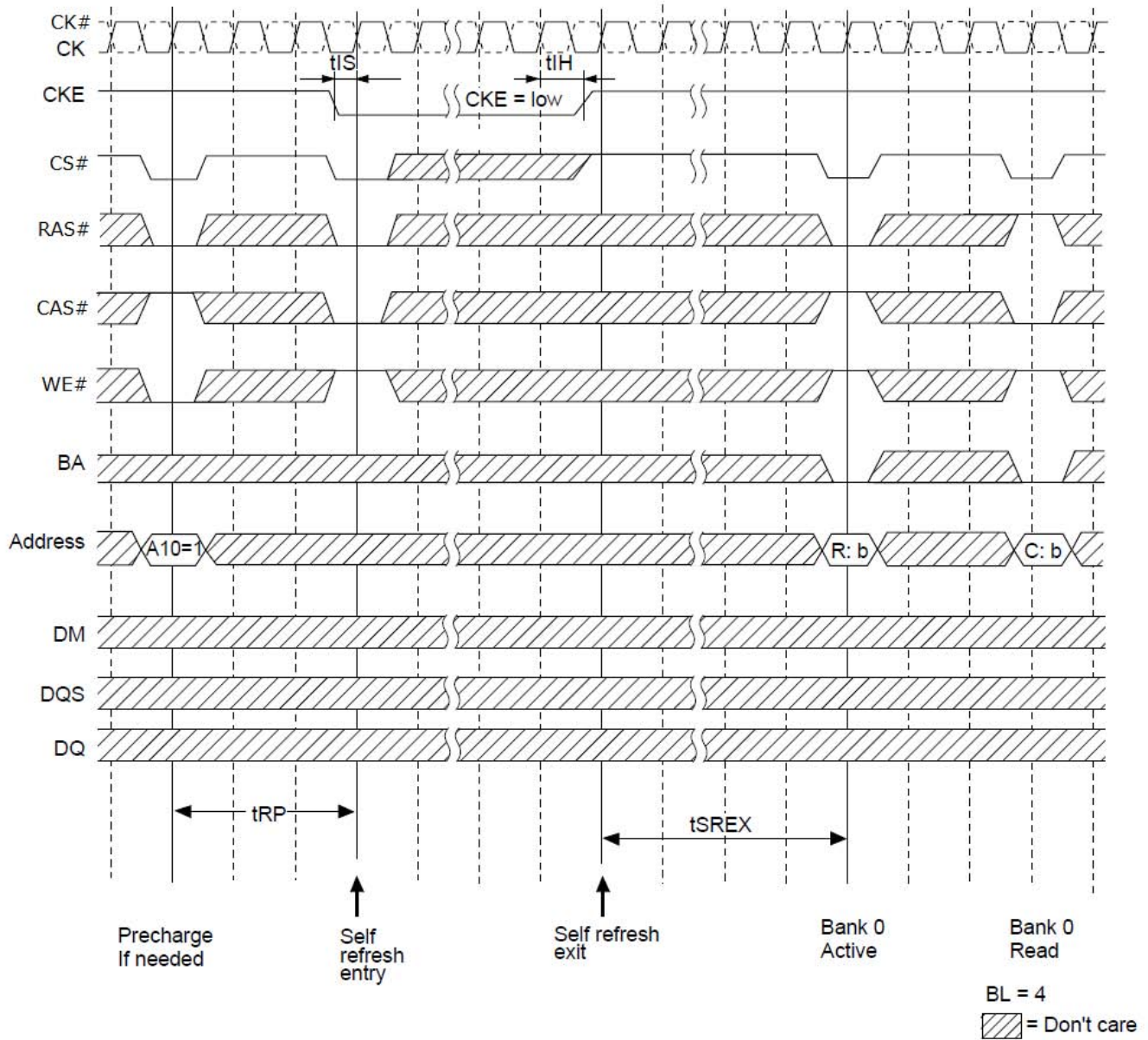


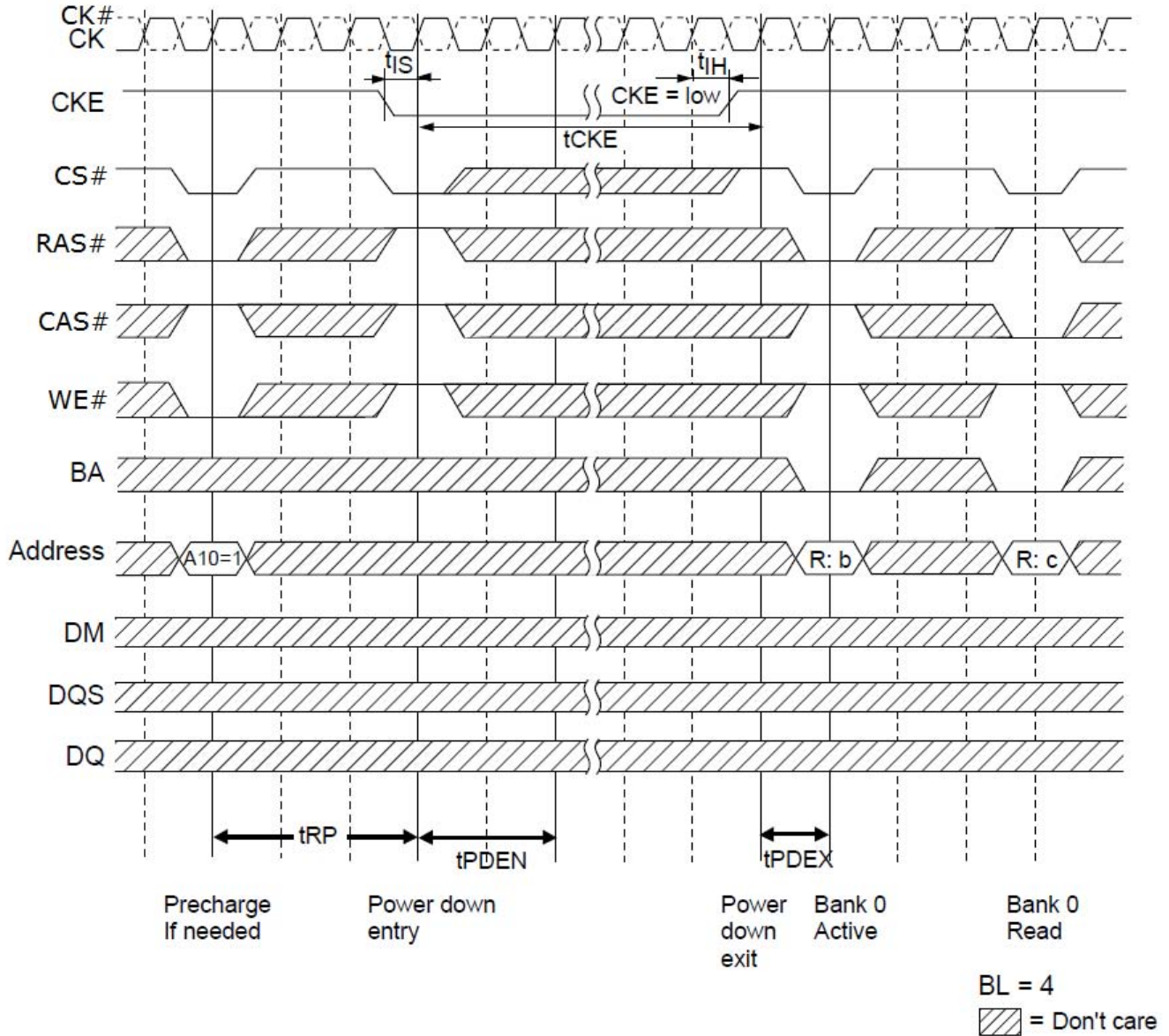
Figure 5.11 Power Down Entry and Exit


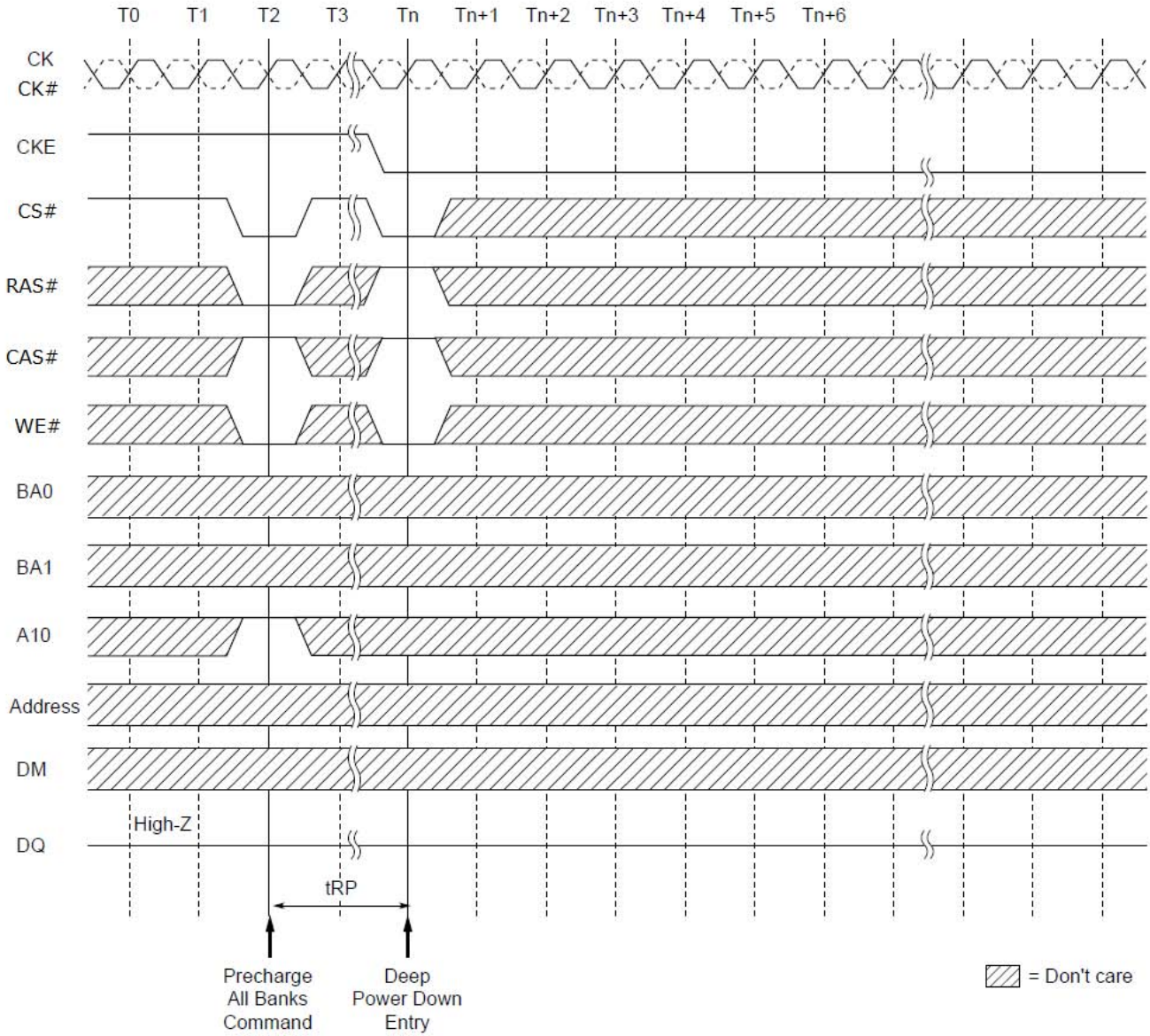
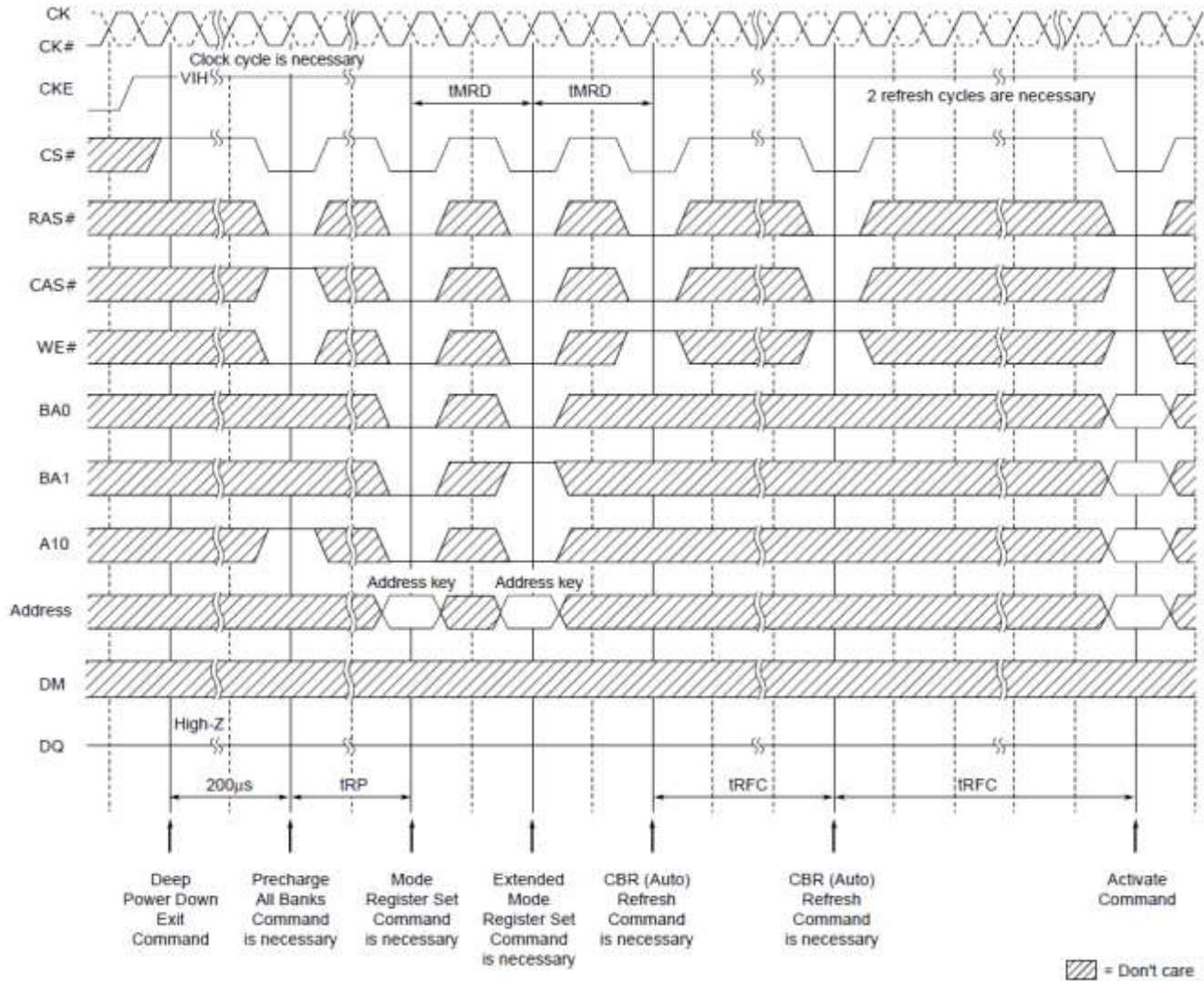
Figure 5.12 Deep Power Down Entry


Figure 5.13 Deep Power Down Exit



Note: The sequence of auto-refresh, mode register programming and extended mode register programming above may be transposed.

6. ELECTRICAL SPECIFICATIONS

- All voltages are referenced to VSS (GND).
- After power-up, wait more than **200 μ s** and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

6.1 Absolute Maximum Ratings

Table 6.1 Absolute maximum ratings

| Parameter | Symbol | Rating | Unit | Note |
|------------------------------------|--------|--------------|------|------|
| Voltage on any pin relative to VSS | VT | -0.5 to +2.3 | V | |
| Supply voltage relative to VSS | VDD | -0.5 to +2.3 | V | |
| Short circuit output current | IOS | 50 | mA | |
| Power dissipation | PD | 1.0 | W | |
| Operating junction temperature | Tj | -30 to +85 | °C | |
| Storage temperature | Tstg | -55 to +125 | °C | |

Caution :

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

6.2 DC Characteristics

Table 6.2 Recommended DC Operating Conditions (Tj=-30°C to +85°C)

| Parameter | Pins | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|----------------------|-----------|------------|------------|------------|------|------|
| Supply voltage | | VDD, VDDQ | 1.7 | 1.8 | 1.95 | V | 1 |
| | | VSS, VSSQ | 0 | 0 | 0 | | |
| Input high voltage | All other input pins | VIH | 0.8 x VDDQ | - | VDDQ + 0.3 | V | |
| Input low voltage | | VIL | -0.3 | - | 0.2 x VDDQ | V | |
| DC input Voltage level | CK, CK# | VIN(DC) | -0.3 | - | VDDQ + 0.3 | V | |
| AC Input differential cross point voltage | | VIX | 0.4 x VDDQ | 0.5 x VDDQ | 0.6 x VDDQ | | 6 |
| DC input differential voltage | | VID(DC) | 0.4 x VDDQ | - | VDDQ + 0.6 | | 5 |
| AC input differential voltage | | VID(AC) | 0.6 x VDDQ | - | VDDQ + 0.6 | | 5 |
| DC input high voltage | DQ, DM, DQS | VIHD(DC) | 0.7 x VDDQ | - | VDDQ + 0.3 | V | |
| DC input low voltage | | VILD(DC) | -0.3 | - | 0.3 x VDDQ | | |
| AC input high voltage | | VIHD(AC) | 0.8 x VDDQ | - | VDDQ + 0.3 | | |
| AC input low voltage | | VILD(AC) | -0.3 | - | 0.2 x VDDQ | | |

Notes:

1. VDDQ must be equal to VDD.
2. VIH (max.) = 2.3V (pulse width \leq 5ns).
3. VIL (min.) = -0.5V (pulse width \leq 5ns).
4. All voltage referred to VSS and VSSQ must be same potential.
5. VID (DC) and VID (AC) are the magnitude of the difference between the input level on CK and the input level on CK#.
6. The value of VIX is expected to be 0.5 x VDDQ and must track variations in the DC level of the same.

Table 6.3 DC Characteristics-I (Tj = -30°C to +85°C, VDD and VDDQ = 1.7V to 1.95V, VSS and VSSQ = 0V)

| Parameter | Symbol | Max. | Unit | Test Condition |
|--|--------|------|------|--|
| Operating current (ACT-PRE) | IDD0 | 85 | mA | One bank active-precharge, CKE = H, CS# = H between valid commands, tCK = tCK (min.), tRC = tRC (min.), Address bus inputs are SWITCHING; Data bus inputs are STABLE |
| Standby current in power down | IDD2P | 0.8 | mA | All banks idle, CKE=L, CS#=H, tCK=tCK (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Standby current in power down with clock stop | IDD2PS | 0.6 | mA | All banks idle, CKE=L, CS#=H, CK=L, CK#=H, Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Standby current in non-power down | IDD2N | 7.0 | mA | All banks idle, CKE=H, CS#=H, tCK=tCK (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Standby current in non-power down with clock stop | IDD2NS | 2.0 | mA | All banks idle, CKE=H, CS#=H, CK=L, CK#=H, Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Active standby current in power down | IDD3P | 3.0 | mA | One bank active, CKE=L, CS#=H, tCK=tCK (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Active standby current in power down with clock stop | IDD3PS | 2.0 | mA | One bank active, CKE=L, CS#=H, CK=L, CK#=H; Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Active standby current in non-power down | IDD3N | 10 | mA | One bank active, CKE=H, CS#=H, tCK=tCK (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Active standby current in non-power down with clock stop | IDD3NS | 7.0 | mA | One bank active, CKE=H, CS#=H, CK=L, CK#=H, Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Burst operating current | IDD4 | 135 | mA | One bank active, Continuous burst reads or writes; tCK=tCK (min.), CL=3, BL=4, IOOUT = 0mA, Address inputs are SWITCHING, 50% data change each burst transfer |
| Auto-refresh current | IDD5 | 90 | mA | CKE=H, tCK=tCK (min.), tRFC=tRFC (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE |
| Deep power down current | IDD8 | 10 | uA | Address and control inputs are STABLE; Data bus inputs are STABLE |

**Table 6.4 Advanced Data Retention Current ($T_j = -30^\circ\text{C}$ to $+85^\circ\text{C}$,
VDD and VDDQ = 1.7V to 1.95V, VSS and VSSQ = 0V)**

| Parameter | Symbol | Typ. | Max. | Unit | Condition |
|---|--------|------|------|------|--|
| Advanced data retention current (Self refresh current) | | | | | |
| PASR="000" (Full) | IDD6 | - | 400 | uA | $-30^\circ\text{C} \leq T_J \leq +40^\circ\text{C}$ CKE = L |
| PASR="001" (2BK) | | - | 350 | | |
| PASR="010" (1BK) | | - | 330 | | |
| PASR="000" (Full) | IDD6 | - | 600 | | $+40^\circ\text{C} < T_J \leq +70^\circ\text{C}$ CKE = L |
| PASR="001" (2BK) | | - | 450 | | |
| PASR="010" (1BK) | | - | 380 | | |
| PASR="000" (Full) | IDD6 | - | 700 | | $+70^\circ\text{C} < T_J \leq +85^\circ\text{C}$ CKE = L |
| PASR="001" (2BK) | | - | 500 | | |
| PASR="010" (1BK) | | - | 400 | | |

Notes:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by Test Conditions.
3. Definitions for IDD:
 - L is defined as $V_{IN} \leq 0.1 \times V_{DDQ}$;
 - H is defined as $V_{IN} \geq 0.9 \times V_{DDQ}$;
 - STABLE is defined as inputs stable at an H or L level;
 - SWITCHING is defined as:
 - Address and command: inputs changing between H and L once per two clock cycles;
 - Data bus inputs: DQ changing between H and L once per clock cycle; DM and DQS are STABLE.

**Table 6.5 DC Characteristics -II ($T_j = -30^\circ\text{C}$ to $+85^\circ\text{C}$, VDD and VDDQ = 1.7V to 1.95V,
VSS and VSSQ = 0V)**

| Parameter | Symbol | Min. | Max. | Unit | Test Condition |
|------------------------|--------|----------------------|----------------------|------|---|
| Input leakage current | ILI | -2.0 | 2.0 | uA | $0 \leq V_{IN} \leq V_{DDQ}$ |
| Output leakage current | ILO | -1.5 | 1.5 | uA | $0 \leq V_{OUT} \leq V_{DDQ}$, DQ = disable |
| Output high voltage | VOH | $0.9 \times V_{DDQ}$ | - | V | IOH = -0.1mA |
| Output low voltage | VOL | - | $0.1 \times V_{DDQ}$ | V | IOL = 0.1 mA |

Table 6.6 Pin Capacitance (TA = +25°C, VDD and VDDQ = 1.7V to 1.95V)

| Parameter | Symbol | Pins | Min. | Typ. | Max. | Unit | Note |
|--------------------------------|--------|---------------------------|------|------|------|------|------|
| Input capacitance | CL1 | CK, CK# | 1.5 | - | 3.5 | pF | 1 |
| | CL2 | All other input only pins | 1.5 | - | 3.0 | | 1 |
| | Cdi1 | CK, CK# | - | - | 0.25 | | 1 |
| Delta input capacitance | | | | | | | |
| | Cdi2 | All other input only pins | - | - | 0.5 | | 1 |
| Data input/output capacitance | CI/O | DQ, DM, DQS | 2.0 | - | 4.5 | | |
| Delta input/output capacitance | Cdio | DQ, DM, DQS | - | - | 0.5 | | 1 |

Notes:

1. These parameters are measured on conditions: $f = 100\text{MHz}$, $V_{OUT} = V_{DDQ}/2$, $\Delta V_{OUT} = 0.2\text{V}$, $T_A = +25^\circ\text{C}$.
2. DOUT circuits are disabled.

6.3 AC Characteristics

Table 6.7 AC Characteristics (Reference) (Tj=-30°C to +85°C,

VDD and VDDQ = 1.7V to 1.95V, VSS and VSSQ = 0V)

| Parameter | Symbol | Min. | Max. | Unit | Note |
|--|--------|-------------------|------|------|------|
| Clock cycle time | tCK | 5.0 | - | ns | |
| CK high-level width | tCH | 0.45 | 0.55 | tCK | |
| CK low-level width | tCL | 0.45 | 0.55 | tCK | |
| CK half period | tHP | Min. (tCH,tCL) | - | tCK | |
| DQ output access time from CK, CK# | tAC | 2.0 | 5.0 | ns | 2, 8 |
| DQS-in cycle time | tDSC | 0.9 | 1.1 | tCK | |
| DQS output access time from CK, CK# | tDQSC | 2.0 | 5.0 | ns | 2, 8 |
| DQ-out high-impedance time from CK, CK# | tHZ | - | 5.0 | ns | 5, 8 |
| DQ-out low-impedance time from CK, CK# | tLZ | 1.0 | - | ns | 6, 8 |
| DQS to DQ skew | tDOSQ | - | 0.4 | ns | 3 |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | - | ns | 4 |
| Data hold skew factor | tQHS | - | 0.5 | ns | |
| DQ and DM input setup time | tDS | 0.5 | - | ns | 3 |
| DQ and DM input hold time | tDH | 0.5 | - | ns | 3 |
| DQ and DM input pulse width | tDIPW | 1.6 | - | ns | |
| Read preamble | tRPRE | 0.9 | 1.1 | tCK | |
| Read post-amble | tRPST | 0.4 | 0.6 | tCK | |
| Write preamble setup time | tWPRES | 0 | - | ns | |
| Write preamble | tWPRE | 0.25 | - | tCK | |
| Write post-amble | tWPST | 0.4 | 0.6 | tCK | 7 |
| Write command to first DQS latching transition | tDOSS | 0.75 | 1.25 | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | - | tCK | |

| | | | | | |
|--|-------|--------|--------|-----|---|
| DQS falling edge hold time from CK | tDSH | 0.2 | - | tCK | |
| DQS input high pulse width | tDSH | 0.4 | - | tCK | |
| DQS input low pulse width | tDQSL | 0.4 | - | tCK | |
| Address and control input setup time | tIS | 0.9 | - | ns | 3 |
| Address and control input hold time | tIH | 0.9 | - | ns | 3 |
| Address and control input pulse width | tIPW | 2.3 | - | ns | 3 |
| Mode register set command cycle time | tMRD | 2 | - | tCK | |
| Active to Precharge command period | tRAS | 40 | 120000 | ns | |
| Active to Active/Auto-refresh command period | tRC | 55 | - | ns | |
| Auto-refresh to Active/Auto-refresh command period | tRFC | 96 | - | ns | |
| Active to Read/Write delay | tRCD | 15 | - | ns | |
| Precharge to active command period | tRP | 15 | - | ns | |
| Column address to column address delay | tCCD | 1 | - | tCK | |
| Active to active command period | tRRD | 10 | - | ns | |
| Write recovery time | tWR | 15 | - | ns | |
| Auto pre-charge write recovery and pre-charge time | tDAL | - | - | - | 9 |
| Self-Refresh Exit Period | tSREX | 120 | - | ns | |
| Power-down entry | tPDEN | 2 | - | tCK | |
| Power-down exit to command input | tPDEX | 1 | - | tCK | |
| Internal Write to Read command delay | tWTR | 2 | - | tCK | |
| Refresh period | tREF | - | 64 | ms | |
| Average periodic refresh interval | tREFI | - | 7.8 | us | |
| CKE minimum pulse width | tCKE | 2 | - | tCK | |
| Write to pre-charge command delay (same bank) | tWPD | 4+BL/2 | - | tCK | |
| Read to pre-charge command delay (same bank) | tRPD | BL/2 | - | tCK | |
| Write to read command delay (to input all data) | tWRD | 3+BL/2 | - | tCK | |

| | | | | | |
|---|-------|---|---|-----|--|
| Burst stop command to write command delay (CL = 3) | tBSTW | 3 | - | tCK | |
|---|-------|---|---|-----|--|

| | | | | | |
|--|-------|--------|---|-----|--|
| Burst stop command to DQ high-Z (CL = 3) | tBSTZ | 3 | - | tCK | |
| Read command to write command delay (to output all data) (CL = 3) | tRWD | 3+BL/2 | - | tCK | |
| Pre-charge command to high-Z (CL = 3) | tHZP | 3 | - | tCK | |
| Mode register set command cycle time | tMRD | 2 | - | tCK | |

Notes:

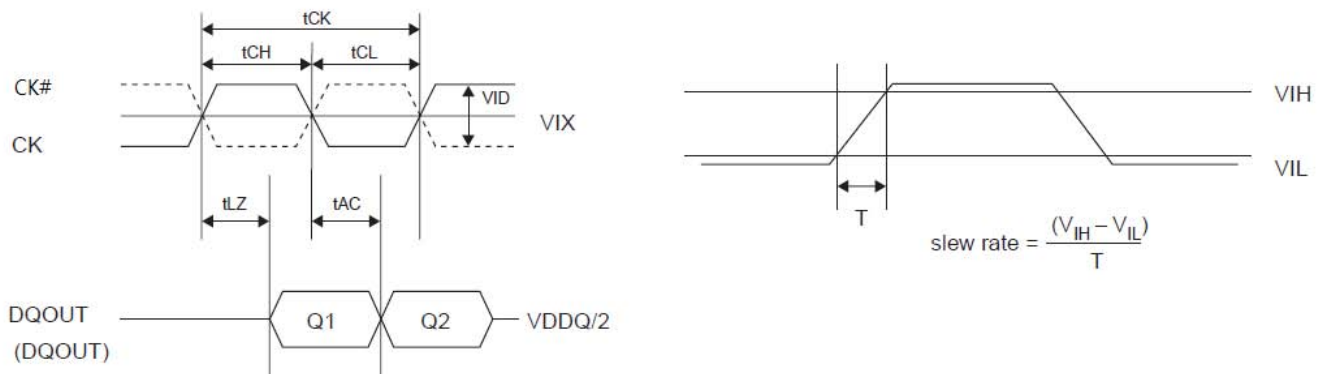
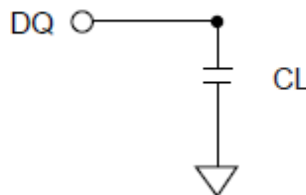
1. On all AC measurements, we assume the test conditions shown in “**Test conditions**” and full driver strength is assumed for the output load, that is both A6 and A5 of EMRS is set to be “L”.
2. This parameter defines the signal transition delay from the cross point of CK and CK#. The signal transition is defined to occur when the signal level crossing VDDQ/2.
3. The timing reference level is VDDQ/2.
4. Output valid window is defined to be the period between two successive transitions of data out signals. The signal transition is defined to occur when the signal level crossing VDDQ/2.
5. tHZ is defined as DOUT transition delay from low-Z to high-Z at the end of read burst operation. The timing reference is cross point of CK and CK#. This parameter is not referred to a specific DOUT voltage level, but specify when the device output stops driving.
6. tLZ is defined as DOUT transition delay from high-Z to low-Z at the beginning of read operation. This parameter is not referred to a specific DOUT voltage level, but specify when the device output begins driving.
7. The transition from low-Z to high-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
8. tAC, tDQSCK, tHZ and tLZ are specified with 15pF bus loading condition.
9. Minimum 3 clocks of tDAL (= tWR + tRP) is required because it need minimum 2 clocks for tWR and minimum 1 clock for tRP.
 $tDAL = (tWR/tCK) + (tRP/tCK)$: for each of the terms above, if not already an integer, round to the next higher integer.

6.4 Test Conditions

Table 6.8 Test Conditions

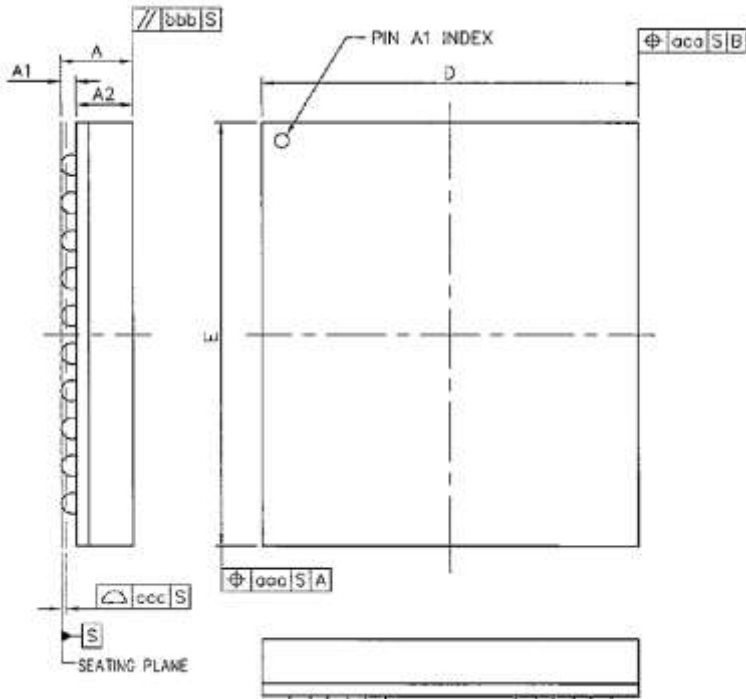
| Parameter | Symbol | Value | Unit | Note |
|---|----------------------|----------------------|------|------|
| Input high voltage | V _{IH} (AC) | 0.8 x VDDQ | V | 1 |
| Input low voltage | V _{IL} (AC) | 0.2 x VDDQ | V | 1 |
| Input differential voltage, CK and CK# inputs | V _{ID} (AC) | 1.4 | V | 1 |
| Input differential cross point voltage, CK and CK# inputs | V _{IX} (AC) | VDDQ/2 with VDD=VDDQ | V | |
| Input signal slew rate | SLEW | 1 | V/ns | 1 |
| Output load | CL | 15 | pF | |

Note : 1. VDD = VDDQ.

Figure 6.1 Wave form and Timing reference

Figure 6.2 Output Load


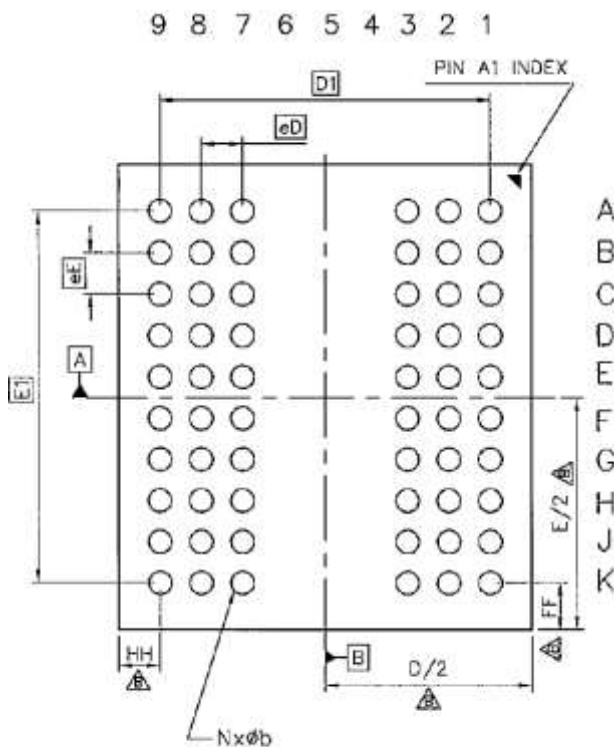
7. PACKAGE OUTLINE INFORMATION

7.1 60-Ball FBGA Package (8.0 x 9.0)



< TOP View >

| Symbol | Dimension (mm) | | |
|------------|----------------|-------|-------|
| | Min. | Typ. | Max. |
| A | - | - | 1.025 |
| A1 | 0.250 | 0.300 | 0.350 |
| b | 0.400 | 0.450 | 0.500 |
| D | 7.900 | 8.000 | 8.100 |
| E | 8.900 | 9.000 | 9.100 |
| D1 | 6.400 BSC. | | |
| E1 | 7.200 BSC. | | |
| eD | 0.800 BSC. | | |
| eE | 0.800 BSC. | | |
| aaa | 0.15 | | |
| bbb | - | - | 0.200 |
| ccc | - | - | 0.120 |
| ddd | - | - | 0.080 |
| N | 60 | | |
| FF | 0.90 | | |
| HH | 0.80 | | |



< Bottom View >

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