

# **BUK9604-40A**

# N-channel TrenchMOS logic level FET Rev. 2 — 7 February 2011

Product data sheet

#### 1. **Product profile**

## 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

#### 1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

## 1.3 Applications

- 12 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$		-	-	40	V
I <sub>D</sub>	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 1</u> ; see <u>Figure 3</u>	[1]	-	-	75	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	-	300	W
Static char	acteristics						
R <sub>DSon</sub>	drain-source on-state	$V_{GS} = 4.3 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$		-	3.7	5.9	mΩ
	resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$		-	2.9	4	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 11}}{\text{Figure 12}};$ see Figure 12		-	3.5	4.4	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 75 A; $V_{sup} \le 40$ V; $R_{GS}$ = 50 $\Omega$ ; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	1.6	J
Dynamic characteristics						
Q <sub>GD</sub>	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 32 \text{ V}; T_j = 25 \text{ °C};$ see Figure 13	-	56	-	nC

<sup>[1]</sup> Continuous current is limited by package.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain[1]	mb	D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

<sup>[1]</sup> It is not possible to make connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9604-40A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

# 4. Limiting values

Table 4. Limiting values

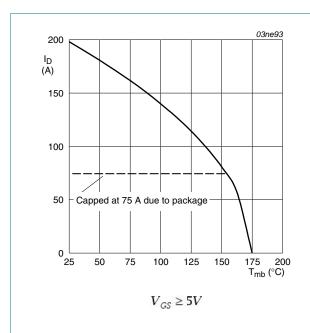
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	40	V
$V_{GS}$	gate-source voltage			-15	15	V
I <sub>D</sub>	drain current	$T_{mb} = 100  ^{\circ}C;  V_{GS} = 5  V;  see  \underline{Figure  1}$	<u>[1]</u>	-	75	Α
		$T_{mb}$ = 25 °C; $V_{GS}$ = 5 V; see <u>Figure 1</u> ;	<u>[1]</u>	-	75	Α
		see <u>Figure 3</u>	[2]	-	198	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; see Figure 3		-	794	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	300	W
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain	n diode					
Is	source current	T <sub>mb</sub> = 25 °C	[3]	-	198	Α
			[1]	-	75	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	794	Α
Avalanche r	uggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D = 75$ A; $V_{sup} \le 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped		-	1.6	J

<sup>[1]</sup> Continuous current is limited by package.

<sup>[2]</sup> Current is limited by power dissipation chip rating.

<sup>[3]</sup> Current is limited by power dissipation chip rating

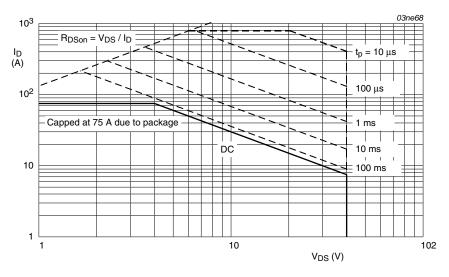


120
Pder (%)
80

40  $P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$ 

Fig 1. Normalized continuous drain current as a function of mounting base temperature

Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25$ °C;  $I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed circuit board; minimum footprint	-	50	-	K/W

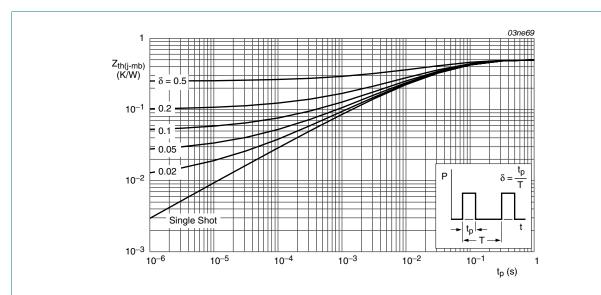


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V <sub>(BR)DSS</sub>	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	40	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	36	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ °C}$ ; see <u>Figure 10</u>	1	1.5	2	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 175$ °C; see <u>Figure 10</u>	0.5	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = -55$ °C; see <u>Figure 10</u>	-	-	2.3	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μΑ
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
R <sub>DSon</sub> drain-source on-state		$V_{GS} = 4.3 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	3.7	5.9	mΩ
	resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	2.9	4	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 °C;$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	8.3	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 11; see Figure 12	-	3.5	4.4	mΩ
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 5 \text{ V};$	-	128	-	nC
$Q_{GS}$	gate-source charge	T <sub>j</sub> = 25 °C; see <u>Figure 13</u>	-	13	-	nC
$Q_{GD}$	gate-drain charge		-	56	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	6200	8260	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 14</u>	-	1040	1250	pF
C <sub>rss</sub>	reverse transfer capacitance		-	680	940	pF
d(on)	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	62	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega$ ; $T_j = 25 °C$	-	309	-	ns
d(off)	turn-off delay time		-	365	-	ns
t <sub>f</sub>	fall time		-	306	-	ns
-D	internal drain inductance	from upper edge of drain mounting base to centre of die; $T_j = 25$ °C	-	2.5	-	nΗ
		from drain lead 6 mm from package to centre of die; $T_j = 25$ °C	-	4.5	-	nΗ
L <sub>S</sub>	internal source inductance	from source lead to source bond pad; $T_j = 25  ^{\circ}\text{C}$	-	7.5	-	nΗ

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drai	n diode					
V <sub>SD</sub>	source-drain voltage	$I_S = 40 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ °C}$ ; see <u>Figure 15</u>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	260	-	ns
Q <sub>r</sub>	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	531	-	nC

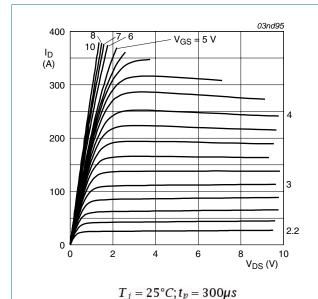


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

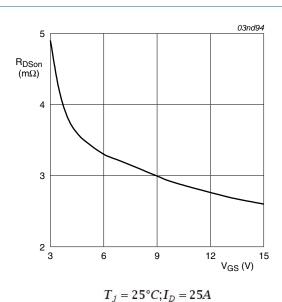


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

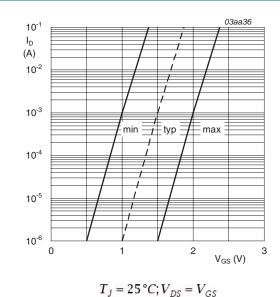


Fig 7. Sub-threshold drain current as a function of gate-source voltage

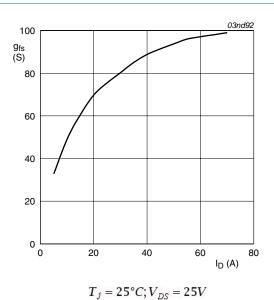


Fig 8. Forward transconductance as a function of drain current; typical values

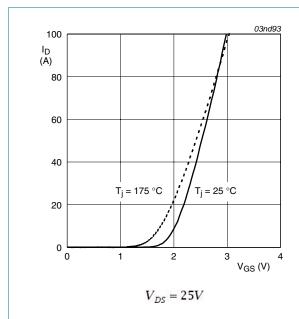


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

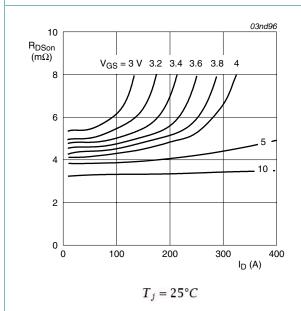
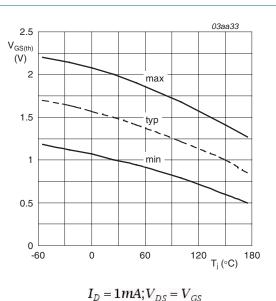


Fig 11. Drain-source on-state resistance as a function of drain current; typical values



 $I_D = IMA, V_{DS} = V_{GS}$ 

Fig 10. Gate-source threshold voltage as a function of junction temperature

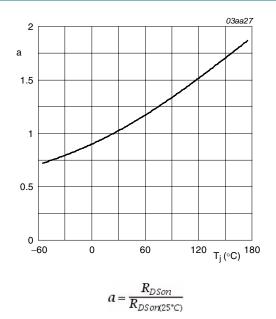


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

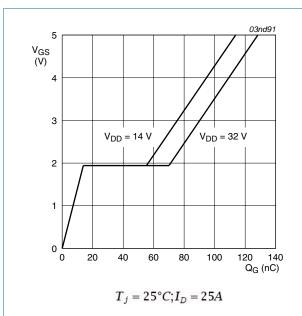
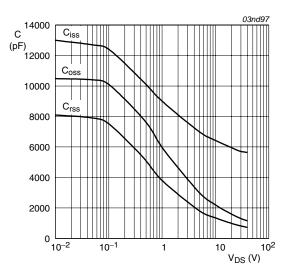


Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$ 

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

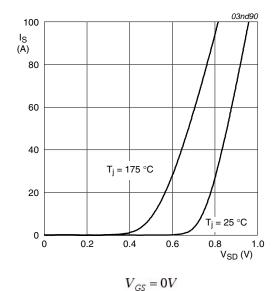


Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

## 7. Package outline

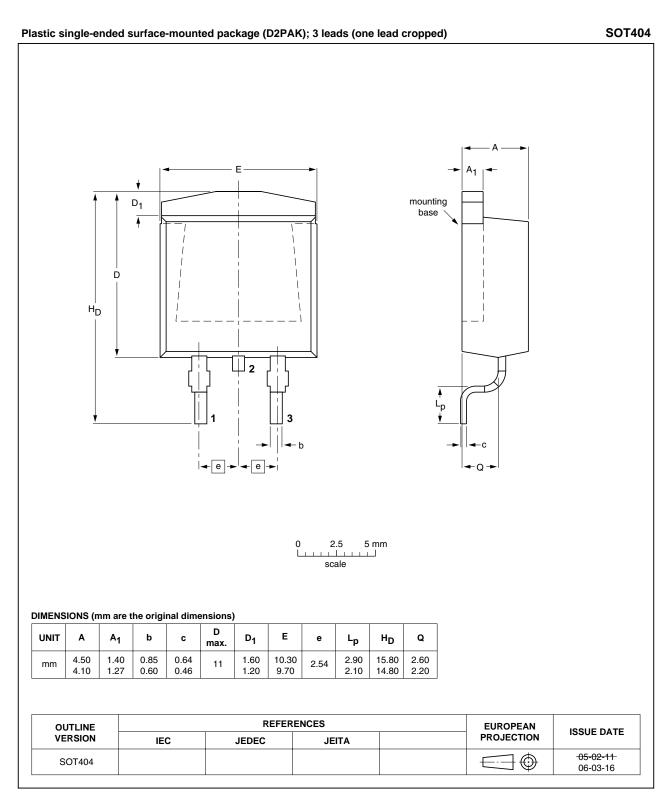


Fig 16. Package outline SOT404 (D2PAK)

# 8. Revision history

## Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BUK9504-40A v.2	20110207	Product data sheet	-	BUK95_96_9E04_40A-01	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>				
	<ul> <li>Legal texts</li> </ul>	have been adapted to the	new company nam	ne where appropriate.	
	<ul> <li>Type numb</li> </ul>	er BUK9504-40A separate	ed from data sheet I	BUK95_96_9E04_40A-01.	
BUK95_96_9E04_40A-01	20011024	Product specification	-	-	

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#### 9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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# **BUK9604-40A**

## **Nexperia**

N-channel TrenchMOS logic level FET

## 11. Contents

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многоканальный

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