

DESCRIPTION

The MP1907 is a high frequency, 100V half bridge N-channel power MOSFET driver. Its low side and high side driver channels are independently controlled and matched with less than 5ns in time delay. Under-voltage lock-out both high side and low side supplies force their outputs low in case of insufficient supply. Both outputs will remain low until a rising edge on either input is detected. The integrated bootstrap diode reduces external component count.

FEATURES

- Drives N-channel MOSFET half bridge
- 100V V_{BST} voltage range
- Input signal overlap protection
- On-chip bootstrap diode
- Typical 20ns propagation delay time
- Less than 5ns gate drive mismatch
- Drive 1nF load with 12ns/9ns rise/fall times with 12V VDD
- TTL compatible input
- Less than 150 μ A quiescent current
- Less than 5 μ A shutdown current
- UVLO for both high side and low side
- In 3 \times 3mm QFN10 Packages

APPLICATIONS

- Battery Powered Hand Tool
- Telecom half bridge power supplies
- Avionics DC-DC converters
- Active-clamp Forward Converters

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TYPICAL APPLICATION

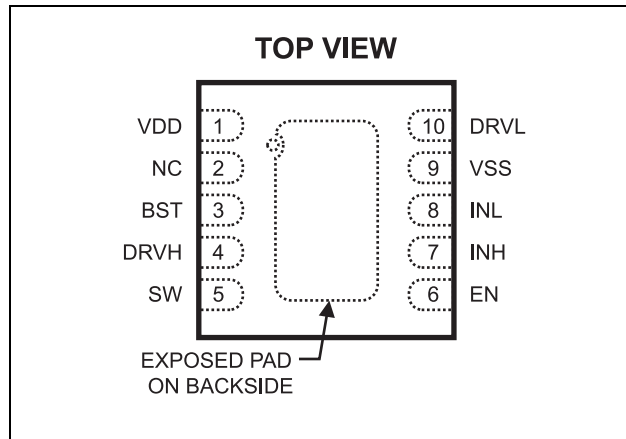


ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|--------------|------------------|-------------|
| MP1907GQ | QFN10 (3 x 3 mm) | ADE |

* For Tape & Reel, add suffix -Z (e.g. MP1907GQ-Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| | |
|---|----------------------------|
| Supply Voltage (V_{DD}) | -0.3V to +20V |
| SW Voltage (V_{SW}) | -5.0V to 105V |
| BST Voltage (V_{BST}) | -0.3V to 110V |
| BST to SW | -0.3V to +18V |
| DRVH to SW | -0.3V to (BST-SW) +0.3V |
| DRVL to VSS | -0.3V to (V_{DD} +0.3V) |
| All Other Pins | -0.3V to 20V |
| Continuous Power Dissipation ($T_A = +25^\circ\text{C}$) ⁽²⁾ | |
| QFN10 (3x3) | 2.5W |
| Junction Temperature | 150°C |
| Lead Temperature | 260°C |
| Storage Temperature | -65°C to +150°C |

Recommended Operating Conditions ⁽³⁾

| | |
|------------------------------------|-----------------------------|
| Supply Voltage (V_{DD}) | +4.5V to 18V ⁽⁴⁾ |
| SW Voltage (V_{SW}) | -1.0V to 100V |
| SW slew rate | <50V/nsec |
| Operating Junction Temp. (T_J) | -40°C to +125°C |

| Thermal Resistance ⁽⁵⁾ | θ_{JA} | θ_{JC} |
|-----------------------------------|---------------|---------------|
| QFN10 (3x3) | 50 | 12... °C/W |

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- 4.5V is only a typical value for minimum supply voltage at V_{DD} falling
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{BST} - V_{SW} = 12V$, $V_{SS} = V_{SW} = 0V$, $V_{EN} = 3.3V$, No load at DRVH and DRVL, $T_A = +25^\circ C$, unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---------------------------------------|------------|--|-----|------|-------------------|-----------|
| Supply Current | | | | | | |
| VDD Shutdown Current | I_{SHDN} | $V_{EN} = 0$, | | 0 | 1 | μA |
| VDD quiescent current | I_{DDQ} | $INL = INH = 0$ | | 80 | 100 | μA |
| VDD operating current | I_{DDO} | $fsw = 500kHz$ | | 2.8 | 3.5 | mA |
| Floating driver quiescent current | I_{BSTQ} | $INL = 0$, $INH = 0$ or 1 | | 55 | 70 | μA |
| Floating driver operating current | I_{BSTO} | $fsw = 500kHz$ | | 2.1 | 3 | mA |
| Leakage Current | I_{LK} | $BST = SW = 100V$ | | 0.05 | 1 | μA |
| Inputs | | | | | | |
| INL/INH High | | | 2.4 | | | V |
| INL/INH Low | | | | | 1 | V |
| INL/INH Hysteresis | | | | 0.6 | | V |
| INL/INH internal pull-down resistance | R_{IN} | | | 185 | | $k\Omega$ |
| Under Voltage Protection | | | | | | |
| VDD rising threshold | V_{DDR} | | 4.6 | 5.0 | 5.4 | V |
| VDD falling threshold | V_{DDF} | | 4.1 | 4.5 | 4.9 | V |
| (BST-SW) rising threshold | V_{BSTR} | | 4.6 | 5.0 | 5.4 | V |
| (BST-SW) falling threshold | V_{BSTF} | | 4.1 | 4.5 | 4.9 | V |
| EN Input Logic Low | | | | | 0.7 | V |
| EN Input Logic High | | | 1.5 | | | V |
| EN Hysteresis | | | | 100 | | mV |
| EN Input Current | I_{EN} | $V_{EN} = 2V$, $T_A = +25^\circ C$ | | 10 | | μA |
| | | $V_{EN} = 5V$, $T_A = -10^\circ C$ to $+70^\circ C$ | | | 35 ⁽⁶⁾ | μA |
| EN internal pull-down resistance | R_{EN} | | | 200 | | $k\Omega$ |
| Bootstrap Diode | | | | | | |
| Bootstrap diode VF @ 100uA | V_{F1} | | | 0.55 | | V |
| Bootstrap diode VF @ 100mA | V_{F2} | | | 1 | | V |
| Bootstrap diode dynamic R | R_D | @ 100mA | | 2.7 | | Ω |
| Low Side Gate Driver | | | | | | |
| Low level output voltage | V_{OLL} | $I_O = 100mA$ | | 0.15 | 0.22 | V |
| High level output voltage to rail | V_{OHL} | $I_O = -100mA$ | | 0.45 | 0.6 | V |
| Peak pull-up current ⁽⁷⁾ | I_{OHL} | $V_{DRVL} = 0V$, $V_{DD} = 4.5V$ ⁽⁸⁾ | | 0.15 | | A |
| | | $V_{DRVL} = 0V$, $V_{DD} = 12V$ | | 1.5 | | A |
| | | $V_{DRVL} = 0V$, $V_{DD} = 16V$ | | 2.5 | | A |
| Peak pull-down current ⁽⁷⁾ | I_{OLL} | $V_{DRVL} = V_{DD} = 4.5V$ ⁽⁸⁾ | | 0.25 | | A |
| | | $V_{DRVL} = V_{DD} = 12V$ | | 2.5 | | A |
| | | $V_{DRVL} = V_{DD} = 16V$ | | 3.5 | | A |
| Floating Gate Driver | | | | | | |
| Low level output voltage | V_{OLH} | $I_O = 100mA$ | | 0.15 | 0.22 | V |

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = V_{BST}-V_{SW}=12V$, $V_{SS}=V_{SW} = 0V$, $V_{EN}=3.3V$, No load at DRVH and DRVL, $T_A= +25^{\circ}C$, unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|------------|---|-----|-------------------|-------------------|-------|
| High level output voltage to rail | V_{OHH} | $I_O=-100mA$ | | 0.45 | 0.6 | V |
| Peak pull-up current ⁽⁷⁾ | I_{OHH} | $V_{DRVH}=0V$, $V_{BST} - V_{SW} =5V$ ⁽⁹⁾ | | 0.25 | | A |
| | | $V_{DRVH}=0V$, $V_{DD}=12V$ | | 1.5 | | A |
| | | $V_{DRVH}=0V$, $V_{DD}=16V$ | | 2.5 | | A |
| Peak pull-down current ⁽⁷⁾ | I_{OLH} | $V_{DRVH}=V_{BST} - V_{SW} =5V$ ⁽⁹⁾ | | 0.65 | | A |
| | | $V_{DRVH}=V_{DD}=12V$ | | 2.5 | | A |
| | | $V_{DRVH}=V_{DD}=16V$ | | 3.5 | | A |
| Switching Spec. --- Low Side Gate Driver | | | | | | |
| Turn-off propagation delay INL falling to DRVL falling | T_{DLFF} | | | 20 | | ns |
| Turn-on propagation delay INL rising to DRVL rising | T_{DLRR} | | | 20 | | ns |
| DRVL rise time | | $C_L=1nF$ | | 12 | | ns |
| DRVL fall time | | $C_L=1nF$ | | 9 | | ns |
| Switching Spec. --- Floating Gate Driver | | | | | | |
| Turn-off propagation delay INL falling to DRVH falling | T_{DHFF} | | | 20 | | ns |
| Turn-on propagation delay INL rising to DRVH rising | T_{DHRR} | | | 18 | | ns |
| DRVH rise time | | $C_L=1nF$ | | 12 | | ns |
| DRVH fall time | | $C_L=1nF$ | | 9 | | ns |
| Switching Spec. --- Matching | | | | | | |
| Floating driver turn-off to low side drive turn-on | T_{MON} | | | 1 | 5 | ns |
| Low side driver turn-off to floating driver turn-on | T_{MOFF} | | | 1 | 5 | ns |
| Minimum input pulse width that changes the output | T_{PW} | | | | 50 ⁽⁷⁾ | ns |
| Bootstrap diode turn-on or turn-off time | T_{BS} | | | 10 ⁽⁷⁾ | | ns |

Note:

- 6) Based on characterization data. Not production tested.
- 7) Guaranteed by design.
- 8) After startup VDD fall to 4.5V
- 9) After startup VBST- VSW fall to 5V


Figure 1—Timing Diagram

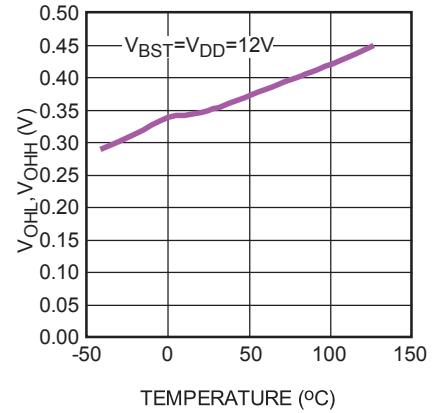
PIN FUNCTIONS

| Package Pin # | Name | Description |
|---------------|---------------------|---|
| 1 | VDD | Supply input. This pin supplies power to all the internal circuitry. A decoupling capacitor to ground must be placed close to this pin to ensure stable and clean supply. |
| 2 | NC | No Connection. |
| 3 | BST | Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin. |
| 4 | DRVH | Floating driver output. |
| 5 | SW | Switching node. |
| 6 | EN | On/off Control. |
| 7 | INH | Control signal input for the floating driver. |
| 8 | INL | Control signal input for the low side driver. |
| 9 | VSS, Exposed Pad | Chip ground. Connect to Exposed pad to VSS for proper thermal operation. |
| 10 | DRVL | Low side driver output. |

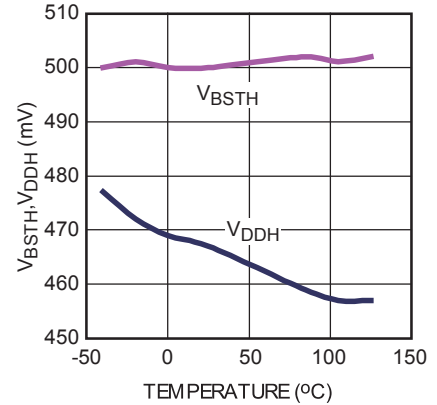
TYPICAL PERFORMANCE CHARACTERISTICS
 $V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = +25^\circ C$, unless otherwise noted.

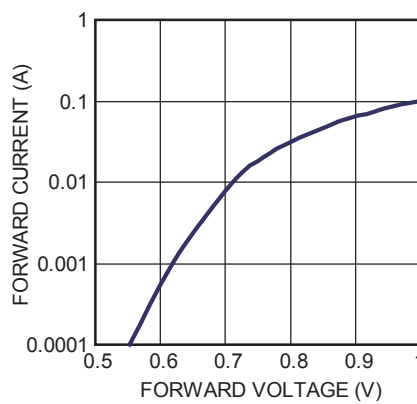
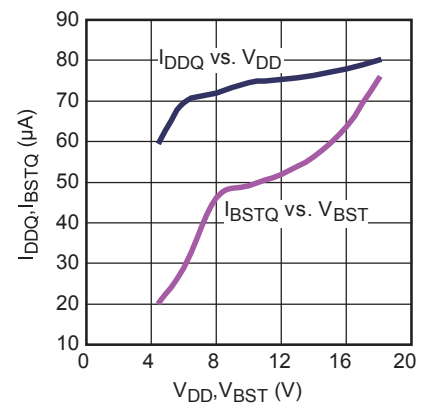
 I_{DDO} Operation Current vs. Frequency

 I_{BSTO} Operation Current vs. Frequency

High Level Output Voltage vs. Temperature

Low Level Output Voltage vs. Temperature

Undervoltage Lockout Threshold vs. Temperature

Undervoltage Lockout Hysteresis vs. Temperature

Propagation Delay vs. Temperature

Bootstrap Diode I-V Characteristics

Quiescent Current vs. Voltage


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

Peak Current vs. V_{DD} Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = +25^\circ C$, unless otherwise noted.

Turn-on Propagation Delay

Turn-on Propagation Delay

Turn-off Protection Delay

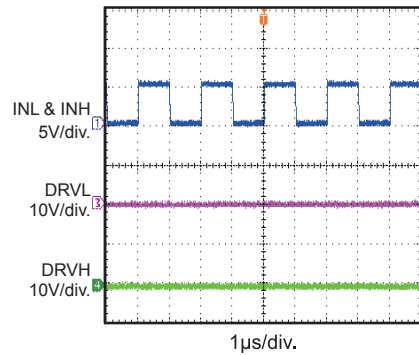
Turn-off Protection Delay

Drive Rise Time (1nF Load)

Drive Rise Time (1nF Load)

Drive Fall Time (1nF Load)

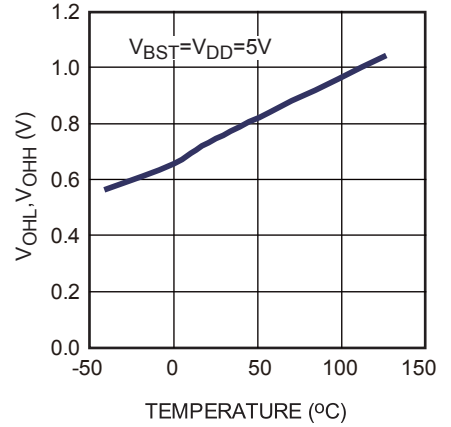
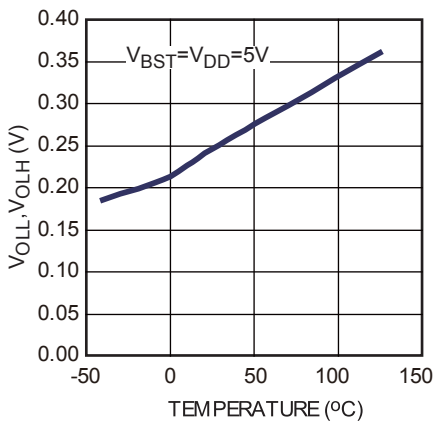
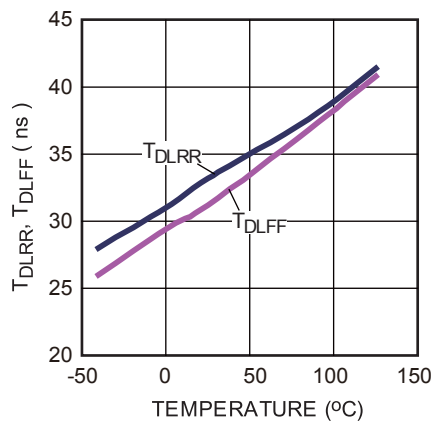
Drive Fall Time (1nF Load)

Input Signal Overlap Protection


TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{DD} = 5V$, after startup V_{DD} falls to 5V, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

 I_{DDO} Operation Current vs. Frequency

 I_{BSTO} Operation Current vs. Frequency

High Level Output Voltage vs. Temperature

Low Level Output Voltage vs. Temperature

Propagation Delay vs. Temperature


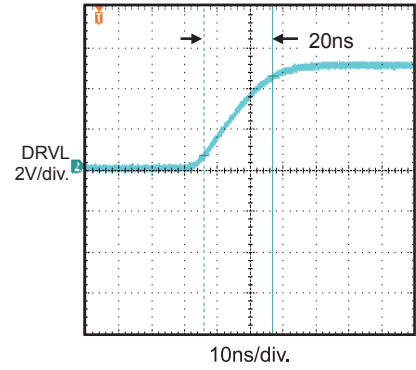
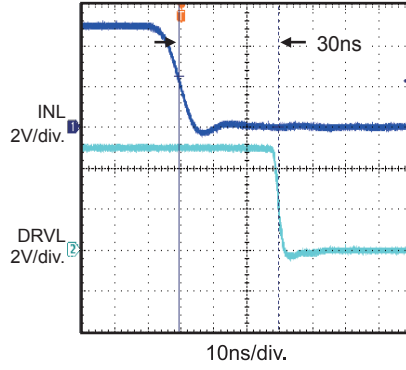
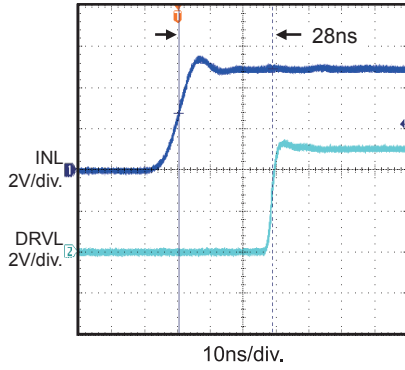
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 5V$, after startup V_{DD} falls to 5V, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

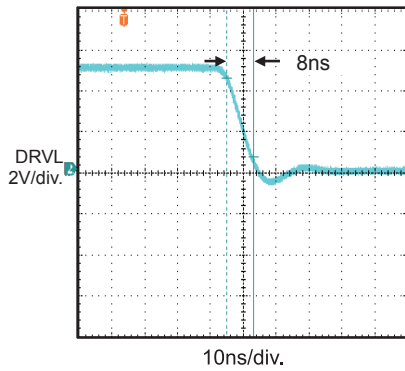
Turn-on Propagation Delay

Turn-off Propagation Delay

Drive Rise Time (1nF Load)



Drive Fall Time (1nF Load)



BLOCK DIAGRAM



Figure 2—Function Block Diagram

OPERATION

Switch Shoot-through Protection

The input signals of INH and INL are controlled independently. Input shoot-through protection circuitry is implemented to prevent shoot-through between the HSFET and LSFET outputs. Only one of the FET drivers can be ON at one time. If both INH and INL are high at the same time, both HSFET and LSFET will be OFF.

Under Voltage Lock Out

When VDD or BST goes below their respective UVLO thresholds, both DRVH and DRVL outputs will go low to turn off both FETs. Once VDD rises above the UVLO threshold, both DRVH and DRVL will stay low until a rising edge is detected on either INH or INL.

The truth table in Table 1 details the operation of the HSFET and LSFET under different INH, INL and UVLO conditions

Table1 States of Driver Output under different conditions

| EN | BST-SW Voltage | V _{DD} Voltage | INH | INL | DRVH | DRVL | UVLO Latch status | Operating Condition | |
|----|----------------|-------------------------|------------------|--------|--------|-----------------|-----------------------|-------------------------------|------------------------------|
| 0 | X | X | X | X | Open | 200kΩ pull down | X | X | |
| 1 | X | X | 0 | 0 | 0 | 0 | X | Normal Operation | |
| | X | X | 1 | 1 | 0 | 0 | X | | |
| | X | Above UVLO | 0 | 1 | 0 | 1 | Normal | | |
| | Above UVLO | Above UVLO | 1 | 0 | 1 | 0 | Normal | | |
| | | Falls below UVLO | Above UVLO | X | X | 0 | 0 | Normal to Tripped | Normal-to-Tripped Transition |
| | | Above UVLO | Falls below UVLO | X | X | 0 | 0 | Normal to Tripped | |
| | | X | Above UVLO | 0 or 1 | 0 or 1 | 0 | 0 | Tripped | When UVLO latch is tripped. |
| | | X | Below UVLO | X | X | 0 | 0 | Tripped | |
| | | X | Above UVLO | 0 to 1 | 0 to 1 | 0 | 0 | Tripped, Reset by INL & INH | Tripped to Normal Transition |
| | | X | Above UVLO | 1 to 0 | 1 | 0 | 0 to 1 | Tripped, Reset by INH Falling | |
| | | Below UVLO | Above UVLO | 1 | 1 to 0 | 0 | 0 | Tripped, Reset by INL Falling | |
| | | Above UVLO | Above UVLO | 1 | 1 to 0 | 0 to 1 | 0 | Tripped, Reset by INL Falling | |
| | | Below UVLO | Above UVLO | 0 | 0 to 1 | 0 | 0 to 1 | Tripped, Reset by INL | |
| | Below UVLO | Above UVLO | 0 to 1 | 0 | 0 | 0 | Tripped, Reset by INH | | |
| | Above UVLO | Above UVLO | 0 to 1 | 0 | 0 to 1 | 0 | Tripped, Reset by INH | | |

Note: x = Don't Care.

APPLICATION INFORMATION

Reference Design Circuits

Half Bridge Motor Driver

In a half-bridge converter topology, the MOSFETs are driven alternately with some dead time. Therefore, INH and INL are driven with

alternating signals from the PWM controller. The input voltage can be up to 100V in this application.

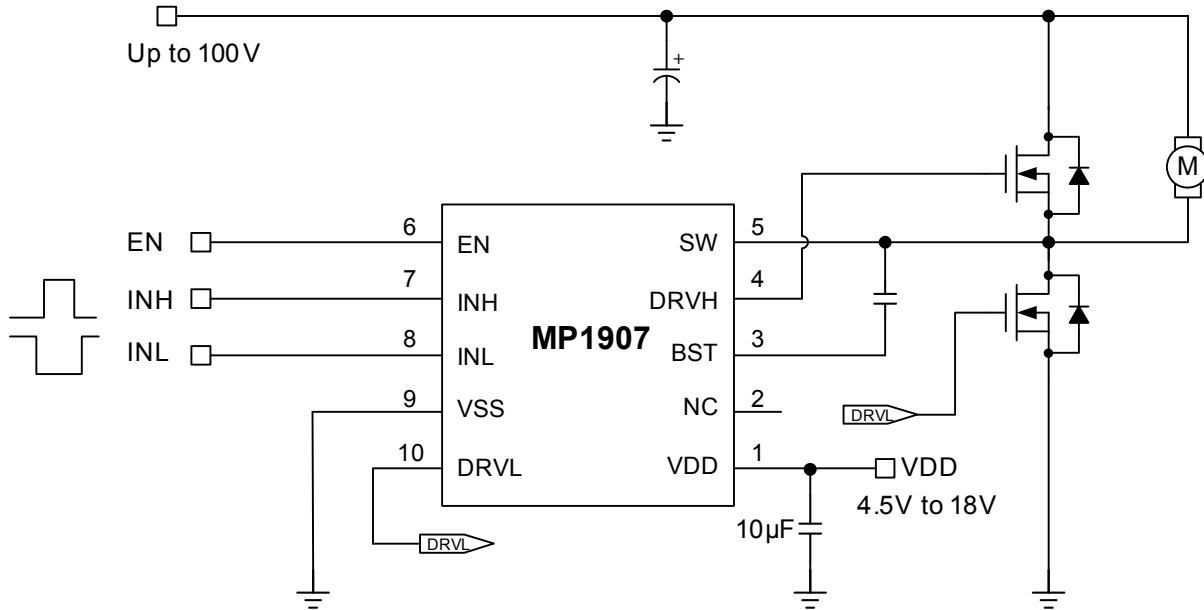


Figure 3—Half-Bridge Motor Driver

Active-Clamp Forward Converter

In active-clamp forward converter topology, the MOSFETs are driven alternately. The high-side MOSFET, along with capacitor C_{reset} , is used to reset the power transformer in a lossless manner.

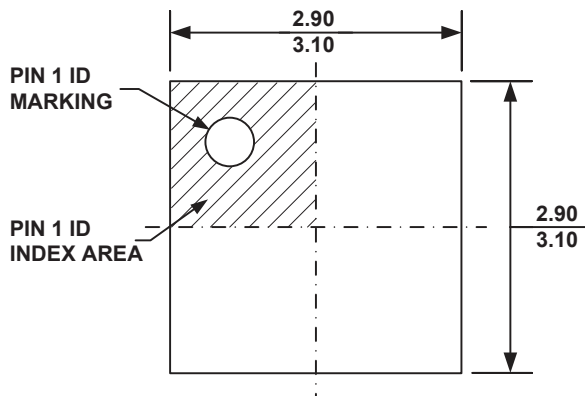
This topology lends itself well to run at duty cycles exceeding 50%. For these reasons, the input voltage may not be able to run at 100V for this application.



Figure 4—Active-clamp Forward Converter

PACKAGE INFORMATION

QFN10 (3 × 3 mm)



TOP VIEW



BOTTOM VIEW

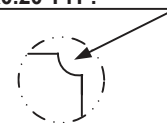


SIDE VIEW

PIN 1 ID OPTION A
R0.20 TYP.



PIN 1 ID OPTION B
R0.20 TYP.



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
- 5) DRAWING IS NOT TO SCALE.

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Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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