

74AHC595-Q100; 74AHCT595-Q100

8-bit serial-in/serial-out or parallel-out shift register with
output latches

Rev. 2 — 26 May 2020

Product data sheet

1. General description

The 74AHC595-Q100; 74AHCT595-Q100 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset MR input. A LOW on MR will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. The 74AHCT595-Q100 features TTL compatible inputs. Both 74AHC595-Q100 and 74AHCT595-Q100 inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 5.5 V
- Balanced propagation delays
- All inputs have Schmitt trigger action
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Input levels:
 - The 74AHC595-Q100 operates with CMOS input levels
 - The 74AHCT595-Q100 operates with TTL input levels
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0 Ω)
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC595D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT595D-Q100				
74AHC595PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHCT595PW-Q100				
74AHC595BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AHCT595BQ-Q100				

5. Functional diagram

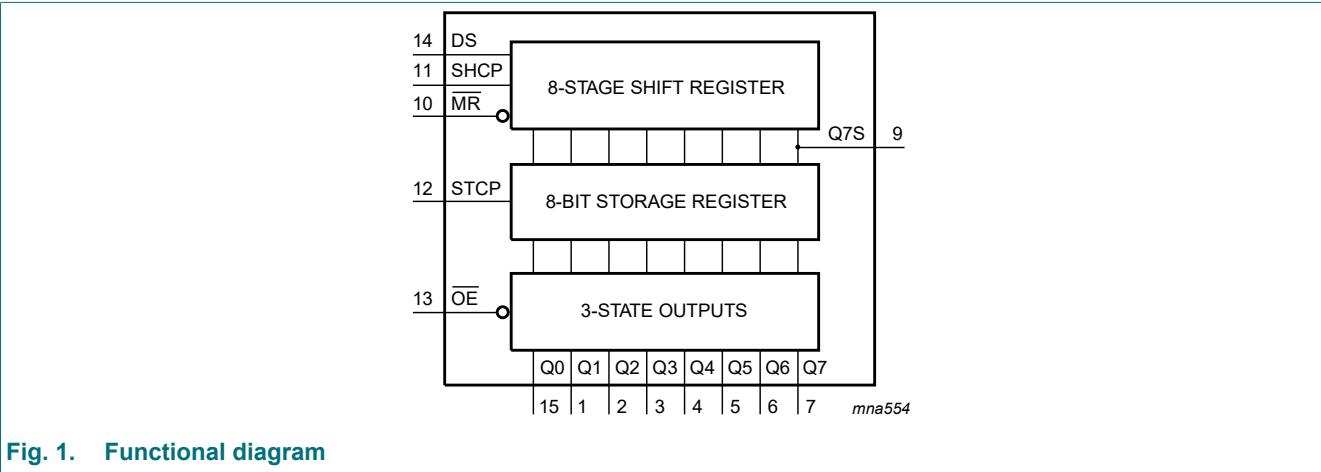


Fig. 1. Functional diagram

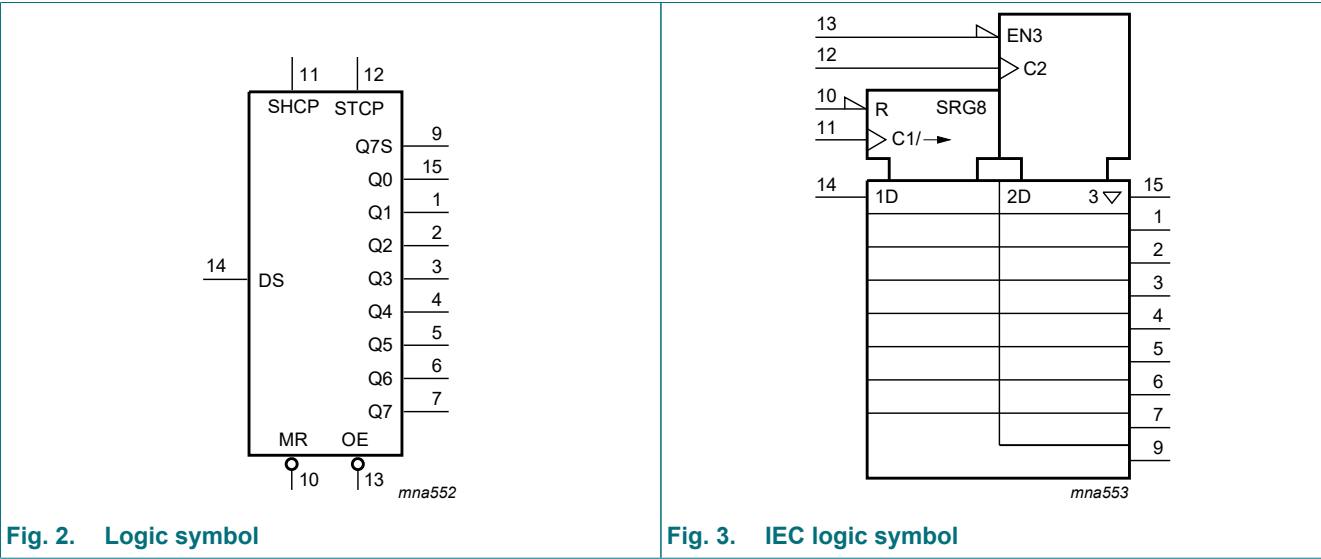
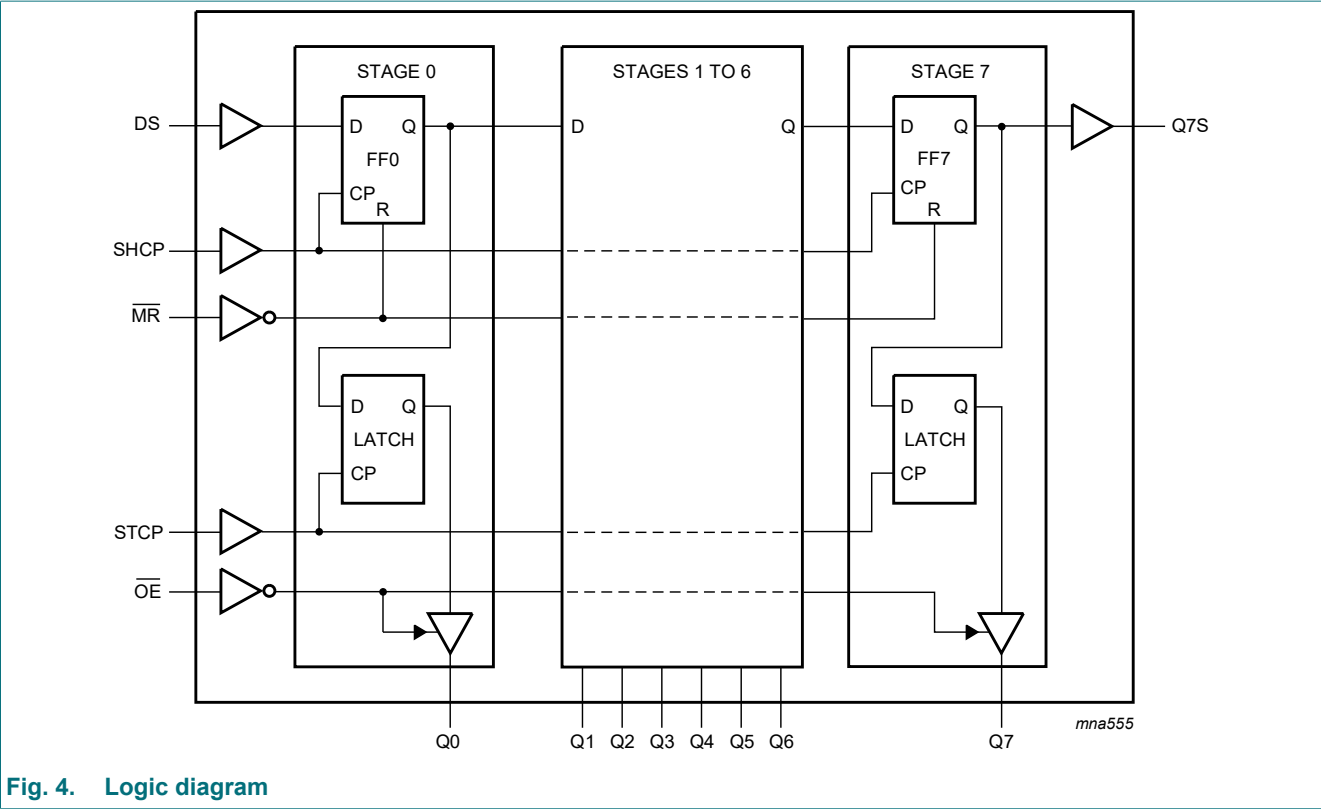


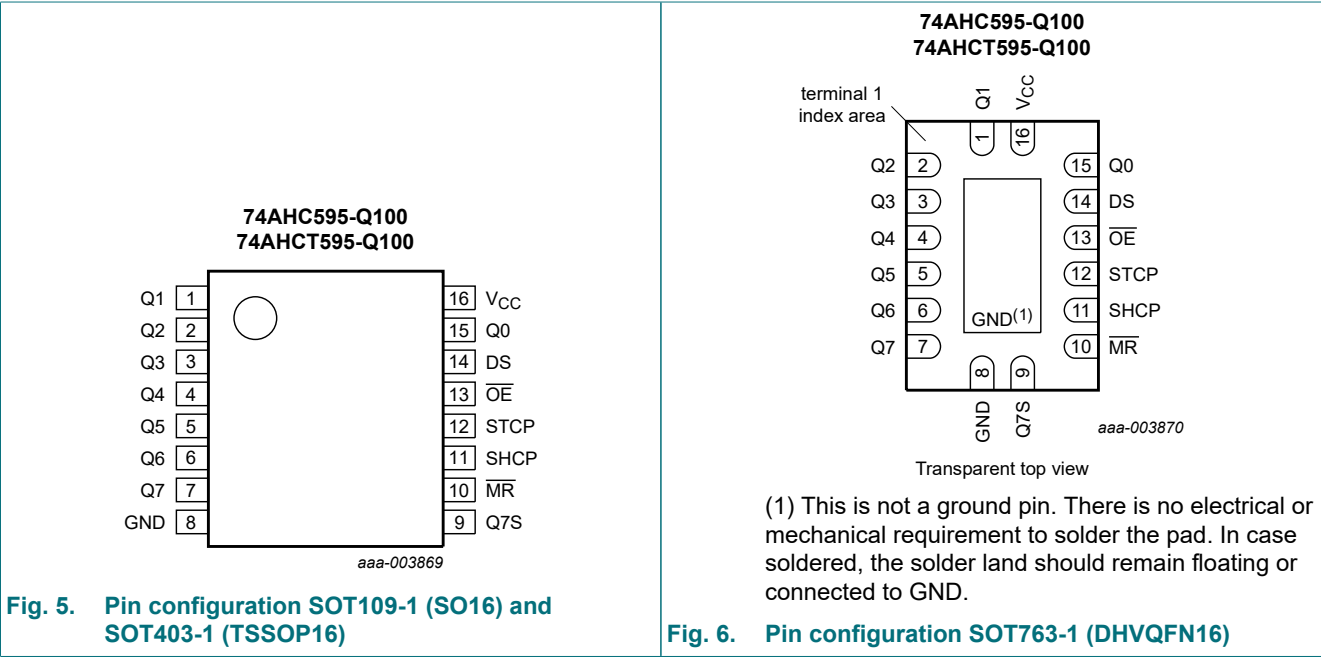
Fig. 2. Logic symbol

Fig. 3. IEC logic symbol



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
OE	13	output enable input (active LOW)
DS	14	serial data input
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage state;

L = LOW voltage state;

↑ = LOW-to-HIGH transition;

X = don't care;

NC = no change;

Z = high-impedance OFF-state.

Control				Input	Output		Function
SHCP	STCP	OE	MR	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on MR only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

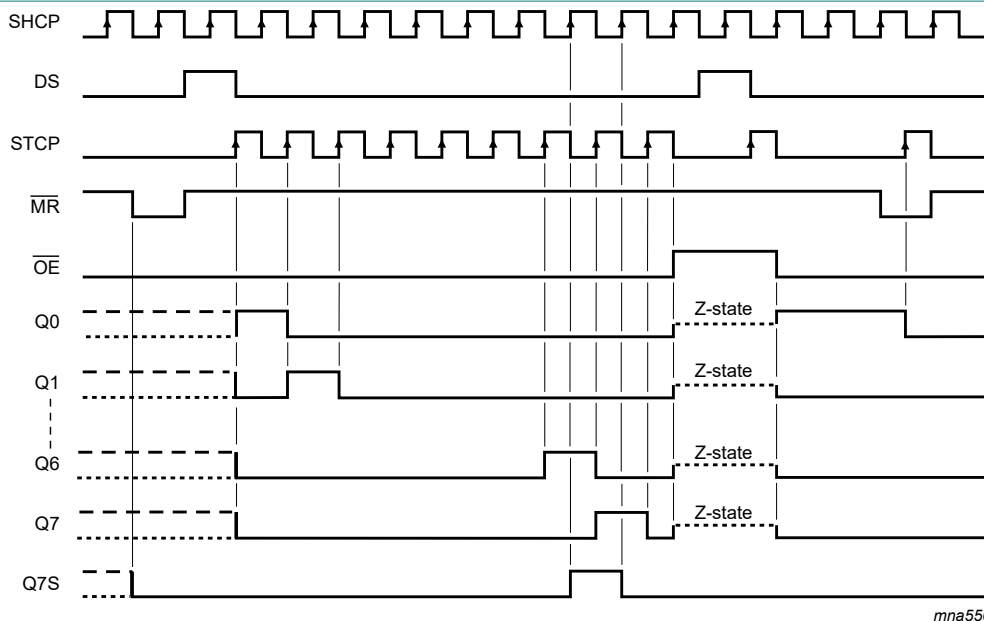


Fig. 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-25	+25	mA
I_{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	74AHC595-Q100			74AHCT595-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.0 V to 3.6 V	-	-	100	-	-	-	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC595-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
C _I	input capacitance		-	3	10	-	10	-	10	pF

8-bit serial-in/serial-out or parallel-out shift register with output latches

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT595-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	3	10	-	10	-	10	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 13.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHC595-Q100										
t _{pd}	propagation delay	SHCP to Q7S; see Fig. 8 [2]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.7	13.0	1.0	15.0	1.0	16.5	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	7.7	16.5	1.0	18.5	1.0	20.1	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.0	8.2	1.0	9.4	1.0	10.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.4	10.0	1.0	11.4	1.0	12.5	ns
		STCP to Qn; see Fig. 9 [2]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.9	11.9	1.0	13.5	1.0	15.0	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	7.7	15.4	1.0	17.0	1.0	18.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.2	7.4	1.0	8.5	1.0	9.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.5	9.0	1.0	10.5	1.0	11.5	ns

8-bit serial-in/serial-out or parallel-out shift register with output latches

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Fig. 11								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	5.9	12.8	1.0	13.7	1.0	15.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	7.4	16.3	1.0	17.2	1.0	18.7	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	4.4	8.0	1.0	9.1	1.0	10.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	5.6	10.0	1.0	11.1	1.0	12.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 12 [3]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	5.6	11.5	1.0	13.5	1.0	15.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	7.4	15.0	1.0	17.0	1.0	18.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	4.0	8.6	1.0	10.0	1.0	11.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	5.3	10.6	1.0	12.0	1.0	13.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 12 [4]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	5.4	11.0	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	8.7	15.7	1.0	16.2	1.0	17.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	3.8	8.0	1.0	9.5	1.0	10.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f_{max}	maximum frequency	SHCP or STCP; see Fig. 8 and Fig. 9								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	80	125	-	60	-	40	-	MHz
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	130	170	-	110	-	90	-	MHz
t_W	pulse width	SHCP HIGH or LOW; see Fig. 8								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Fig. 9								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$\overline{MR}$ LOW; see Fig. 11								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	DS to SHCP; see Fig. 10								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.5	-	-	3.5	-	3.5	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Fig. 9								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	8.5	-	-	8.5	-	8.5	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
t_h	hold time	DS to SHCP; see Fig. 10								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	-	1.5	-	1.5	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	2.0	-	2.0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Fig. 11								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.0	-	-	3.0	-	3.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.5	-	-	2.5	-	2.5	-	ns
C_{PD}	power dissipation capacitance	$f_i = 1\text{ MHz}; V_I = \text{GND to }V_{CC}$ [5] [6]	-	180	-	-	-	-	-	pF

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Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHCT595-Q100										
t _{pd}	propagation delay	SHCP to Q7S; see Fig. 8 [2]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.8	8.2	1.0	9.0	1.0	10.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.2	10.0	1.0	11.0	1.0	12.0	ns
		STCP to Qn; see Fig. 9 [2]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.0	7.4	1.0	8.5	1.0	9.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.3	9.0	1.0	10.5	1.0	11.5	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Q7S; see Fig. 11								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.6	8.2	1.0	9.5	1.0	10.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.8	10.5	1.0	11.5	1.0	12.5	ns
t _{en}	enable time	OE to Qn; see Fig. 12 [3]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.8	9.0	1.0	11.0	1.0	12.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	6.2	11.6	1.0	13.0	1.0	14.5	ns
t _{dis}	disable time	OE to Qn; see Fig. 12 [4]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.6	6.9	1.0	8.0	1.0	9.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f _{max}	maximum frequency	SHCP and STCP; V _{CC} = 4.5 V to 5.5 V; see Fig. 8 and Fig. 9	130	170	-	110	-	90	-	MHz
t _W	pulse width	SHCP HIGH or LOW; V _{CC} = 4.5 V to 5.5 V; see Fig. 8	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; V _{CC} = 4.5 V to 5.5 V; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; V _{CC} = 4.5 V to 5.5 V; see Fig. 11	5.0	-	-	5.0	-	5.0	-	ns
t _{su}	set-up time	DS to SHCP; V _{CC} = 4.5 V to 5.5 V; see Fig. 10	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; V _{CC} = 4.5 V to 5.5 V; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
t _h	hold time	DS to SHCP; V _{CC} = 4.5 V to 5.5 V; see Fig. 10	2.0	-	-	2.0	-	2.0	-	ns
t _{rec}	recovery time	MR to SHCP; V _{CC} = 4.5 V to 5.5 V; see Fig. 11	3.0	-	-	3.0	-	3.0	-	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [5] [6]	-	190	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

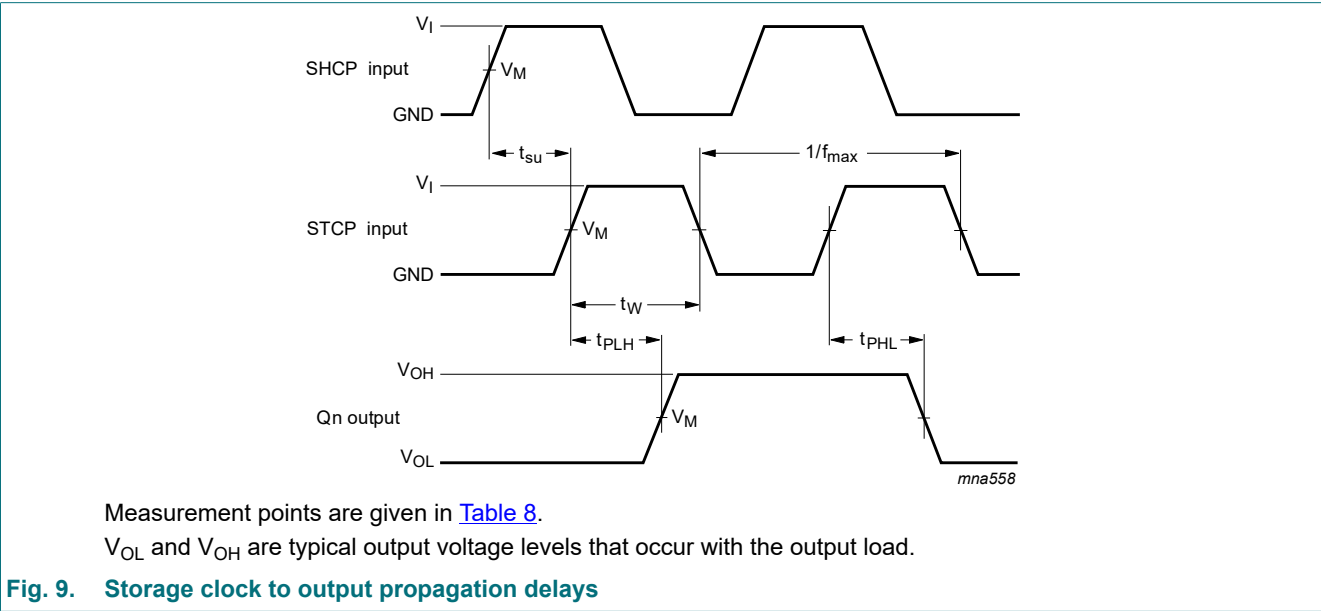
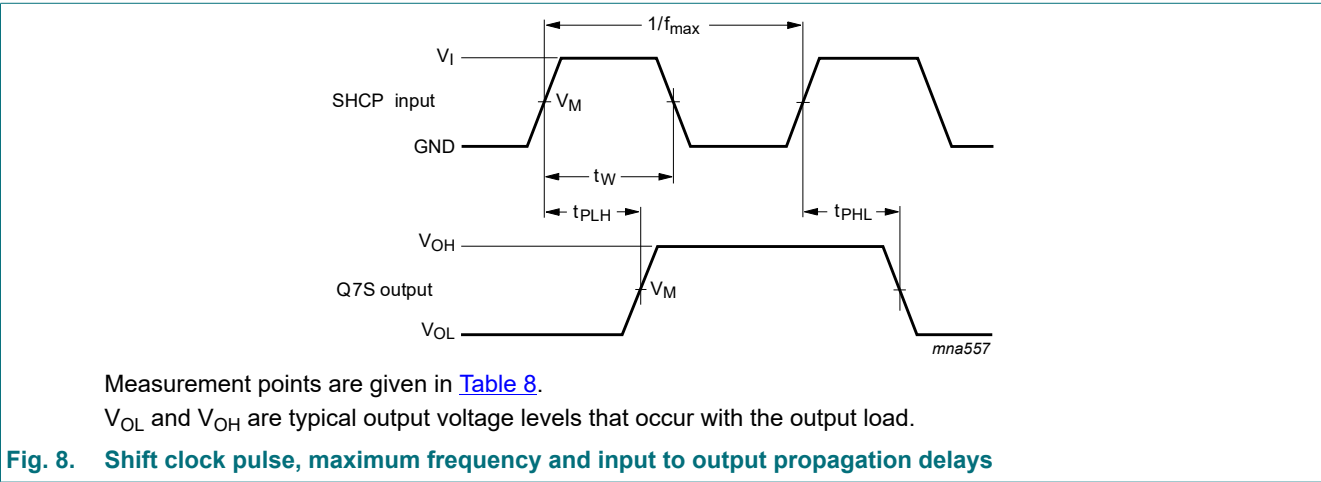
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

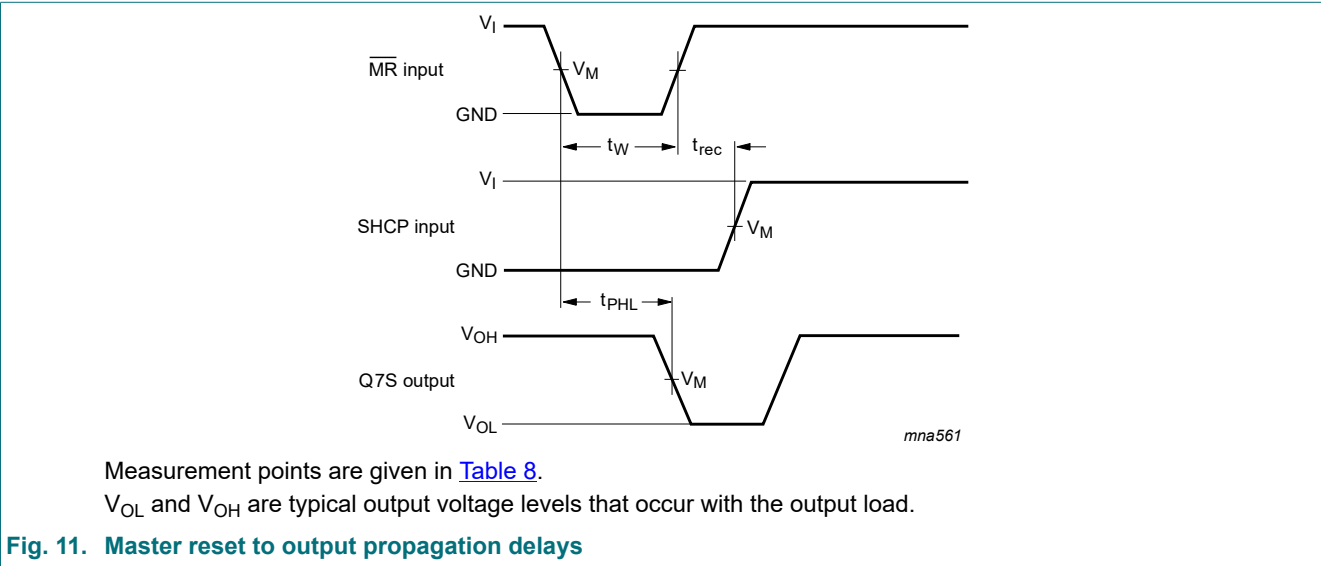
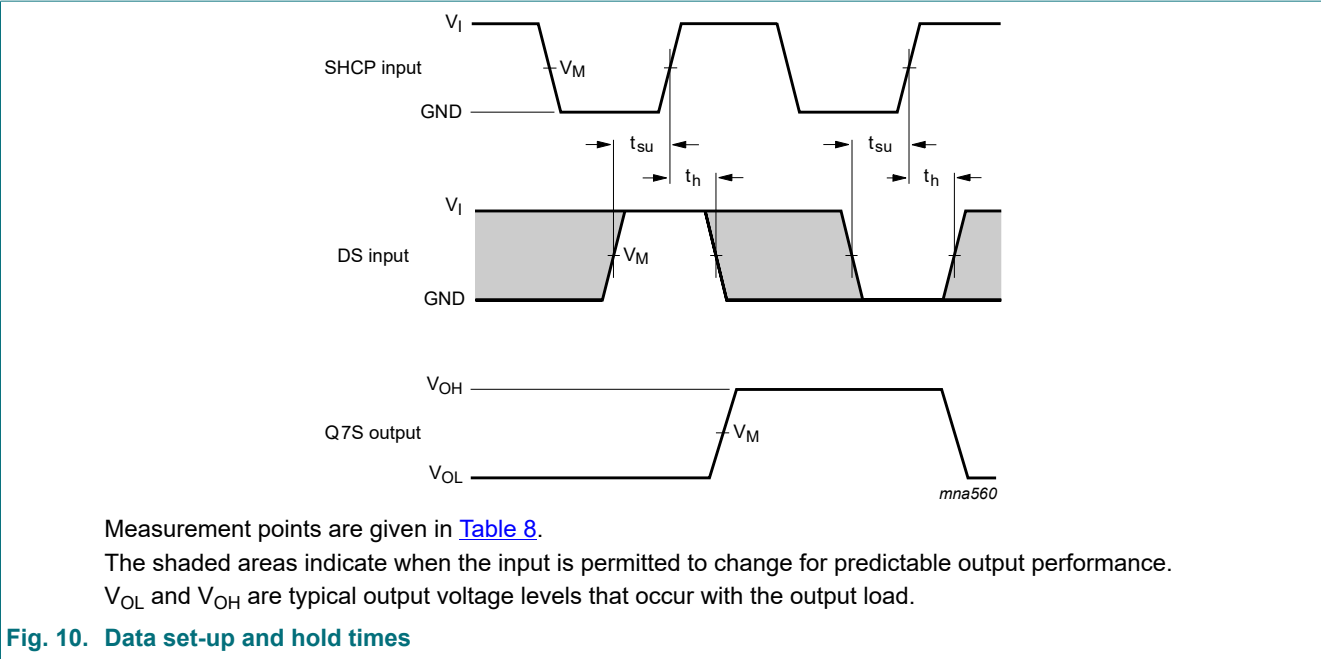
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

[6] All 9 outputs switching.

11.1. Waveforms and test circuit





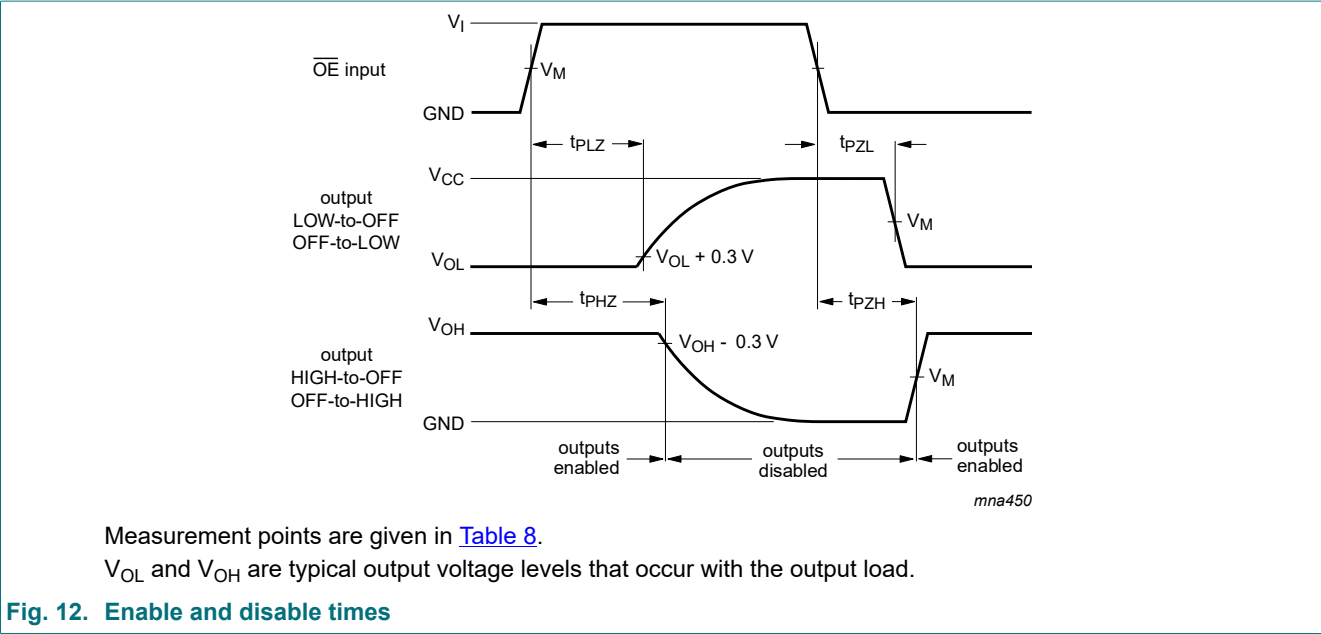


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC595-Q100	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT595-Q100	1.5 V	$0.5V_{CC}$

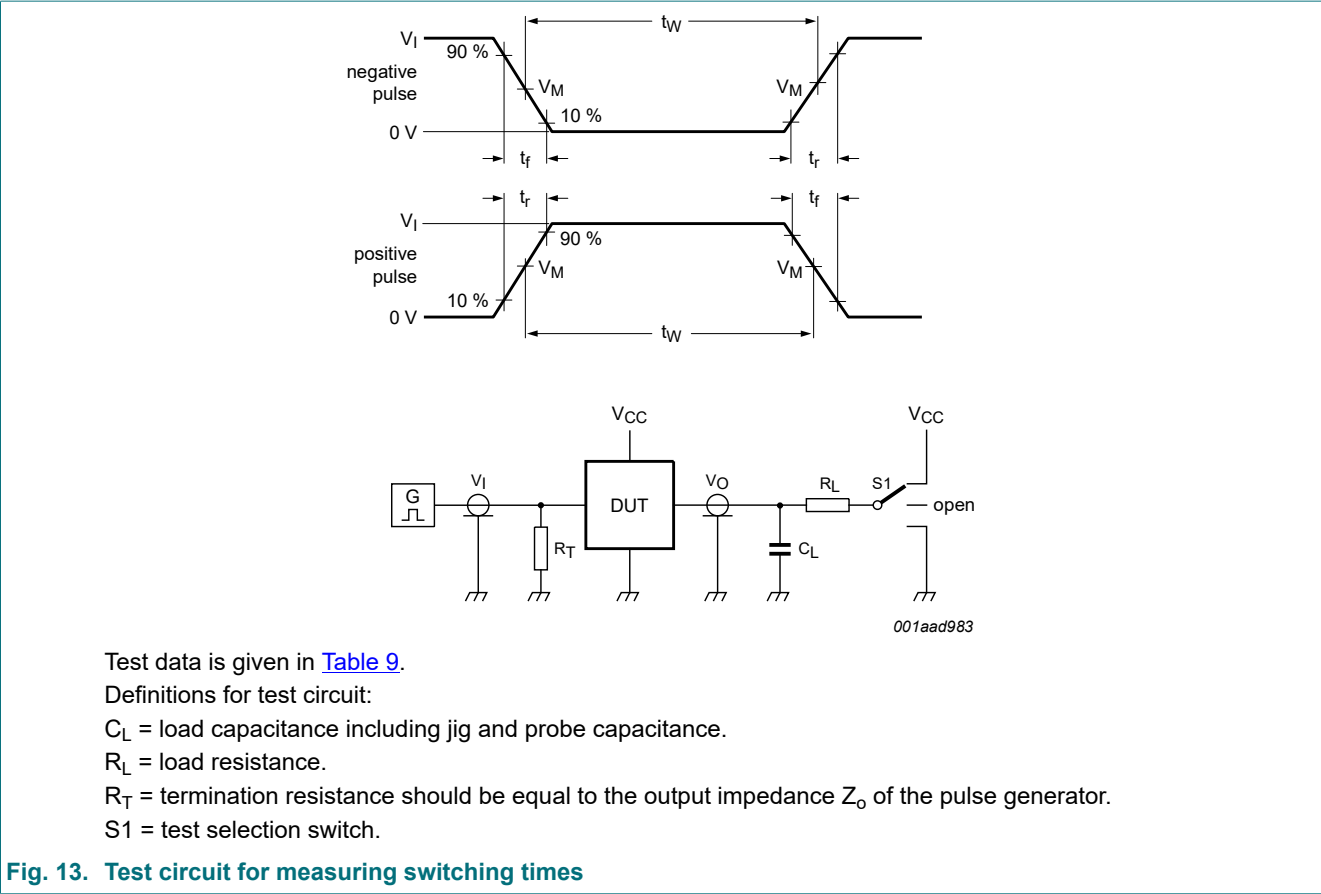


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC595-Q100	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74AHCT595-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

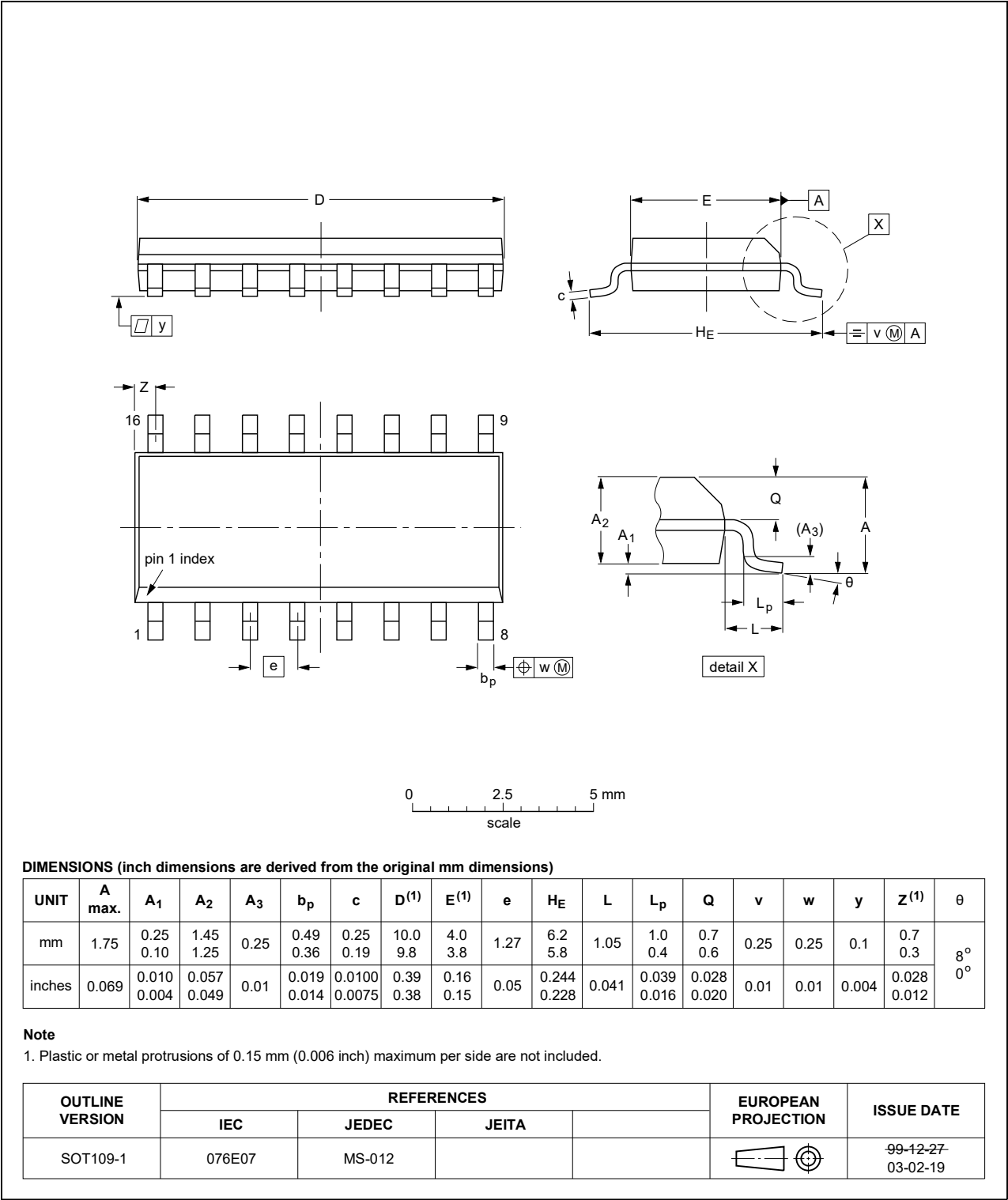


Fig. 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

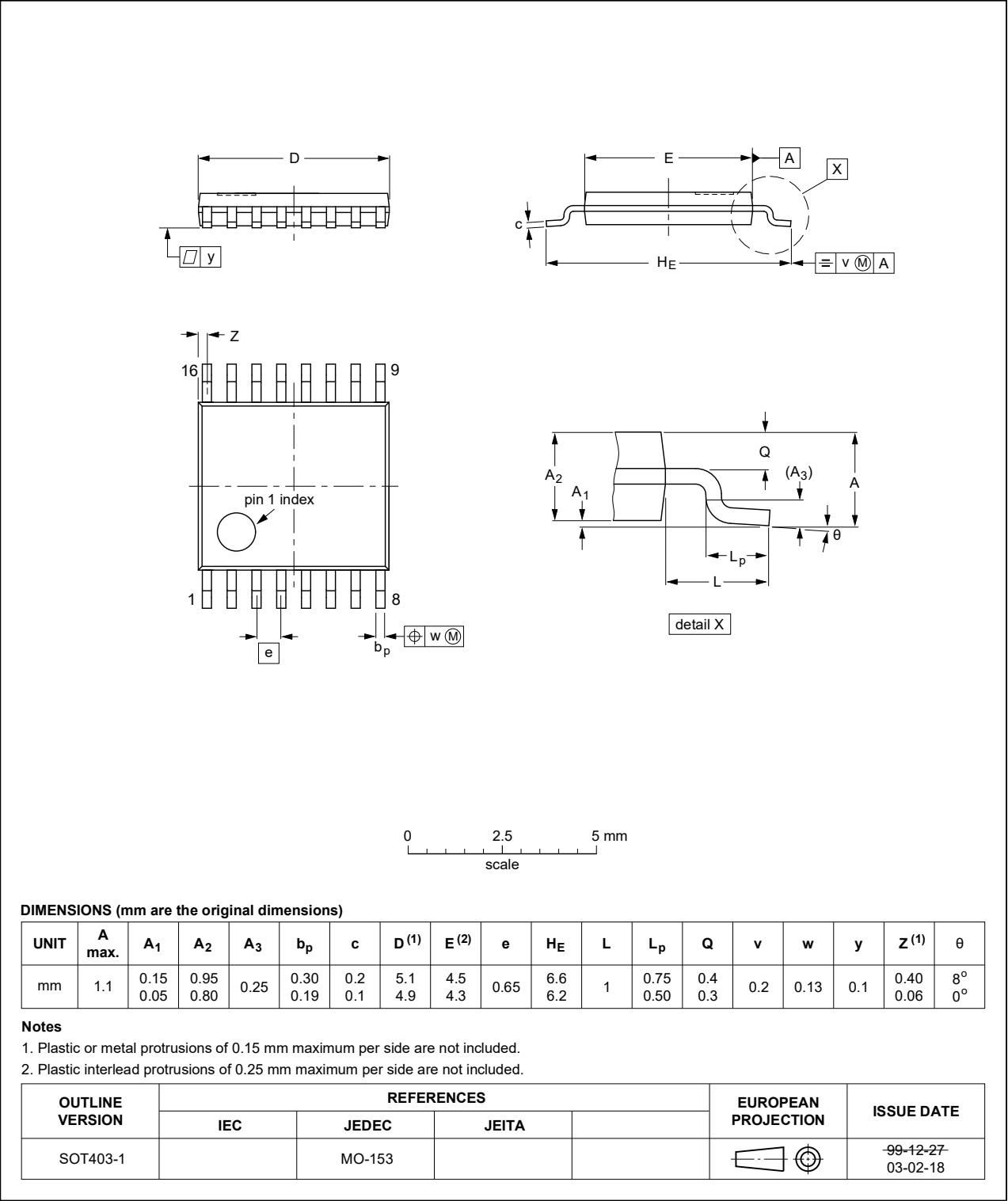


Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

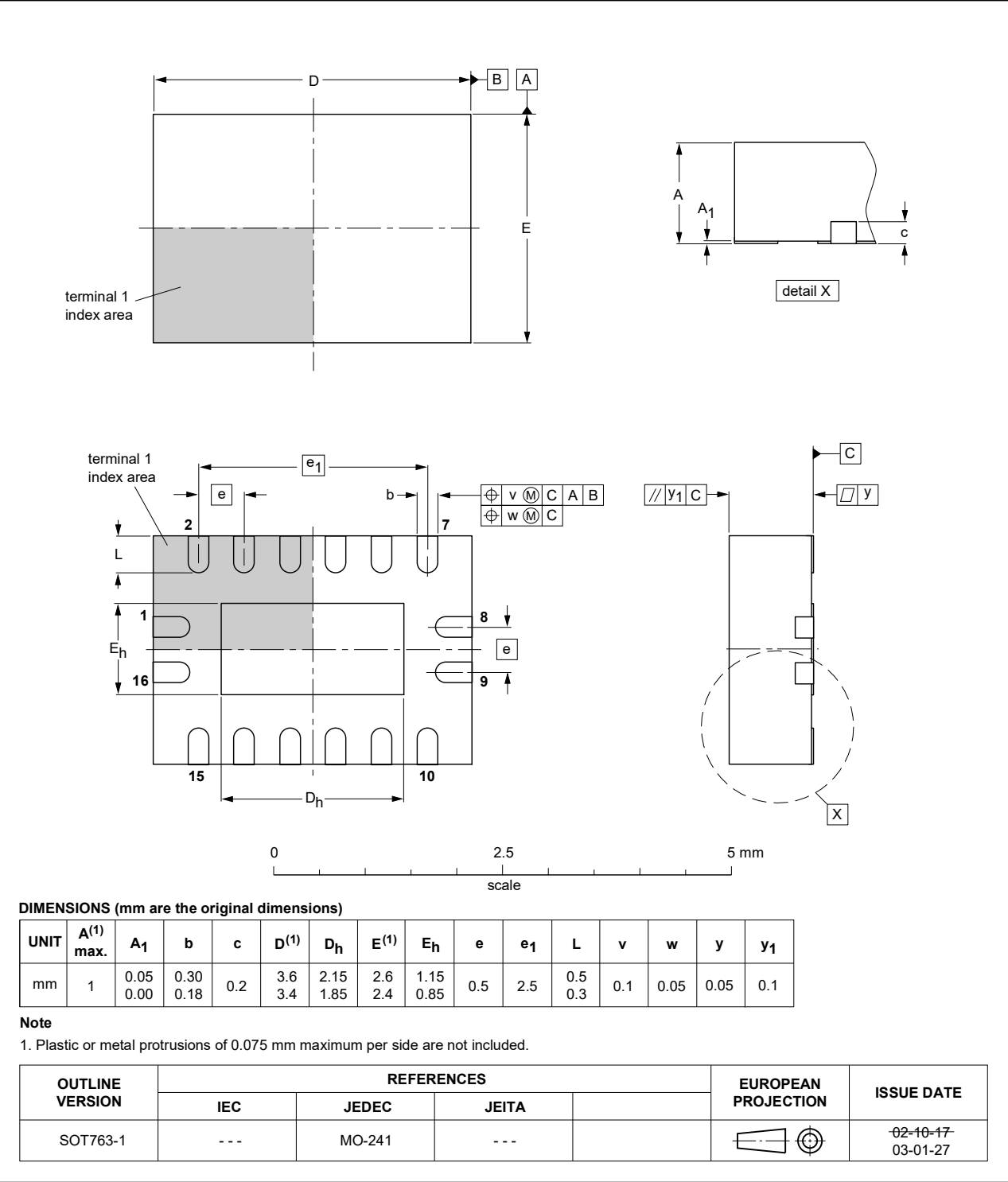


Fig. 16. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT595_Q100 v.2	20200526	Product data sheet	-	74AHC_AHCT595_Q100 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Fig. 7: Timing diagram updated with SHCP waveform. • Table 4: Derating values for P_{tot} total power dissipation updated. • Table 7: Propagation delay symbol and parameter corrected (Errata).			
74AHC_AHCT595_Q100 v.1	20120712	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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