

N-channel 40 V, 2.1 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

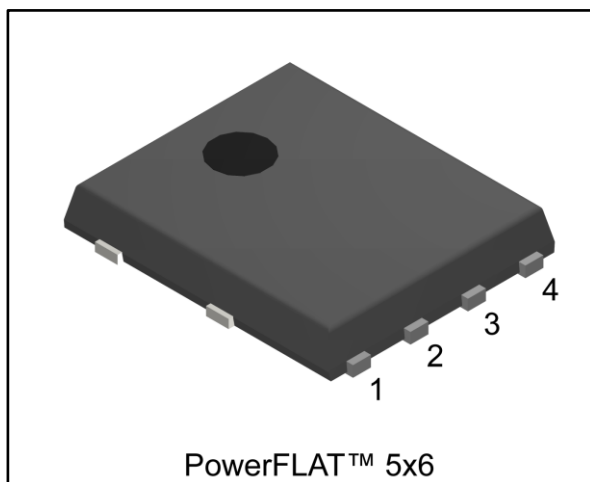
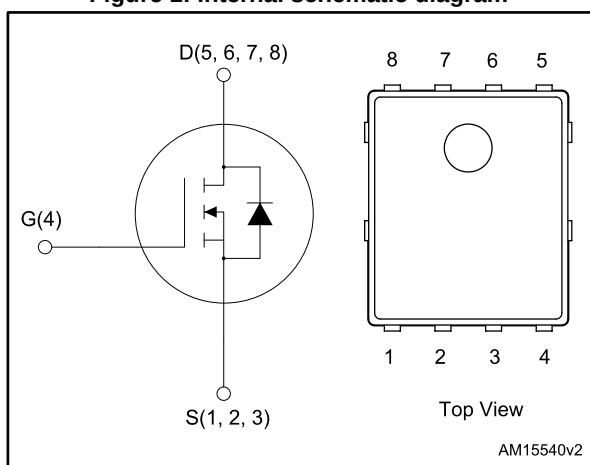


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL160N4F7	40 V	2.5 mΩ	120 A

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL160N4F7	160N4F7	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings.....	3
2	Electrical characteristics	4
3	Electrical curves	6
4	Test circuits	8
5	Package information	9
5.1	PowerFLAT™ 5x6 type C package information	9
5.2	PowerFLAT™ 5x6 packing information.....	11
6	Revision history.....	13

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)(2)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	108	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	480	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	111	W
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	32	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	22	A
$I_{DM}^{(3)(4)}$	Drain current (pulsed)	128	A
$P_{TOT}^{(4)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
I_{AV}	Avalanche current	16	A
E_{AS}	Single pulse avalanche energy ($T_J = 25\text{ }^\circ\text{C}$, $I_D = 16\text{ A}$, $V_{DD} = 25\text{ V}$)	260	mJ
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operating junction temperature range		

Notes:

- (1) Drain current is limited by package
 (2) This value is rated according to R_{thj-c}
 (3) Pulse width limited by safe operating area
 (4) This value is rated according to $R_{thj-pcb}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	31.3	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case max.	1.35	$^\circ\text{C/W}$

Notes:

- (1) When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40		V	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ $V_{DS} = 40\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 16\text{ A}$		2.1	2.5	m Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2300	-	pF
C_{oss}	Output capacitance		-	786	-	pF
C_{rss}	Reverse transfer capacitance		-	43	-	pF
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 32\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	29	-	nC
Q_{gs}	Gate-source charge		-	13	-	nC
Q_{gd}	Gate-drain charge		-	5.6	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 16\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	14	-	ns
t_r	Rise time		-	6.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	19	-	ns
t_f	Fall time		-	5.7	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 32\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_D = 32\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 32\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	55		ns
Q_{rr}	Reverse recovery charge		-	67		nC
I_{RRM}	Reverse recovery current		-	2.4		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Electrical curves

Figure 2: Safe operating area

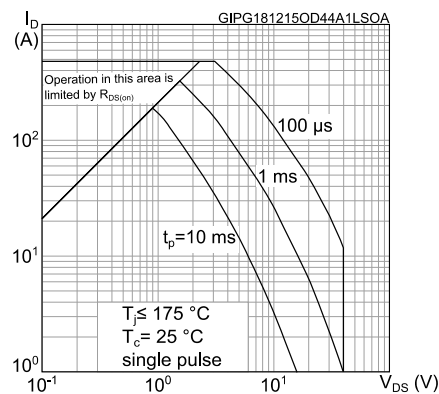


Figure 3: Thermal impedance

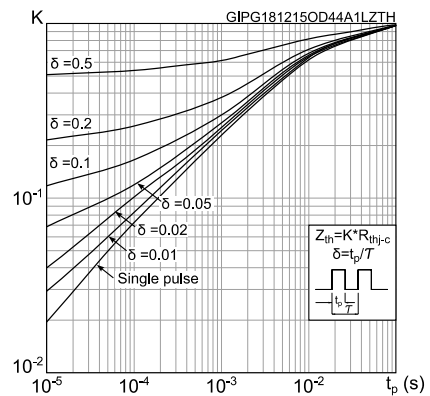


Figure 4: Output characteristics

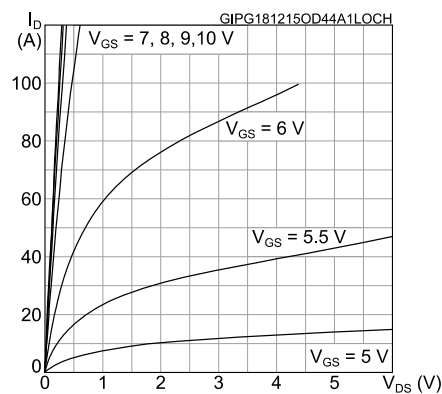


Figure 5: Transfer characteristics

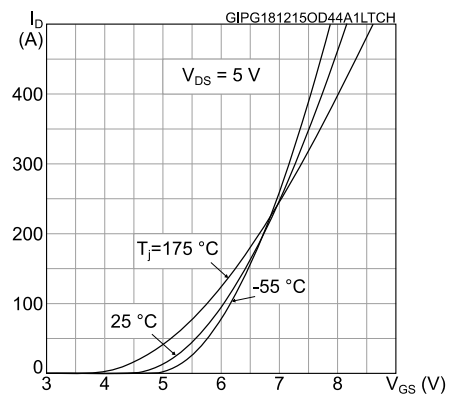


Figure 6: Gate charge vs gate-source voltage

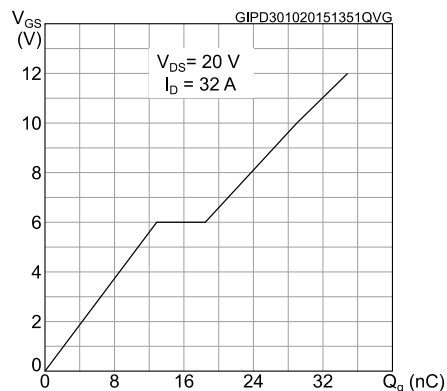


Figure 7: Static drain-source on-resistance

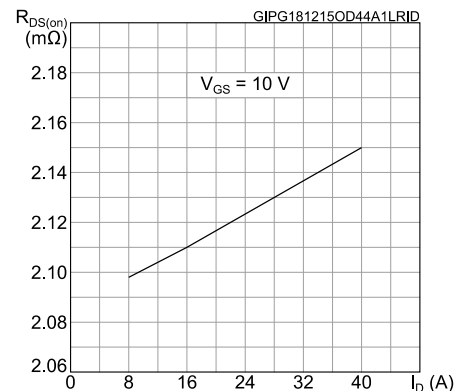


Figure 8: Capacitance variations

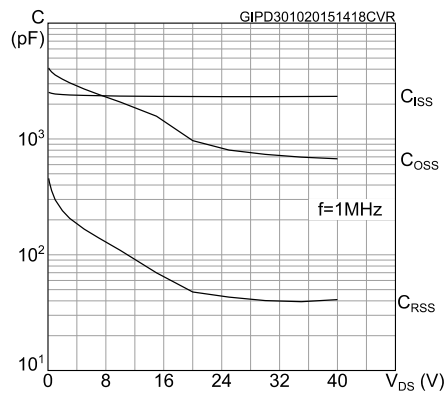


Figure 9: Normalized gate threshold voltage vs temperature

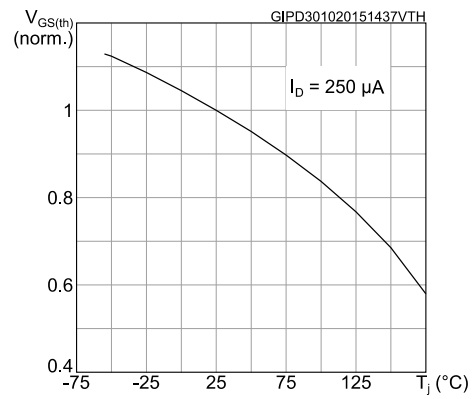


Figure 10: Normalized on-resistance vs temperature

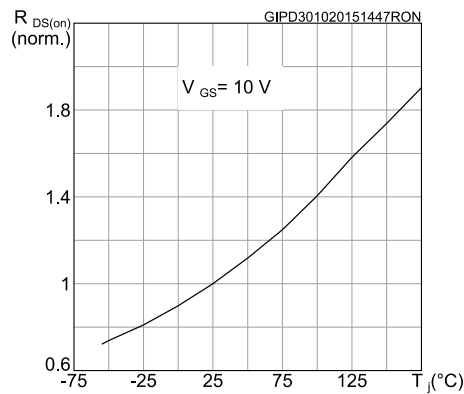
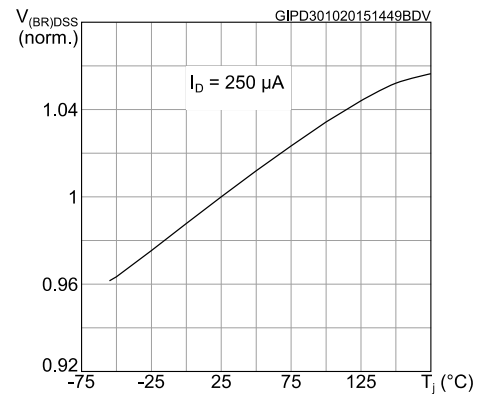
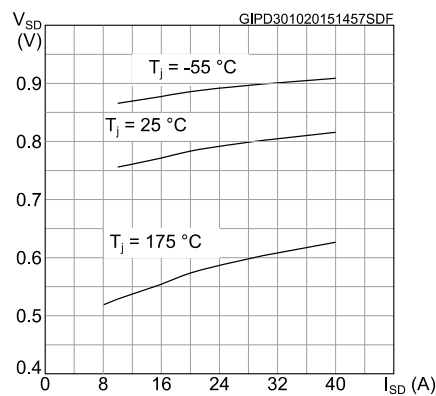
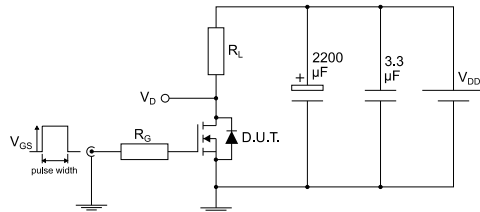
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics



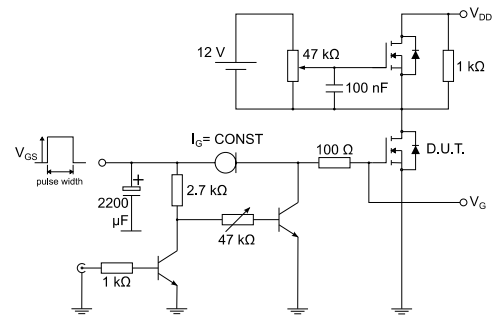
4 Test circuits

Figure 13: Test circuit for resistive load switching times



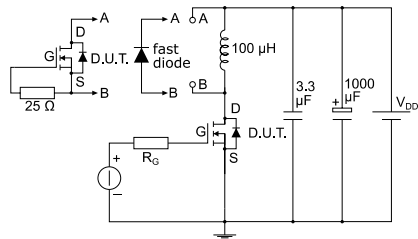
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Figure 14: Test circuit for gate charge behavior



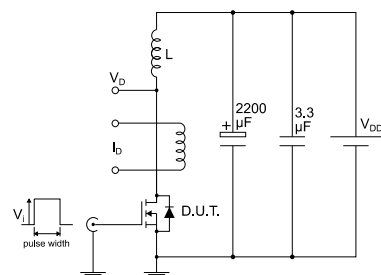
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Figure 15: Test circuit for inductive load switching and diode recovery times



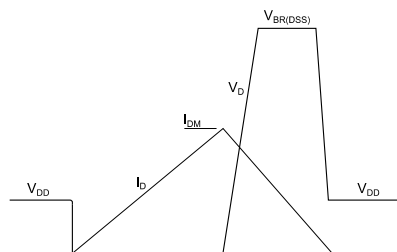
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Figure 16: Unclamped inductive load test circuit



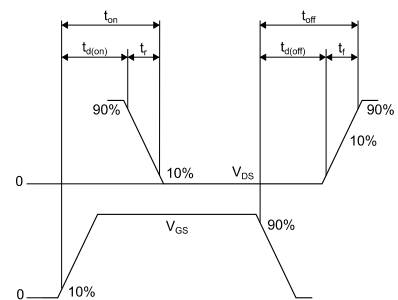
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 PowerFLAT™ 5x6 type C package information

Figure 19: PowerFLAT™ 5x6 type C package outline

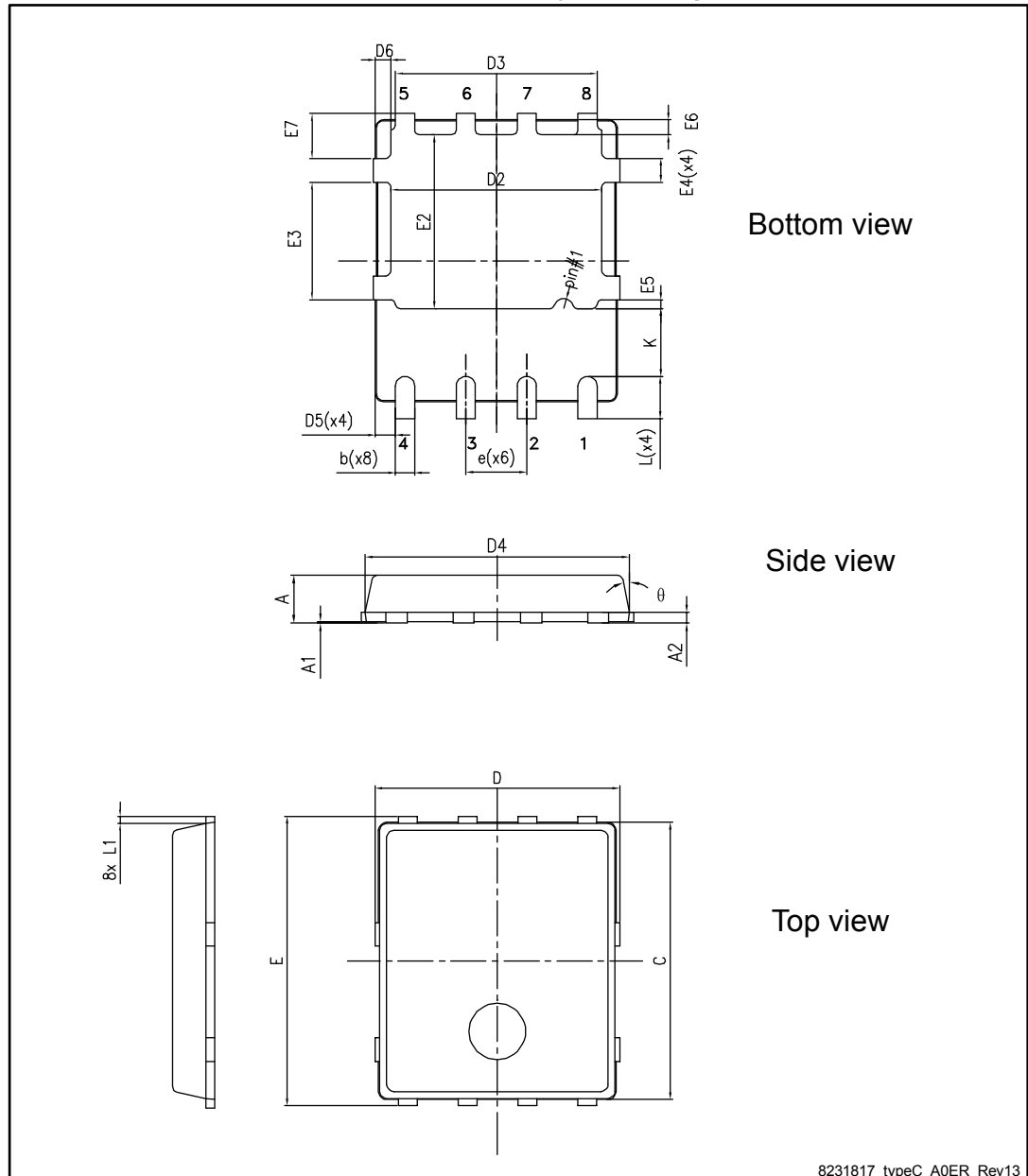
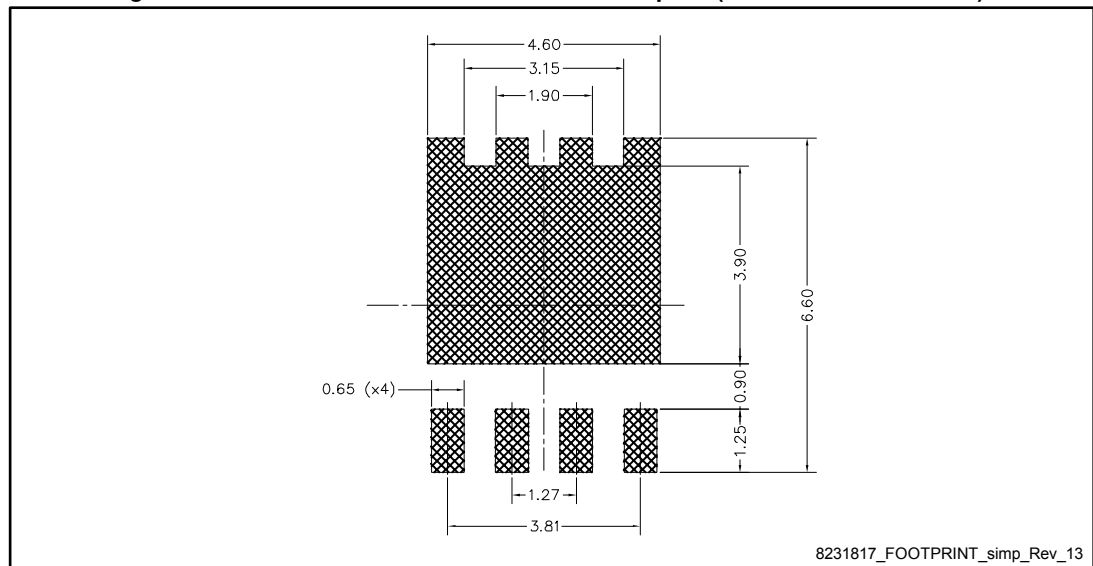


Table 8: PowerFLAT™ 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.450
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.715		1.015
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



5.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

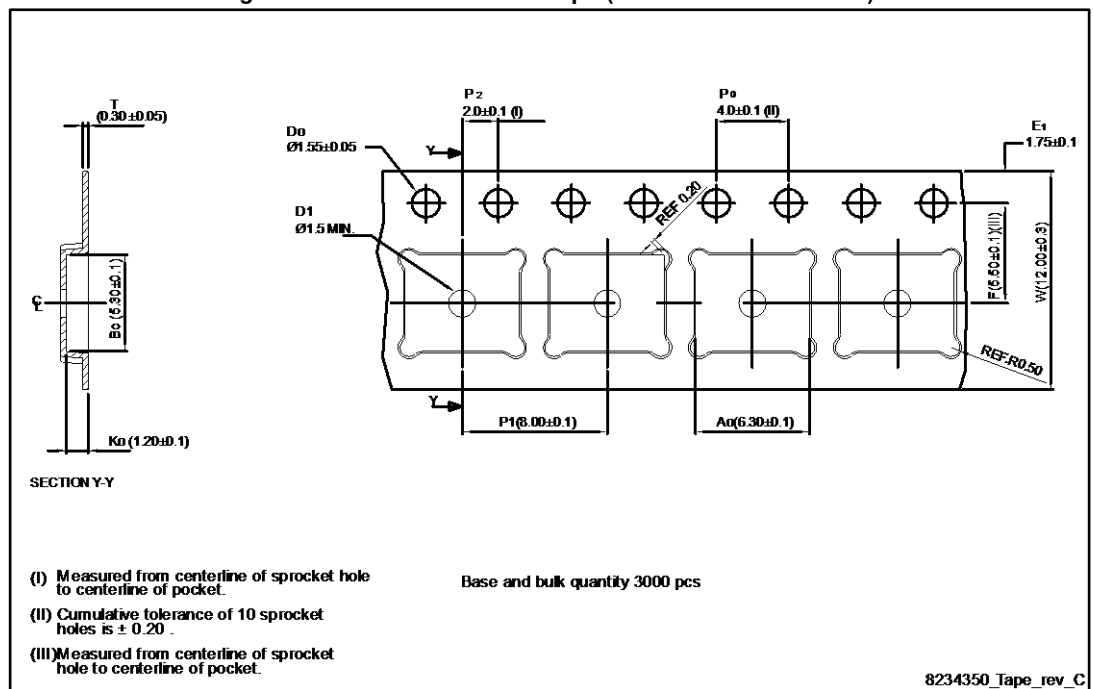


Diagram of a 16-pin connector. The top row shows 8 pins, each represented by a circle with a crosshair. The bottom row shows 8 rectangular slots, each containing a small dot and the label "ST". An arrow points from the text "Pin 1 identification" to the first pin in the top row and the first slot in the bottom row.

Technical drawing of a reel-to-reel tape cassette, showing front, side, and core details with dimensions in millimeters.

Front View (Left): Shows the circular tape compartments. Dimensions include: PART NO. (top left), R25.00 (radius of central hub), 2.50 (width of central hub), 4.00 (width of central hub), 1.90 (width of central hub), 2.50 (width of central hub), 1.90 (width of central hub), 2.50 (width of central hub), 1.90 (width of central hub), 2.50 (width of central hub), 1.90 (width of central hub), 2.50 (width of central hub).

Side View (Right): Shows the profile of the cassette. Dimensions include: W3 11.9/15.4 (width of top flange), W2 18.4 (max) (width of middle flange), 3N 17.8(+2/-0) (width of bottom flange), W1 12.4 (+2/-0) (width of bottom flange), A 330 (+0/-4.0) (overall height).

Core Detail (Bottom Left): Shows the central hub. Dimensions include: R1.10 (radius of central hub), Ø21.2 (outer diameter of central hub), Ø13.00 (inner diameter of central hub), 2.20 (width of central hub).

ESD LOGO: A logo is located on the bottom flange, labeled "ESD LOGO".

All dimensions are in millimeters

8234350 Reel rev

6 Revision history

Table 9: Document revision history

Date	Revision	Changes
14-May-2015	1	First release.
23-Feb-2016	2	Updated title. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source-drain diode"</i> Minor text changes.

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