0.2 µV/°C Offset Drift, 105 MHz, Low Power, Multimode, Rail-to-Rail Amplifier

Data Sheet

ADA4806-1

FEATURES

- **Ultralow supply current**
  - **Full power mode: 500 µA**
  - **Sleep mode: 74 µA**
  - **Shutdown mode: 2.9 µA**
- **Dynamic power scaling**
  - **Turn-on time from shutdown mode: 1.5 µs**
  - **Turn-on time from sleep mode: 0.45 µs**
- **High speed performance with dc precision**
  - **Input offset voltage: 125 µV maximum**
  - **Input offset voltage drift: 1.5 µV/°C maximum**
  - **−3 dB bandwidth: 105 MHz**
  - **Slew rate: 160 V/ µs**
- **Low noise and distortion**
  - **5.9 nV/√Hz input voltage noise with 8 Hz 1/f corner**
  - **−102 dBc/−126 dBc HD2/HD3 at 100 kHz**
- **Wide supply range: 2.7 V to 10 V**
- **Small package: 8-lead SOT-23**

APPLICATIONS

- **Portable and battery-powered instruments and systems**
- **High channel density data acquisition systems**
- **Precision analog-to-digital converter (ADC) drivers**
- **Voltage reference buffers**
- **Portable point of sales terminals**
- **Active RFID readers**

GENERAL DESCRIPTION

The ADA4806-1 is a high speed, voltage feedback, rail-to-rail output, single operational amplifier with three power modes: full power mode, sleep mode, and shutdown mode. In full power mode, this amplifier provides a wide bandwidth of 105 MHz at a gain of +1, a fast slew rate 160 V/µs, and excellent dc precision with a low input offset voltage of 125 µV (maximum) and an input offset voltage drift of 1.5 µV/°C (maximum), while con-suming only 500 µA of quiescent current. Despite being a low power amplifier, the ADA4806-1 provides excellent overall performance, making it ideal for low power, high resolution data conversion systems.

For data conversion applications where minimizing power dissipation is paramount, the ADA4806-1 offers a method to reduce power by dynamically scaling the quiescent power of the ADC driver with the sampling rate of the system by switching the amplifier to a lower power mode between samples.

TYPICAL APPLICATIONS CIRCUIT

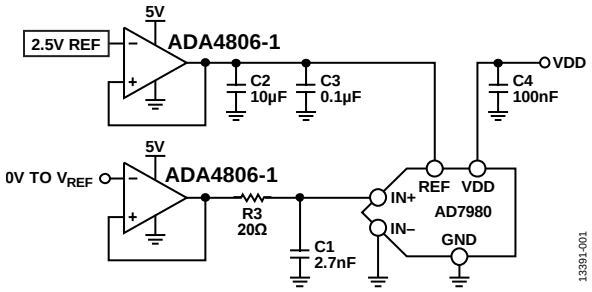

Figure 1. Driving the AD7980 with the ADA4806-1

Sleep mode reduces the amplifier quiescent current to 74 µA and provides a fast turn-on time of only 0.45 µs, enabling the use of dynamic power scaling for sample rates approaching 2 MSPS. For additional power savings at lower samples rates, the shutdown mode further reduces the quiescent current to only 2.9 µA.

The ADA4806-1 operates over a wide range of supply voltages and is fully specified at supplies of 3 V, 5 V and ±5 V. This amplifier is available in a compact, 8-lead SOT-23 package and is rated to operate over the industrial temperature range of −40°C to +125°C.

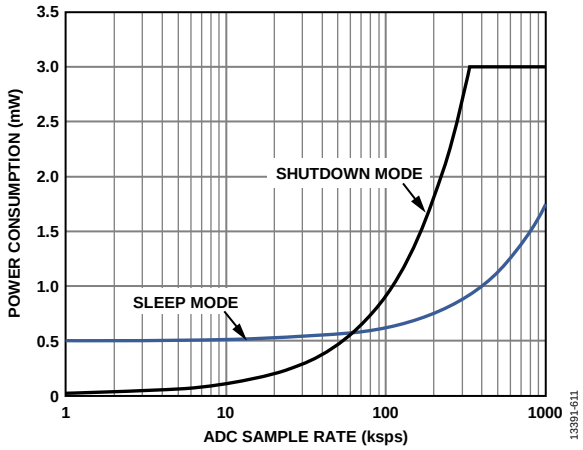

Figure 2. Quiescent Power Dissipation vs. ADC Sample Rate, Using Dynamic Power Scaling for the Two Low Power Modes

Table 1. Complementary ADCs to the ADA4806-1

Product	ADC Power (mW)	Throughput (MSPS)	Resolution (Bits)	SNR (dB)
AD7980	4.0	1	16	90.5[1]
AD7982	7.0	1	18	98
AD7984	10.5	1.33	18	98.5

[1] This SNR value is for the A Grade version of the AD7980.

Rev. 0 **Document Feedback**

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REVISION HISTORY

9/15—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

V_S = ±5 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to ground; unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		120		MHz
	G = +1, V_{OUT} = 2 V p-p		40		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		18		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step		190		V/µs
	G = +2, V_{OUT} = 4 V step		250		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		35		ns
	G = +2, V_{OUT} = 4 V step		78		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 2 V p-p		−114/−140		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−102/−128		dBc
	f_C = 20 kHz, V_{OUT} = 4 V p-p, G = +1		−109/−143		dBc
	f_C = 100 kHz, V_{OUT} = 4 V p-p, G = +1		−93/−130		dBc
	f_C = 20 kHz, V_{OUT} = 4 V p-p, G = +2		−113/−142		dBc
	f_C = 100 kHz, V_{OUT} = 4 V p-p, G = +2		−96/−130		dBc
Input Voltage Noise	f = 100 kHz		5.2		nV/√Hz
Input Voltage Noise 1/f Corner Frequency			8		Hz
0.1 Hz to 10 Hz Voltage Noise			44		nV rms
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	Full power mode		13	125	µV
	Low power mode, $\overline{SLEEP}$ = $-V_S$		800		µV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	µV/°C
Input Bias Current (I_B)	Full power mode		550	800	nA
	Low power mode, $\overline{SLEEP}$ = $-V_S$		3		nA
Input Offset Current			2.1	25	nA
Open-Loop Gain	V_{OUT} = −4.0 V to +4.0 V	107	111		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−5.1		+4	V
Common-Mode Rejection Ratio (CMRR)	$V_{IN, CM}$ = −4.0 V to +4.0 V	103	130		dB
$\overline{SHUTDOWN}$ PIN					
$\overline{SHUTDOWN}$ Voltage					
Low	Powered down		<−1.3		V
High	Enabled		>−0.9		V
$\overline{SHUTDOWN}$ Current					
Low	Powered down	−1.0	+0.2		µA
High	Enabled		0.02	1.0	µA
Turn-Off Time	50% of $\overline{SHUTDOWN}$ to <10% of enabled quiescent current		1.25	2.75	µs
Turn-On Time	50% of $\overline{SHUTDOWN}$ to >99% of final V_{OUT}		1	3	µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{\text{SLEEP}}$ PIN					
$\overline{\text{SLEEP}}$ Voltage					
Low	Powered down		<−1.3		V
High	Enabled		>−0.9		V
$\overline{\text{SLEEP}}$ Current					
Low	Low Power Mode, $\overline{\text{SLEEP}} = -V_S$	−1.0	+0.2		µA
High	Enabled		0.02	1.0	µA
Turn-Off Time (Full Power Mode to Sleep Mode)	50% of $\overline{\text{SLEEP}}$ to 30% of enabled quiescent current		180	240	ns
Turn-On Time (Sleep Mode to Full Power Mode)	50% of $\overline{\text{SLEEP}}$ to >99% of final V_{OUT}		450	600	ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = +6 V to −6 V, G = +2		95/100		ns
Output Voltage Swing	R_L = 2 kΩ	−4.98		+4.98	V
Short-Circuit Current	Sourcing/sinking; full power mode		85/73		mA
	Sourcing/sinking; low power mode, $\overline{\text{SLEEP}} = -V_S$		1.4/1.8		mA
Linear Output Current	<1% total harmonic distortion (THD) at 100 kHz, V_{OUT} = 2 V p-p		±58		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{\text{SHUTDOWN}} = -V_S$		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current per Amplifier	Full power mode		570	625	µA
	Low power mode, $\overline{\text{SLEEP}} = -V_S$		85		µA
	$\overline{\text{SHUTDOWN}} = -V_S$		7.4	12	µA
Power Supply Rejection Ratio (PSRR)					
Positive	$+V_S$ = +3 V to +5 V, $-V_S$ = −5 V	100	119		dB
Negative	$+V_S$ = +5 V, $-V_S$ = −3 V to −5 V	100	122		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

5 V SUPPLY

V_S = 5 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to midsupply; unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		105		MHz
	G = +1, V_{OUT} = 2 V p-p		35		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		20		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step		160		V/µs
	G = +2, V_{OUT} = 4 V step		220		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		35		ns
	G = +2, V_{OUT} = 4 V step		82		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 2 V p-p		−114/−135		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−102/−126		dBc
	f_C = 20 kHz, G = +2, V_{OUT} = 4 V p-p		−107/−143		dBc
	f_C = 100 kHz, G = +2, V_{OUT} = 4 V p-p		−90/−130		dBc
Input Voltage Noise	f = 100 kHz		5.9		nV/√Hz
Input Voltage Noise 1/f Corner			8		Hz
0.1 Hz to 10 Hz Voltage Noise			54		nV rms
Input Current Noise	f = 100 kHz		0.6		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	Full power mode		10	125	µV
	Low power mode, $\overline{SLEEP}$ = $-V_S$		500		µV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	µV/°C
Input Bias Current	Full power mode		470	720	nA
	Low power mode, $\overline{SLEEP}$ = $-V_S$		3		nA
Input Offset Current			0.4		nA
Open-Loop Gain	V_{OUT} = 1.25 V to 3.75 V	105	109		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−0.1		+4	V
Common-Mode Rejection Ratio	$V_{IN, CM}$ = 1.25 V to 3.75 V	103	133		dB
$\overline{SHUTDOWN}$ PIN					
$\overline{SHUTDOWN}$ Voltage					
Low	Powered down		<1.5		V
High	Enabled		>1.9		V
$\overline{SHUTDOWN}$ Current					
Low	Powered down	−1.0	+0.1		µA
High	Enabled		0.01	1.0	µA
Turn-Off Time	50% of $\overline{SHUTDOWN}$ to <10% of enabled quiescent current		0.9	1.25	µs
Turn-On Time	50% of $\overline{SHUTDOWN}$ to >99% of final V_{OUT}		1.5	4	µs
$\overline{SLEEP}$ PIN					
$\overline{SLEEP}$ Voltage					
Low	Powered down		<1.5		V
High	Enabled		>1.9		V
$\overline{SLEEP}$ Current					
Low	Low power mode, $\overline{SLEEP}$ = $-V_S$	−1.0	+0.1		µA
High	Enabled		0.01	1.0	µA
Turn-Off Time (Full Power Mode to Sleep Mode)	50% of $\overline{SLEEP}$ to 30% of enabled quiescent current		150	185	ns
Turn-On Time (Sleep Mode to Full Power Mode)	50% of $\overline{SLEEP}$ to >99% of final V_{OUT}		450	600	ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +6 V, G = +2		130/145		ns
Output Voltage Swing	R_L = 2 kΩ	0.02		4.98	V
Short-Circuit Current	Sourcing/sinking; full power mode		73/63		mA
	Sourcing/sinking; low power mode, $\overline{SLEEP}$ = $-V_S$		1.0/1.3		mA
Linear Output Current	<1% THD at 100 kHz, V_{OUT} = 2 V p-p		±47		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{SHUTDOWN}$ = $-V_S$		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current per Amplifier	Full power mode		500	520	µA
	Low power mode, $\overline{SLEEP}$ = $-V_S$		74		µA
	$\overline{SHUTDOWN}$ = $-V_S$		2.9	4	µA
Power Supply Rejection Ratio					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −2.5 V	100	120		dB
Negative	$+V_S$ = 2.5 V, $-V_S$ = −1.5 V to −3.5 V	100	126		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

3 V SUPPLY

V_S = 3 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to midsupply; unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		95		MHz
	G = +1, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		30		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		35		MHz
Slew Rate	G = +1, V_{OUT} = 1 V step, $+V_S$ = 2 V, $-V_S$ = −1 V		85		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 1 V step		41		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		−123/−143		dBc
	f_C = 100 kHz, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		−107/−133		dBc
Input Voltage Noise	f = 100 kHz		6.3		nV/√Hz
Input Voltage Noise 1/f Corner			8		Hz
0.1 Hz to 10 Hz Voltage Noise			55		nV rms
Input Current Noise	f = 100 kHz		0.8		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	Full power mode		7	125	µV
	Low power mode, $\overline{SLEEP}$ = $-V_S$		300		µV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	µV/°C
Input Bias Current	Full power mode		440	690	nA
	Low power mode, $\overline{SLEEP}$ = $-V_S$		3		nA
Input Offset Current			0.5		nA
Open-Loop Gain	V_{OUT} = 1.1 V to 1.9 V	100	107		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−0.1		+2	V
Common-Mode Rejection Ratio	$V_{IN, CM}$ = 0.5 V to 2 V	89	117		dB
$\overline{\text{SHUTDOWN}}$ PIN					
$\overline{\text{SHUTDOWN}}$ Voltage					
Low	Powered down		<0.7		V
High	Enabled		>1.1		V
$\overline{\text{SHUTDOWN}}$ Current					
Low	Powered down	−1.0	+0.1		µA
High	Enabled		0.01	1.0	µA
Turn-Off Time	50% of $\overline{\text{SHUTDOWN}}$ to <10% of enabled quiescent current		0.9	1.25	µs
Turn-On Time	50% of $\overline{\text{SHUTDOWN}}$ to >99% of final V_{OUT}		2.5	8	µs
$\overline{\text{SLEEP}}$ PIN					
$\overline{\text{SLEEP}}$ Voltage					
Low	Powered down		<0.7		V
High	Enabled		>1.1		V
$\overline{\text{SLEEP}}$ Current					
Low	Low Power Mode, $\overline{\text{SLEEP}}$ = $-V_S$	−1.0	+0.1		µA
High	Enabled		0.01	1.0	µA
Turn-Off Time (Full Power Mode to Sleep Mode)	50% of $\overline{\text{SLEEP}}$ to 30% of enabled quiescent current		155	210	ns
Turn-On Time (Sleep Mode to Full Power Mode)	50% of $\overline{\text{SLEEP}}$ to >99% of final V_{OUT}		450	600	ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +4 V, G = +2		135/175		ns
Output Voltage Swing	R_L = 2 kΩ	0.02		2.98	V
Short-Circuit Current	Sourcing/sinking; full power mode		65/47		mA
	Sourcing/sinking; low power mode, $\overline{\text{SLEEP}}$ = $-V_S$		1.0/1.3		mA
Linear Output Current	<1% THD at 100 kHz, V_{OUT} = 1 V p-p		±40		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{\text{SHUTDOWN}}$ = $-V_S$		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current per Amplifier	Full power mode		470	495	µA
	Low power mode, $\overline{\text{SLEEP}}$ = $-V_S$		70		µA
	$\overline{\text{SHUTDOWN}}$ = $-V_S$		1.3	3	µA
Power Supply Rejection Ratio					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −1.5 V	96	119		dB
Negative	$+V_S$ = 1.5 V, $-V_S$ = −1.5 V to −3.5 V	96	125		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	±1 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages. Table 6 lists the θ_{JA} for the ADA4806-1.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOT-23	209.1	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4806-1 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4806-1. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4806-1 output load drive.

The quiescent power dissipation is the voltage between the supply pins (V_S) multiplied by the quiescent current (I_S).

$$P_D = Quiescent\ Power + (Total\ Drive\ Power - Load\ Power)$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages must be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, the worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Additionally, more metal directly in contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard, 4-layer board. θ_{JA} values are approximations.

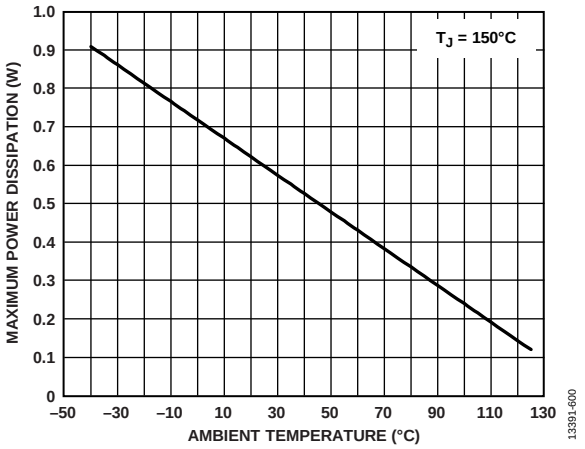


Figure 3. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

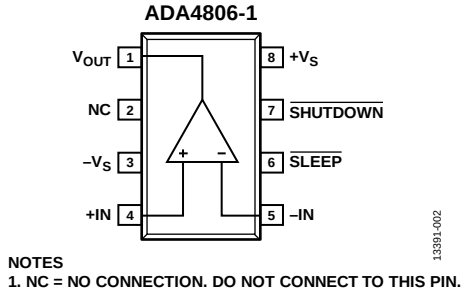


Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}	Output.
2	NC	No Connection. Do not connect to this pin.
3	$-V_S$	Negative Supply.
4	+IN	Noninverting Input.
5	−IN	Inverting Input.
6	$\overline{\text{SLEEP}}$	Low Power Mode.
7	$\overline{\text{SHUTDOWN}}$	Power-Down Mode.
8	$+V_S$	Positive Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

R_L = 2 kΩ, unless otherwise noted. When G = +1, R_F = 0 Ω.

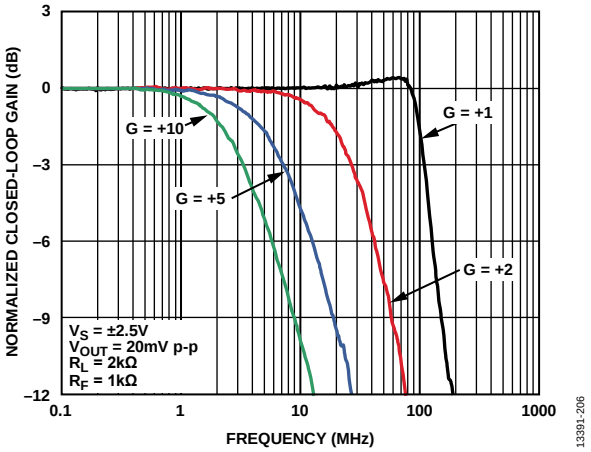


Figure 5. Small Signal Frequency Response for Various Gains

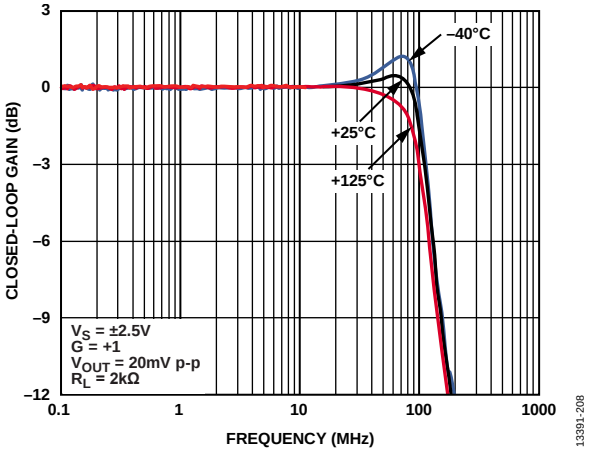


Figure 6. Small Signal Frequency Response for Various Temperatures

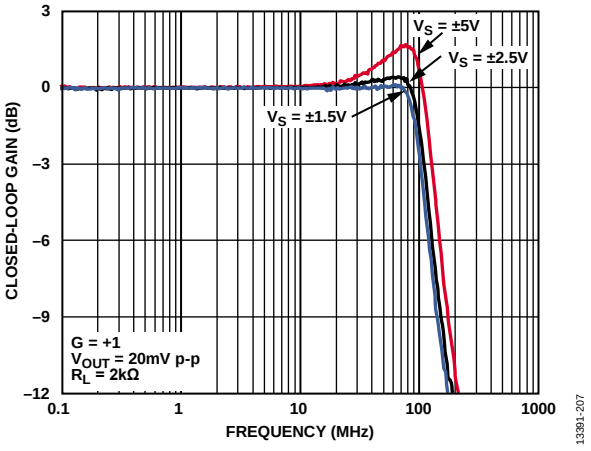


Figure 7. Small Signal Frequency Response for Various Supply Voltages

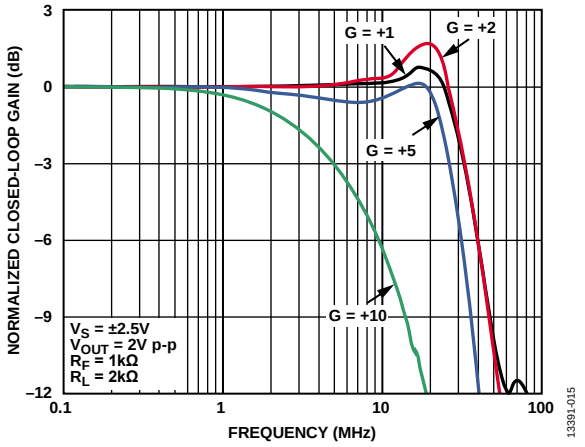


Figure 8. Large Signal Frequency Response for Various Gains

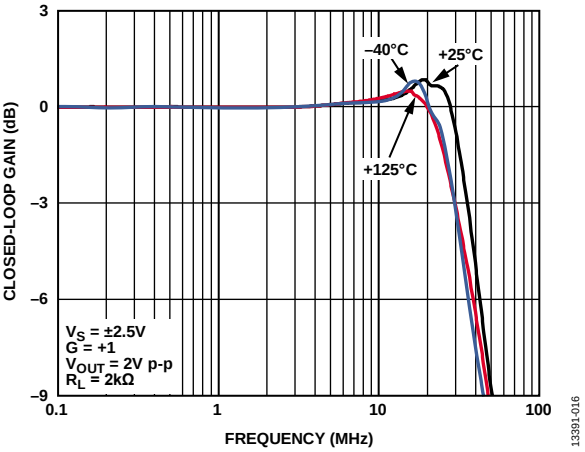


Figure 9. Large Signal Frequency Response for Various Temperatures

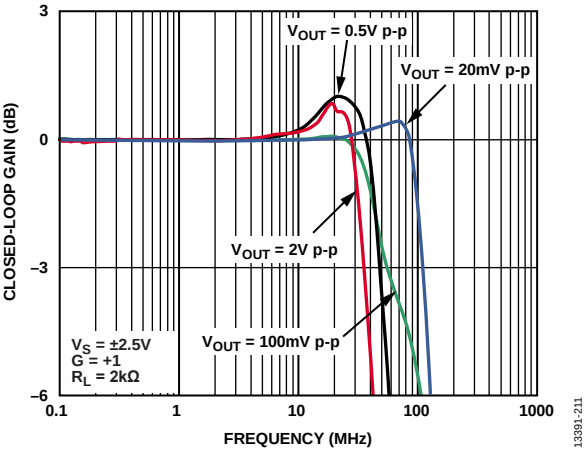


Figure 10. Frequency Response for Various Output Voltages

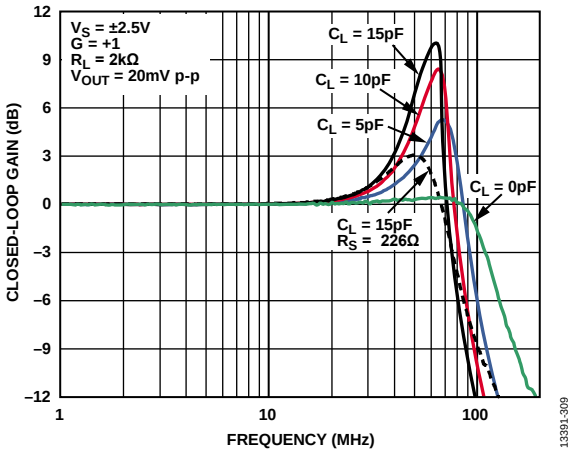


Figure 11. Small Signal Frequency Response for Various Capacitive Loads (See Figure 47)

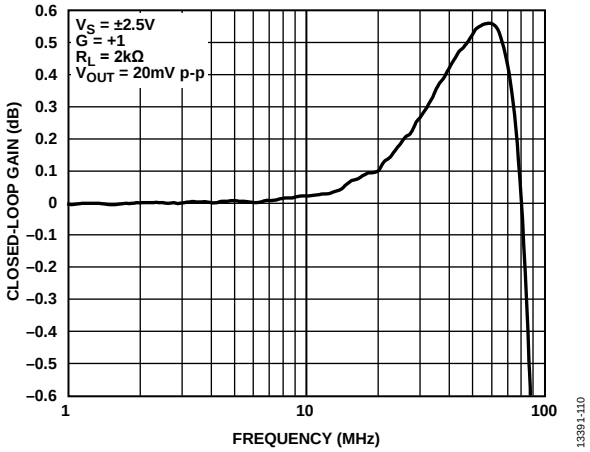


Figure 14. Small Signal 0.1 dB Bandwidth

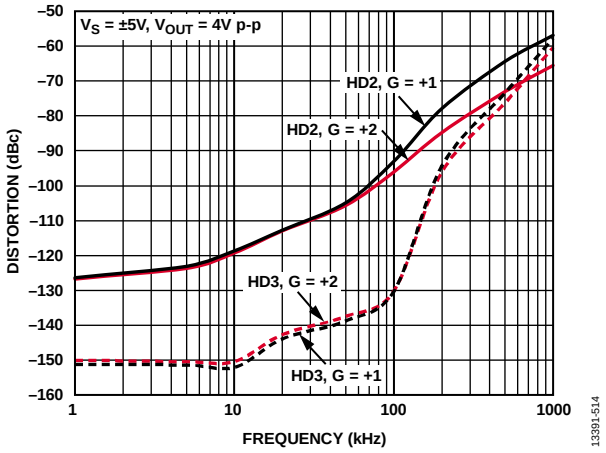


Figure 12. Distortion vs. Frequency for Various Gains

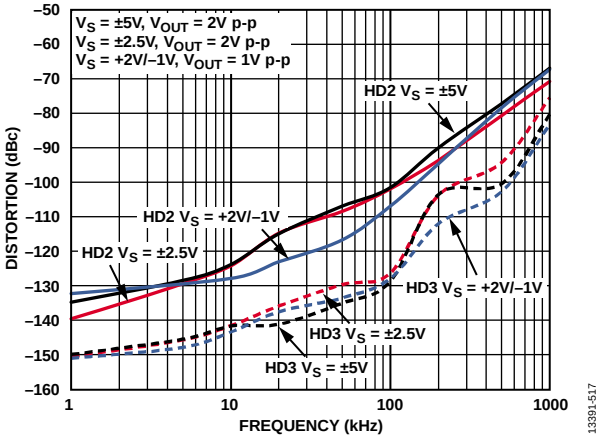


Figure 15. Distortion vs. Frequency for Various Supplies, G = +1

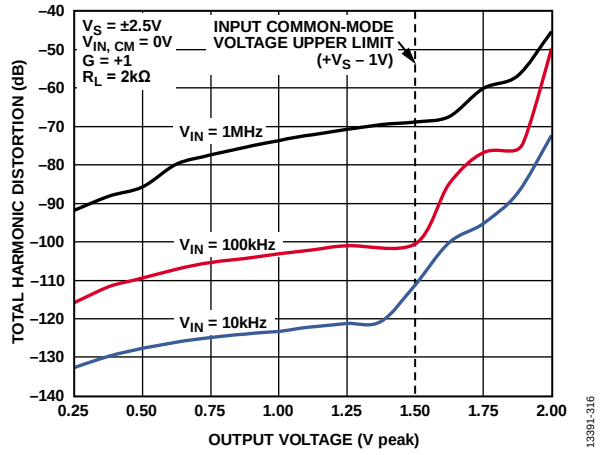


Figure 13. Total Harmonic Distortion vs. Output Voltage For Various Frequencies

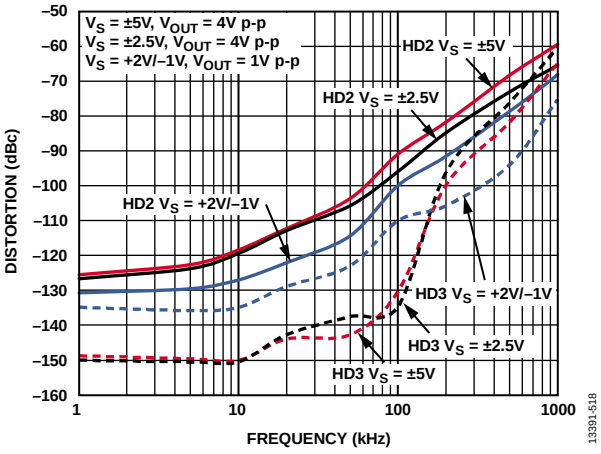


Figure 16. Distortion vs. Frequency, G = +2

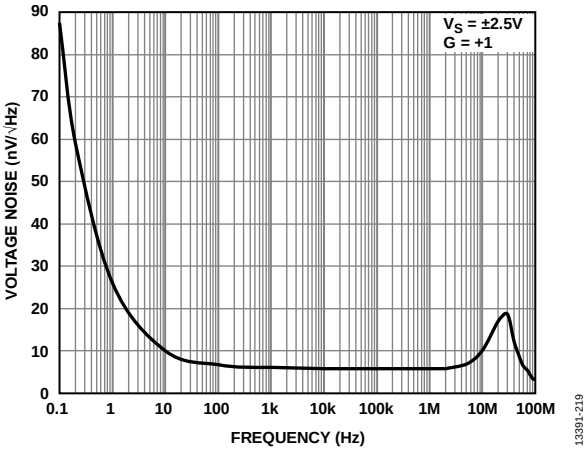


Figure 17. Voltage Noise vs. Frequency

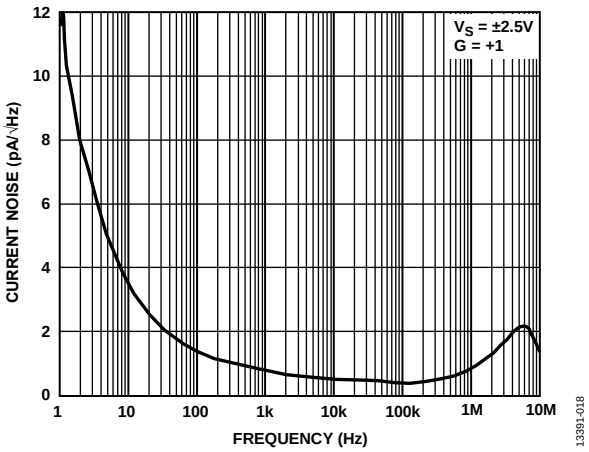


Figure 20. Current Noise vs. Frequency (See Figure 48)

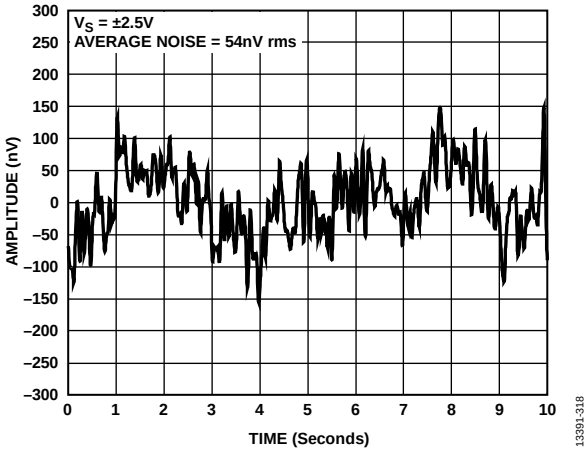


Figure 18. 0.1 Hz to 10 Hz Voltage Noise

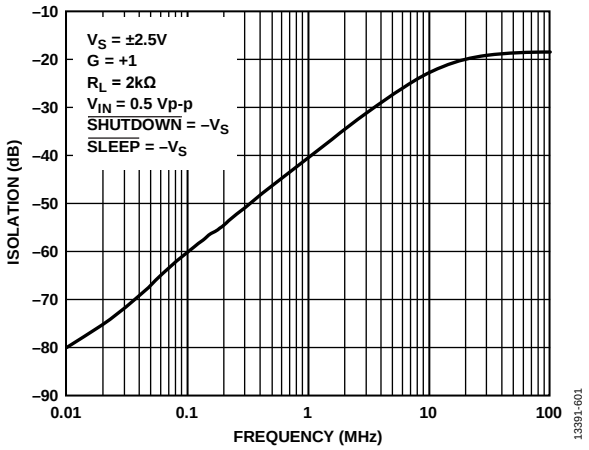


Figure 21. Forward Isolation vs. Frequency

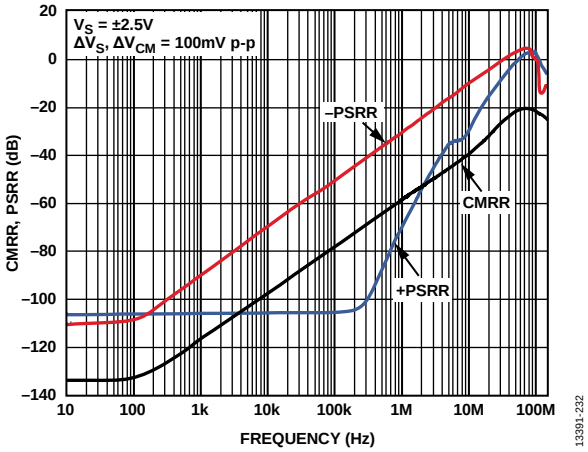


Figure 19. CMRR, PSRR vs. Frequency

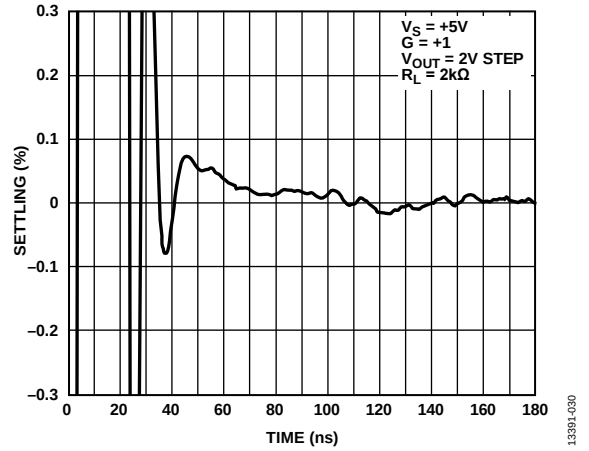


Figure 22. Settling Time to 0.1%

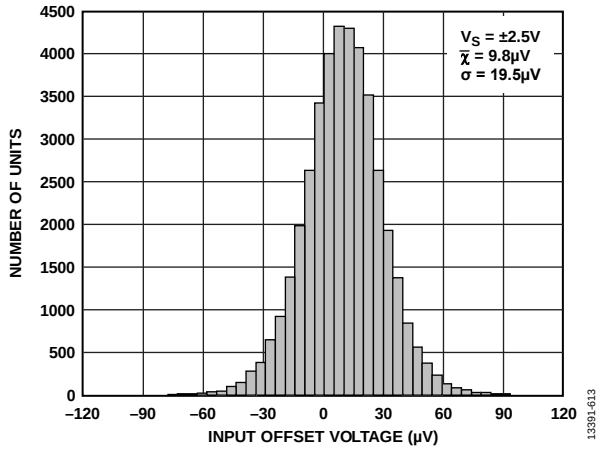


Figure 23. Input Offset Voltage Distribution

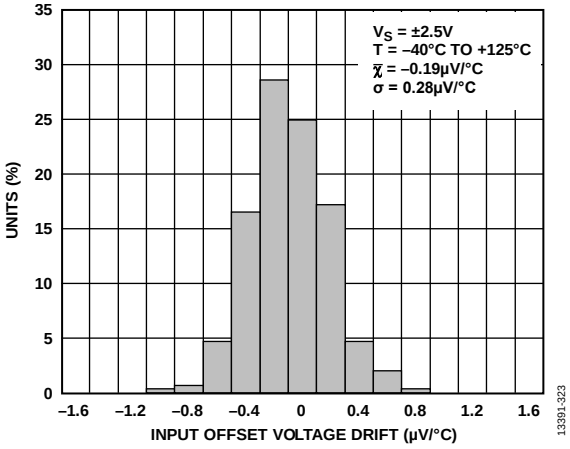


Figure 26. Input Offset Voltage Drift Distribution

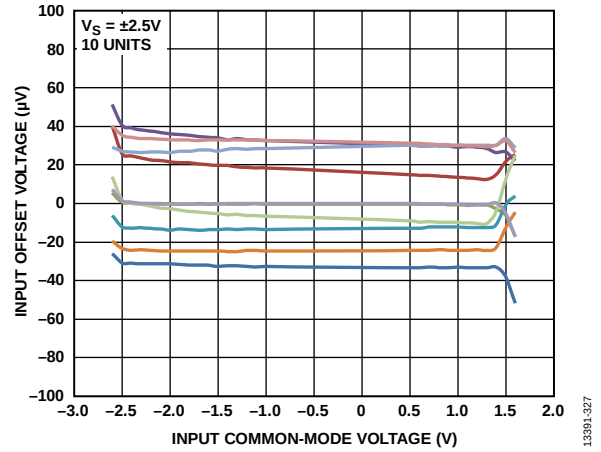


Figure 24. Input Offset Voltage vs. Input Common-Mode Voltage

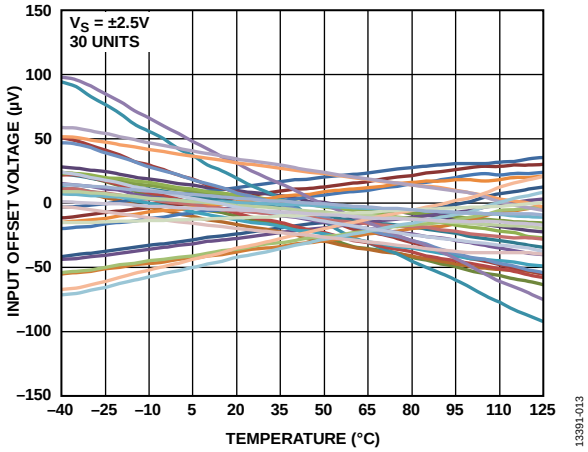


Figure 27. Input Offset Voltage vs. Temperature

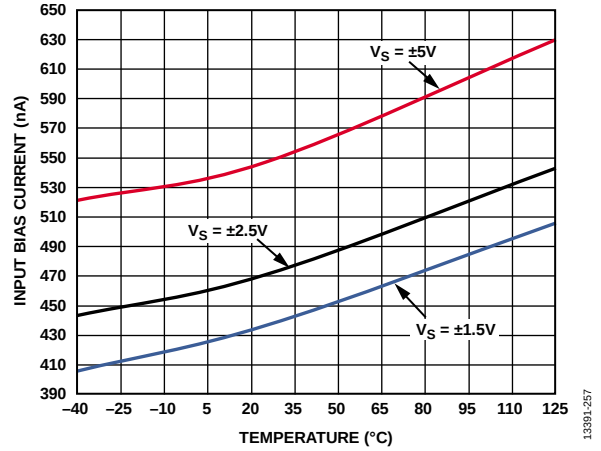


Figure 25. Input Bias Current vs. Temperature for Various Supplies (See Figure 49)

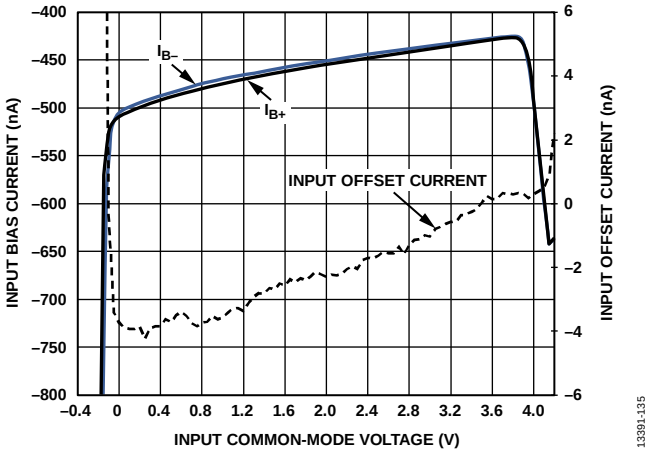


Figure 28. Input Bias Current and Input Offset Current vs. Input Common-Mode Voltage

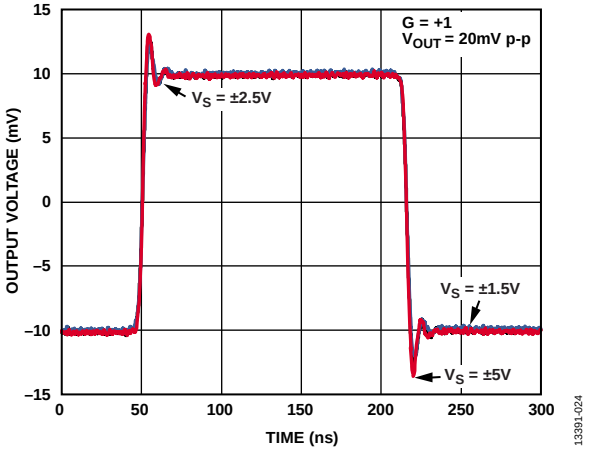


Figure 29. Small Signal Transient Response for Various Supplies

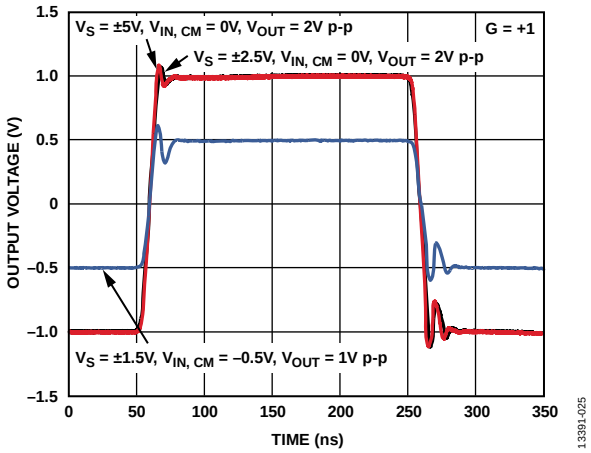


Figure 32. Large Signal Transient Response for Various Supplies

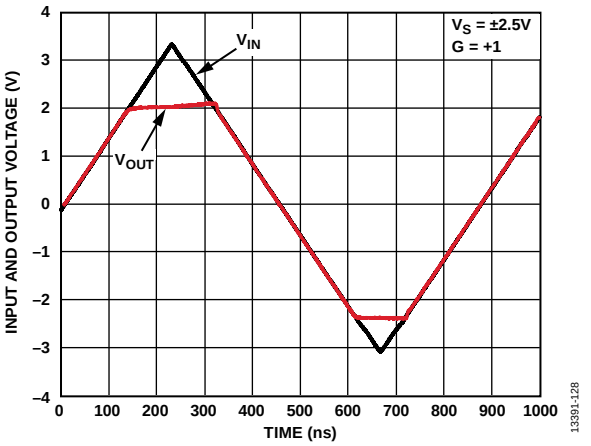


Figure 30. Input Overdrive Recovery Time

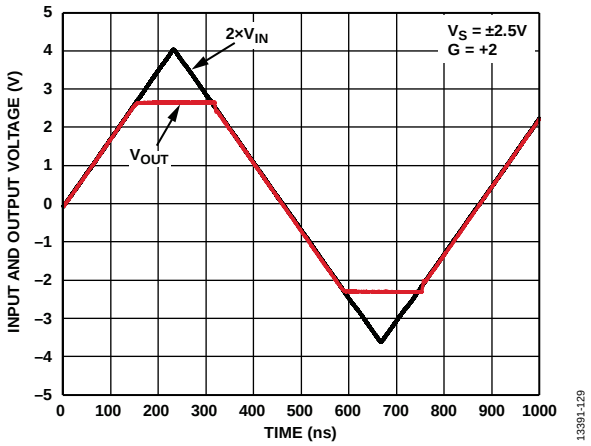


Figure 33. Output Overdrive Recovery Time

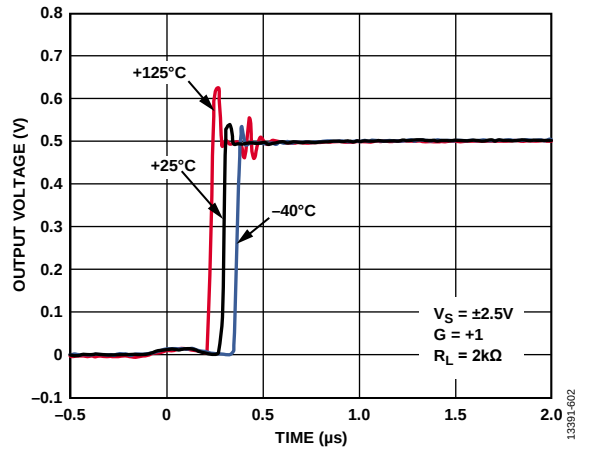


Figure 31. Turn-On Response Time from Shutdown for Various Temperatures (See Figure 50)

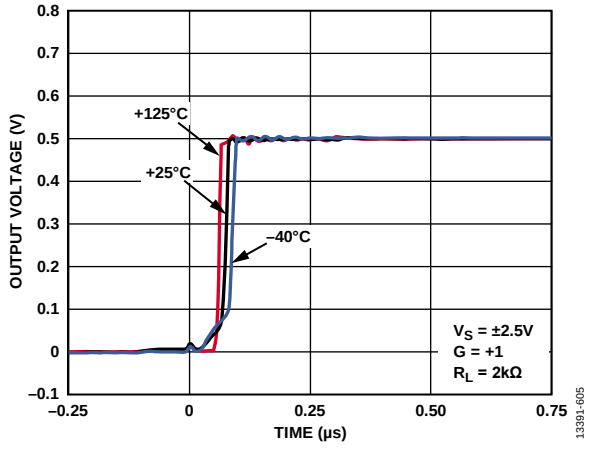


Figure 34. Turn-On Response Time from Sleep for Various Temperatures (See Figure 50)

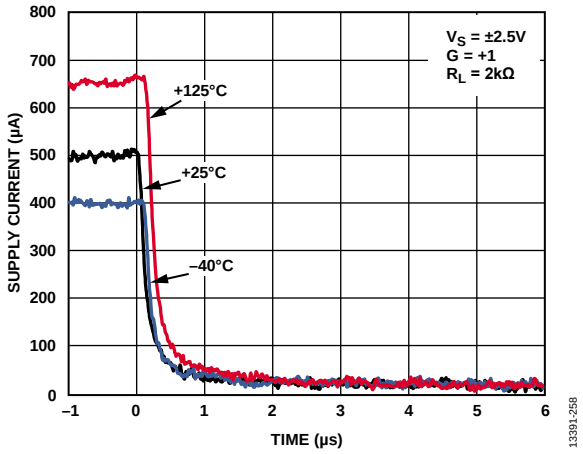


Figure 35. Turn-Off Response Time to Shutdown for Various Temperatures (See Figure 51)

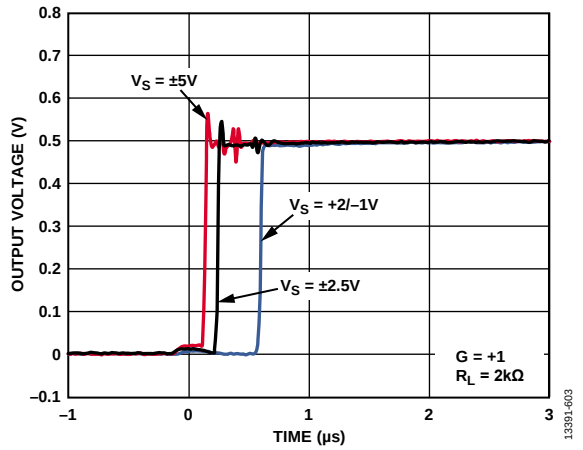


Figure 36. Turn-On Response Time from Shutdown for Various Supplies

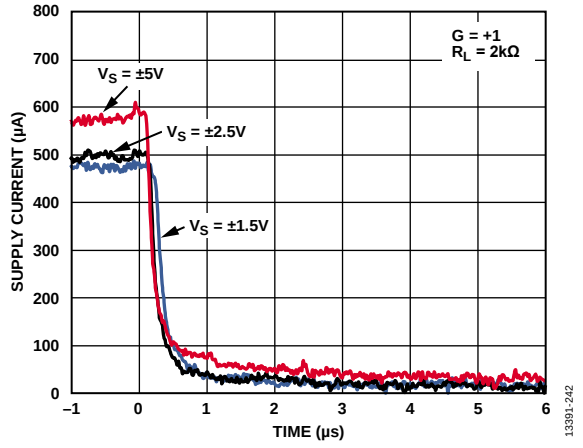


Figure 37. Turn-Off Response Time to Shutdown for Various Supplies

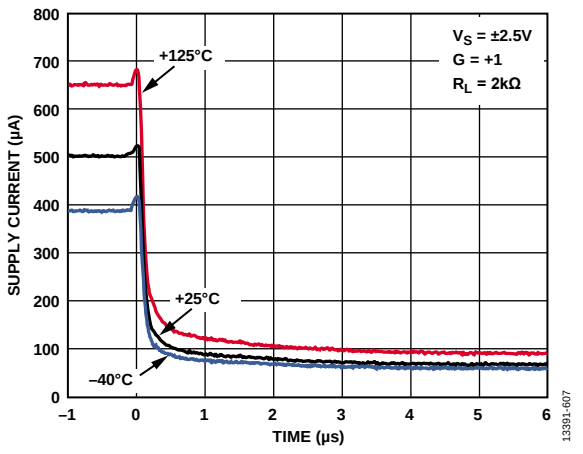


Figure 38. Turn-Off Response Time to Sleep for Various Temperatures (See Figure 51)

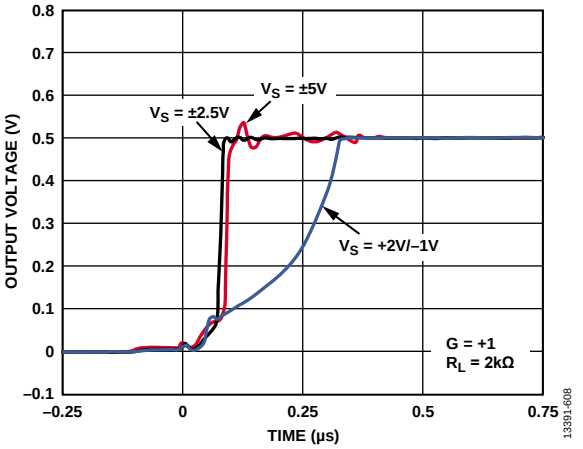


Figure 39. Turn-On Response Time from Sleep for Various Supplies

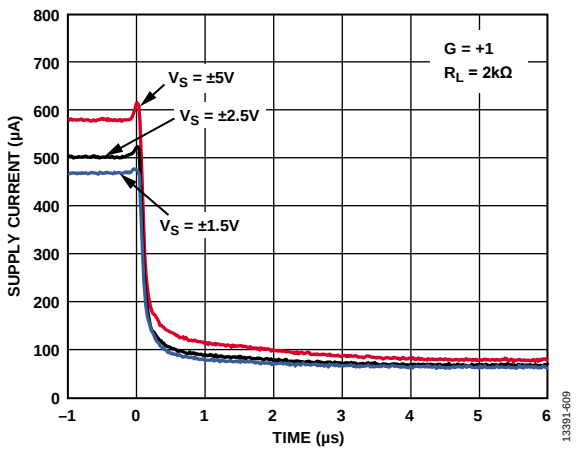


Figure 40. Turn-Off Response Time to Sleep for Various Supplies

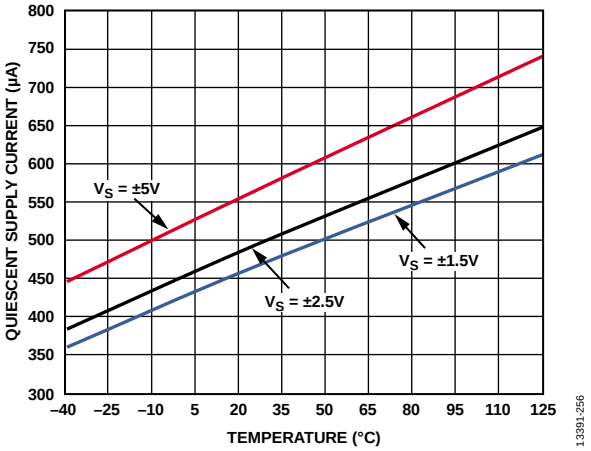


Figure 41. Quiescent Supply Current vs. Temperature

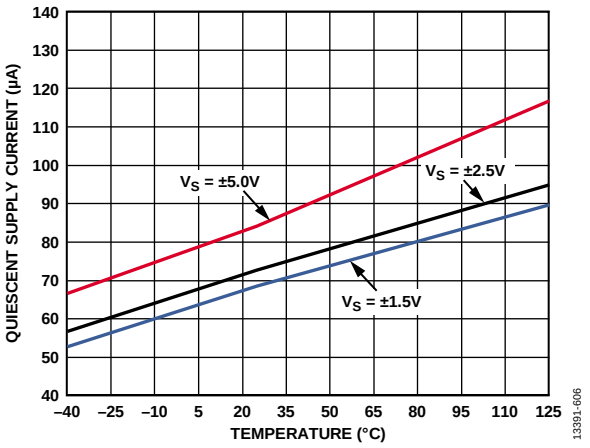


Figure 44. Sleep Mode Quiescent Supply Current vs. Temperature

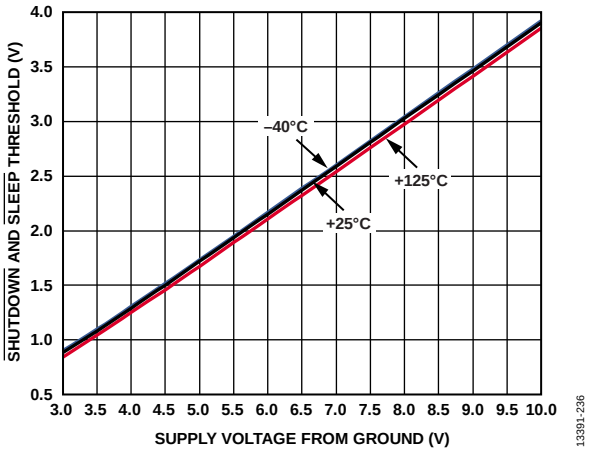


Figure 42. $\overline{SHUTDOWN}$ and $\overline{SLEEP}$ Threshold vs. Supply Voltage from Ground for Various Temperatures

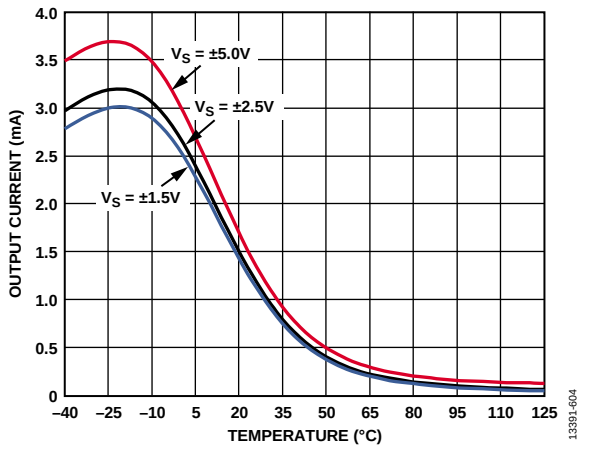


Figure 45. Sleep Mode Output Current vs. Temperature

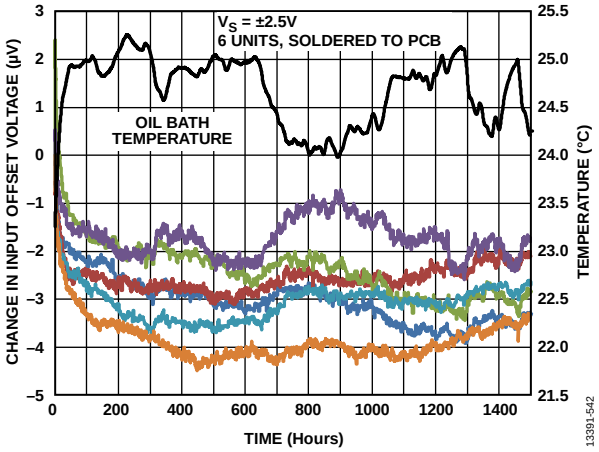


Figure 43. Long-Term V_{OS} Drift

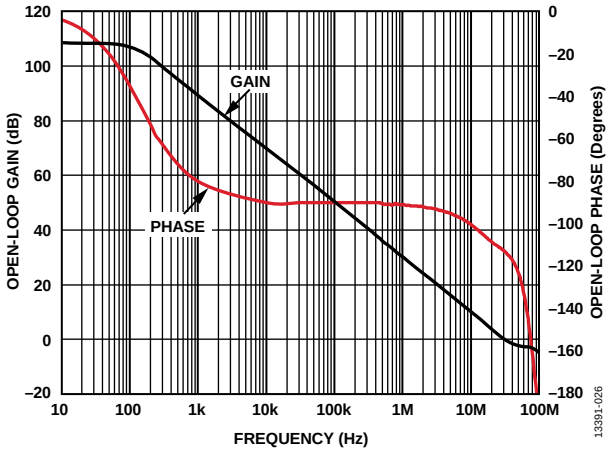


Figure 46. Open-Loop Gain and Phase Margin

TEST CIRCUITS

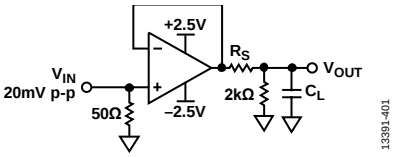


Figure 47. Output Capacitive Load Behavior Test Circuit (See Figure 11)

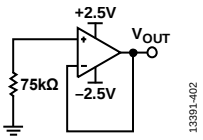


Figure 48. Current Noise Test Circuit (See Figure 20)

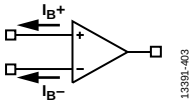


Figure 49. Input Bias Current Temperature Test Circuit (See Figure 25)

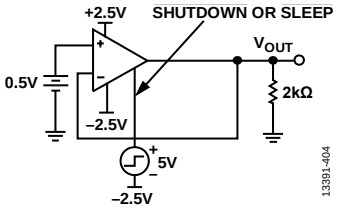


Figure 50. Turn-On Response Test Circuit (See Figure 31 and Figure 34)

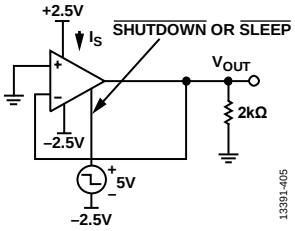


Figure 51. Turn-Off Response Test Circuit (See Figure 35 and Figure 38)

THEORY OF OPERATION

AMPLIFIER DESCRIPTION

The ADA4806-1 has a bandwidth of 105 MHz and a slew rate of 160 V/µs. It has an input referred voltage noise of only 5.9 nV/√Hz. The ADA4806-1 operates over a supply voltage range of 2.7 V to 10 V and consumes only 500 µA of supply current at V_S = 5 V. The low end of the supply range allows −10% variation of a 3 V supply. The amplifier is unity-gain stable, and the input structure results in an extremely low input 1/f noise. The ADA4806-1 uses a slew enhancement architecture, as shown in Figure 52. The slew enhancement circuit detects the absolute difference between the two inputs. It then modulates the tail current, I_{TAIL}, of the input stage to boost the slew rate. The architecture allows a higher slew rate and fast settling time with low quiescent current while maintaining low noise.

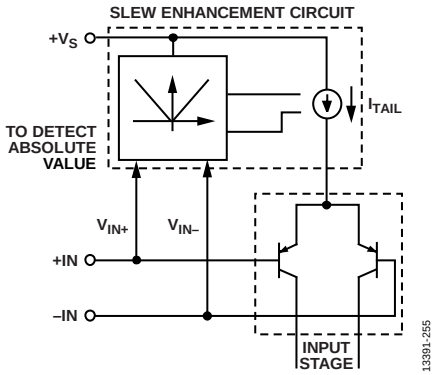


Figure 52. Slew Enhancement Circuit

INPUT PROTECTION

The ADA4806-1 is fully protected from ESD events, withstanding human body model ESD events of ±3.5 kV and charged device model events of ±1.25 kV with no measured performance degradation. The precision input is protected with an ESD network between the power supplies and diode clamps across the input device pair, as shown in Figure 53.

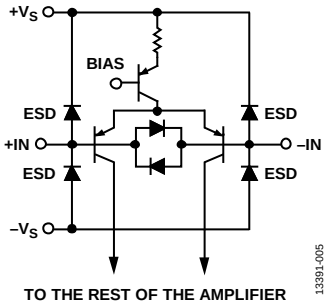


Figure 53. Input Stage and Protection Diodes

For differential voltages above approximately 1.2 V at room temperature, and 0.8 V at 125°C, the diode clamps begin to conduct. If large differential voltages must be sustained across the input terminals, the current through the input clamps must be limited to less than 10 mA. Series input resistors that are sized appropriately for the expected differential overvoltage provide the needed protection.

The ESD clamps begin to conduct for input voltages that are more than 0.7 V above the positive supply and input voltages more than 0.7 V below the negative supply. If an overvoltage condition is expected, the input current must be limited to less than 10 mA.

SHUTDOWN/SLEEP MODE OPERATION

Figure 54 shows the ADA4806-1 shutdown circuitry. To maintain very low supply current in shutdown mode, no internal pull-up resistor is supplied; therefore, the $\overline{\text{SHUTDOWN}}$ pin must be driven high or low externally and must not be left floating. Pulling the $\overline{\text{SHUTDOWN}}$ pin to ≥1 V below midsupply turns the device off, reducing the supply current to 2.9 µA for a 5 V supply. When the amplifier is powered down, its output enters a high impedance state. The output impedance decreases as frequency increases. In shutdown mode, a forward isolation of −62 dB can be achieved at 100 kHz (see Figure 21).

A second circuit similar to Figure 54 is used for sleep mode operation. Pulling the $\overline{\text{SLEEP}}$ pin low places the amplifier in a low power state, drawing only 74 µA from a 5 V supply. Leaving the amplifier biased on at a very low level greatly reduces the turn-on time from sleep to full power mode, thus enabling dynamic power scaling of the ADA4806-1 at higher sample rates.

The ADA4806-1 is not characterized for operation in sleep mode.

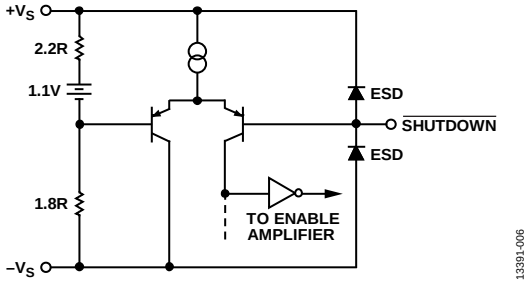


Figure 54. Shutdown/Sleep Equivalent Circuit

The $\overline{\text{SHUTDOWN}}$ pin and the $\overline{\text{SLEEP}}$ pin are protected by ESD clamps, as shown in Figure 54. Voltages beyond the power supplies cause these diodes to conduct. To protect the $\overline{\text{SHUTDOWN}}$ and $\overline{\text{SLEEP}}$ pins, ensure that the voltage to these pins does not exceed 0.7 V above the positive supply or 0.7 V below the negative supply. If an overvoltage condition is expected, the input current must be limited to less than 10 mA with a series resistor.

Table 8 summarizes the threshold voltages for the $\overline{\text{SHUTDOWN}}$ and $\overline{\text{SLEEP}}$ pins for various supplies. Table 9 shows the truth table for the $\overline{\text{SHUTDOWN}}$ and $\overline{\text{SLEEP}}$ pins.

Table 8. Threshold Voltages for Enabled Mode and Shutdown/Sleep Modes

Mode	+3 V	+5 V	±5 V	+7 V/−2 V
Enabled	>+1.1 V	>+1.9 V	>−0.9 V	>+1.6 V
Shutdown/Sleep Mode	<+0.7 V	<+1.5 V	<−1.3 V	<+1.2 V

Table 9. Truth Table for the $\overline{\text{SHUTDOWN}}$ and $\overline{\text{SLEEP}}$ Pins

$\overline{\text{SHUTDOWN}}$	$\overline{\text{SLEEP}}$	Operating State
Low	Low	Powered down
Low	High	Powered down
High	Low	Low power mode
High	High	Full power mode

NOISE CONSIDERATIONS

Figure 55 shows the primary noise contributors for the typical gain configurations. The total output noise (v_{n_OUT}) is the root sum square of all the noise contributions.

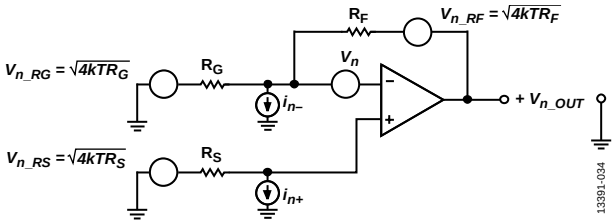


Figure 55. Noise Sources in Typical Connection

The output noise spectral density is calculated by

$$v_{n\_OUT} = \sqrt{4kTR_F + \left(1+\frac{R_F}{R_G}\right)^2 \left[4kTRs + i_{n+}{}^2 R_S{}^2 + v_n{}^2\right] + \left(\frac{R_F}{R_G}\right)^2 4kTR_G + i_{n-}{}^2 R_F{}^2}$$

where:
k is Boltzmann's constant.
T is the absolute temperature in degrees Kelvin.
R_F and R_G are the feedback network resistances, as shown in Figure 55.
R_S is the source resistance, as shown in Figure 55.
i_{n+} and i_{n-} represent the amplifier input current noise spectral density in pA/√Hz.
v_n is the amplifier input voltage noise spectral density in nV/√Hz.

Source resistance noise, amplifier input voltage noise (v_n), and the voltage noise from the amplifier input current noise ($i_{n+} \times R_S$) are all subject to the noise gain term ($1 + R_F/R_G$).

Figure 56 shows the total referred to input (RTI) noise due to the amplifier vs. the source resistance. Note that with a 5.9 nV/√Hz input voltage noise and 0.6 pA/√Hz input current noise, the noise contributions of the amplifier are relatively small for source resistances from approximately 2.6 kΩ to 47 kΩ.

The Analog Devices, Inc., silicon germanium (SiGe) bipolar process makes it possible to achieve a low noise of 5.9 nV/√Hz for the ADA4806-1. This noise is much improved compared to similar low power amplifiers with a supply current in the range of hundreds of microamperes.

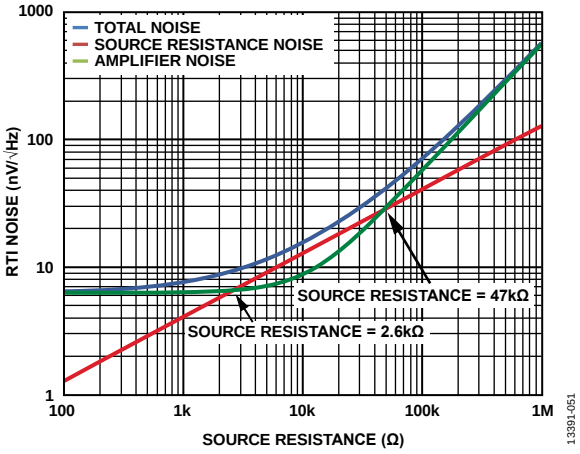


Figure 56. RTI Noise vs. Source Resistance

APPLICATIONS INFORMATION

SLEW ENHANCEMENT

The ADA4806-1 has an internal slew enhancement circuit that increases the slew rate as the feedback error voltage increases. This circuit allows the amplifier to settle a large step response faster, as shown in Figure 57. This is useful in ADC applications where multiple input signals are multiplexed. The impact of the slew enhancement can also be seen in the large signal frequency response, where larger input signals cause a slight increase in peaking, as shown in Figure 58.

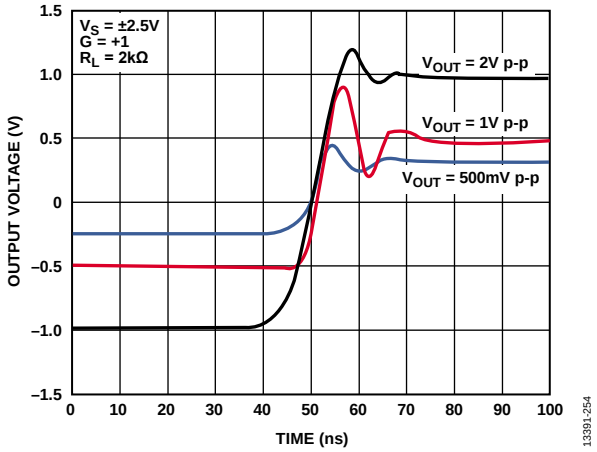


Figure 57. Step Response with Selected Output Steps

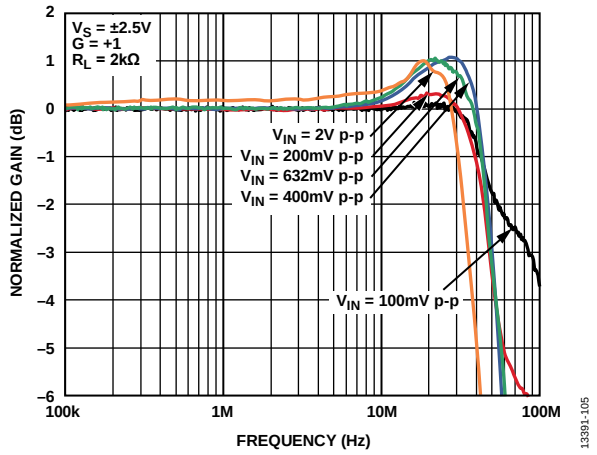


Figure 58. Peaking in Frequency Responses as Signal Level Changes, G = +1

EFFECT OF FEEDBACK RESISTOR ON FREQUENCY RESPONSE

The amplifier input capacitance and feedback resistor form a pole that, for larger value feedback resistors, can reduce phase margin and contribute to peaking in the frequency response. Figure 59 shows the peaking for selected feedback resistors (R_F) when the amplifier is configured in a gain of +2. Figure 59 also shows how peaking can be mitigated with the addition of a small value capacitor placed across the feedback resistor of the amplifier.

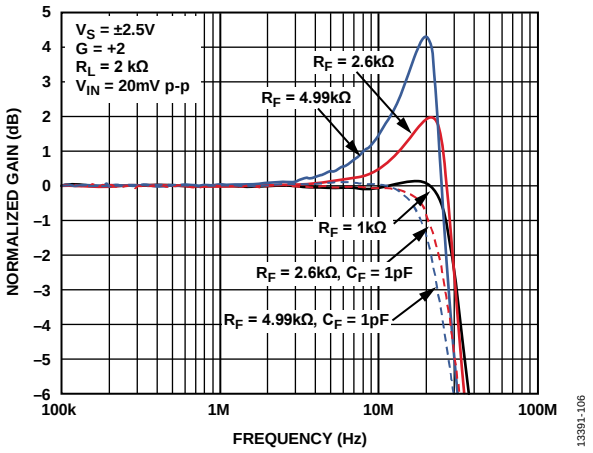


Figure 59. Peaking in Frequency Response at Selected R_F Values

COMPENSATING PEAKING IN LARGE SIGNAL FREQUENCY RESPONSE

At high frequency, the slew enhancement circuit can contribute to peaking in the large signal frequency response. Figure 59 shows the effect of a feedback capacitor on the small signal response, whereas Figure 60 shows that the same technique is effective for reducing peaking in the large signal response.

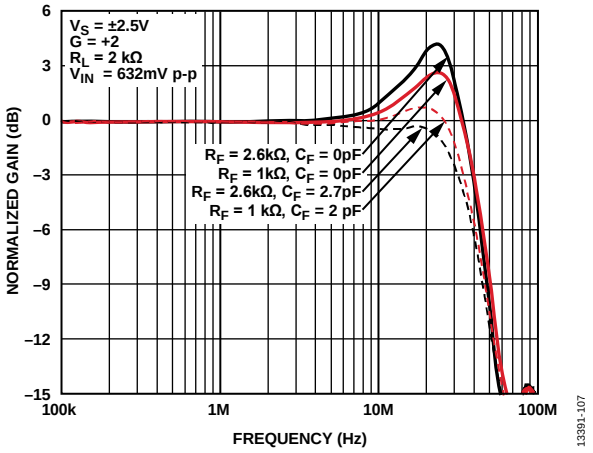


Figure 60. Peaking Mitigation in Large Signal Frequency Response

DRIVING LOW POWER, HIGH RESOLUTION SUCCESSIVE APPROXIMATION REGISTER (SAR) ADCs

The ADA4806-1 is ideal for driving low power, high resolution SAR ADCs. The 5.9 nV/√Hz input voltage noise and rail-to-rail output stage of the ADA4806-1 help minimize distortion at large output levels. With its low power of 500 µA, the amplifier consumes power that is compatible with low power SAR ADCs, which are usually in the microwatt (µW) to low milliwatt (mW) range. Furthermore, the ADA4806-1 supports a single-supply configuration; the input common-mode range extends to 0.1 V below the negative supply, and 1 V below the positive supply.

Figure 61 shows a typical 16-bit, single-supply application. The ADA4806-1 drives the AD7980, a 16-bit, 1 MSPS, SAR ADC in a low power configuration. The AD7980 operates on a 2.5 V supply and supports an input from 0 V to V_{REF}. In this case, the ADR435 provides a 5 V reference. The ADA4806-1 is used both as a driver for the AD7980 and as a reference buffer for the ADR435.

The low-pass filter formed by R3 and C1 reduces the noise to the input of the ADC (see Figure 61). In lower frequency applications, the designer can reduce the corner frequency of the filter to remove additional noise.

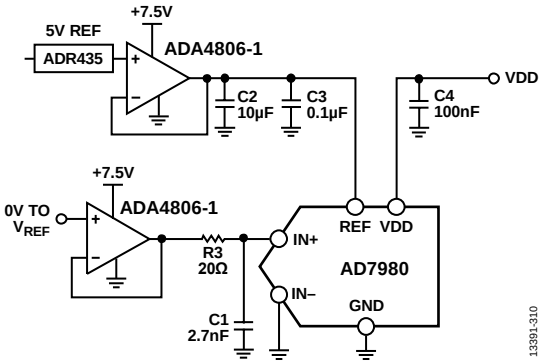


Figure 61. Driving the AD7980 with the ADA4806-1

In this configuration, the ADA4806-1 consume 7.2 mW of quiescent power. The measured signal-to-noise ratio (SNR), THD, and signal-to-noise-and-distortion ratio (SINAD) of the whole system for a 10 kHz signal are 89.4 dB, 104 dBc, and 89.3 dB, respectively. This translates to an effective number of bits (ENOB) of 14.5 at 10 kHz, which is compatible with the AD7980 performance. Table 10 shows the performance of this setup at selected input frequencies.

DYNAMIC POWER SCALING

One of the merits of a SAR ADC, like the AD7980, is that its power scales with the sampling rate. This power scaling makes SAR ADCs very power efficient, especially when running at a low sampling frequency. However, the ADC driver used with the SAR ADC traditionally consumes constant power regardless of the sampling frequency.

Figure 62 illustrates a method by which the quiescent power of the ADC driver can be dynamically scaled with the sampling rate of the system. By providing properly timed signals to the convert input (CNV) pin of the ADC and the $\overline{\text{SHUTDOWN}}$ and $\overline{\text{SLEEP}}$ pins of the ADA4806-1, both devices can be run at optimum efficiency.

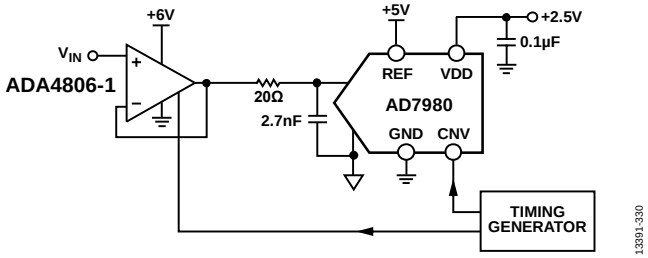


Figure 62. ADA4806-1/AD7980 Power Management Circuitry

Figure 63 illustrates the relative signal timing for power scaling the ADA4806-1 and the AD7980. To prevent any degradation in the performance of the ADC, the ADA4806-1 must have a fully settled output into the ADC before the activation of the CNV pin. The amplifier on-time ($t_{AMP,ON}$) is the time the amplifier is enabled prior to the rising edge of the CNV signal; this time depends on whether the $\overline{\text{SHUTDOWN}}$ pin or $\overline{\text{SLEEP}}$ pin is being driven. In the example shown in Figure 64, $t_{AMP,ON}$ is 3 µs for the $\overline{\text{SHUTDOWN}}$ pin and 0.5 µs for the $\overline{\text{SLEEP}}$ pin. After a conversion, the $\overline{\text{SHUTDOWN}}$ pin and/or the $\overline{\text{SLEEP}}$ pin of the ADA4806-1 are pulled low when the ADC input is inactive in between samples. While in shutdown mode, the ADA4806-1 output impedance is high.

Table 10. System Performance at Selected Input Frequencies for Driving the AD7980 Single-Ended

	ADC Driver		Reference Buffer		Results			
Input Frequency (kHz)	Supply (V)	Gain	Supply (V)	Gain	SNR (dB)	THD (dBc)	SINAD (dB)	ENOB
1	7.5	1	7.5	1	89.8	103	89.6	14.6
10	7.5	1	7.5	1	89.4	104	89.3	14.5
20	7.5	1	7.5	1	89.9	103	89.7	14.6
50	7.5	1	7.5	1	88.5	99	88.1	14.3
100	7.5	1	7.5	1	86.3	93.7	85.6	13.9

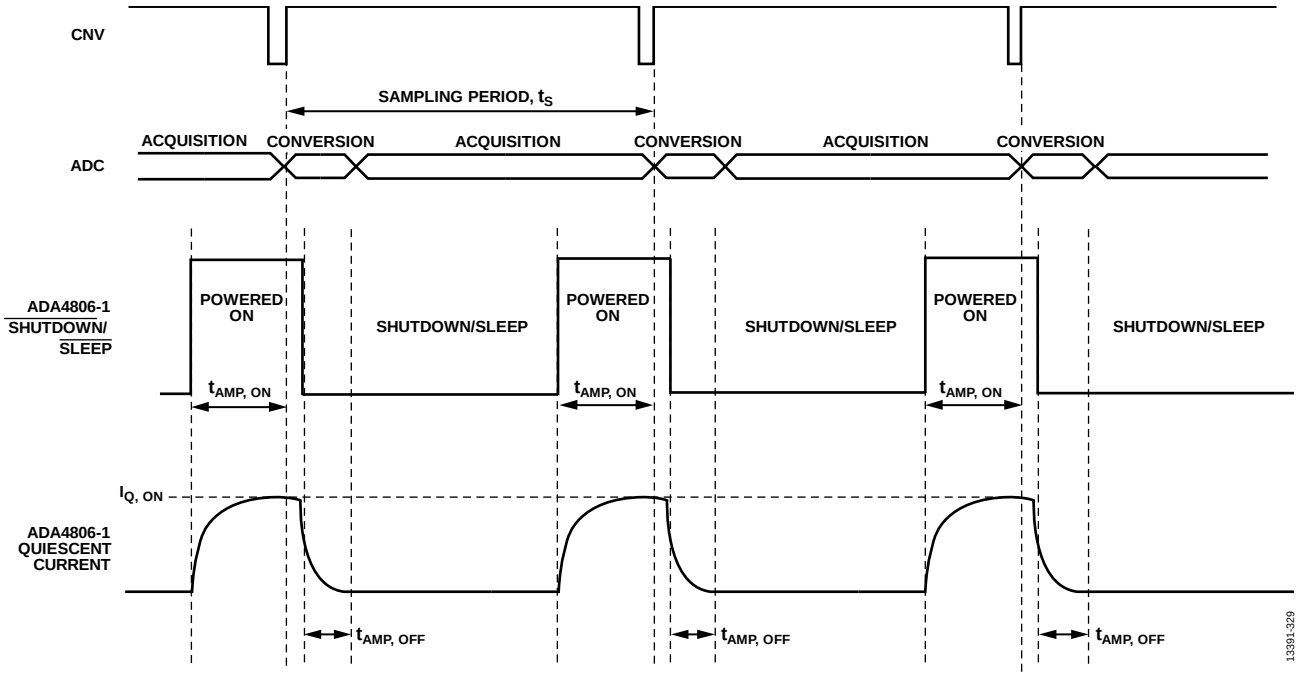


Figure 63. Timing Waveforms

Figure 64 shows the quiescent power of the ADA4806-1, operating from a single +6 V supply, without power scaling and while power scaling via the $\overline{\text{SHUTDOWN}}$ pin and the $\overline{\text{SLEEP}}$ pin. Without power scaling, the ADA4806-1 consumes constant power regardless of the sampling frequency, as shown in Equation 1.

$$P_Q = I_Q \times V_S \quad (1)$$

With power scaling, the quiescent power becomes proportional to the ratio between the amplifier on time, $t_{AMP, ON}$, and the sampling time, t_S:

$$P_Q = \left(I_{Q\_on} \times V_S \times \frac{t_{AMP,ON}}{t_S} \right) + \left(I_{Q\_off} \times V_S \times \frac{t_S - t_{AMP,ON}}{t_S} \right) \quad (2)$$

Thus, by dynamically switching the ADA4806-1 between shutdown/sleep and full power modes between consecutive samples, the quiescent power of the driver scales with the sampling rate.

Note that $t_{AMP, ON}$ in Figure 64 is 3 µs for the $\overline{\text{SHUTDOWN}}$ pin and 0.5 µs for the $\overline{\text{SLEEP}}$ pin.

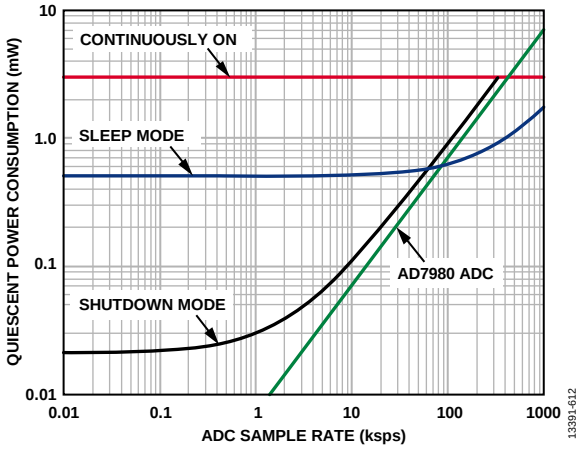


Figure 64. Quiescent Power Consumption of the ADA4806-1 vs. ADC Sample Rate, Using Dynamic Power Scaling

SINGLE-ENDED TO DIFFERENTIAL CONVERSION

Most high resolution ADCs have differential inputs to reduce common-mode noise and harmonic distortion. Therefore, it is necessary to use an amplifier to convert a single-ended signal into a differential signal to drive the ADCs.

There are two common ways the user can convert a single-ended signal into a differential signal: either use a differential amplifier, or configure two amplifiers as shown in Figure 65. The use of a differential amplifier yields better performance, whereas the 2-op-amp solution results in lower system cost. The ADA4806-1 solves this dilemma of choosing between the two methods by combining the advantages of both. Its low harmonic distortion, low offset voltage, and low bias current mean that it can produce a differential output that is well matched with the performance of the high resolution ADCs.

Figure 65 shows how the ADA4806-1 converts a single-ended signal into a differential output. The first amplifier is configured in a gain of +1 with its output then inverted to produce the complementary signal. The differential output then drives the AD7982, an 18-bit, 1 MSPS SAR ADC. To further reduce noise, the user can reduce the values of R1 and R2. However, note that this increases the power consumption. The low-pass filter of the ADC driver limits the noise to the ADC.

The measured SNR, THD, and SINAD of the whole system for a 10 kHz signal are 93 dB, 113 dBc, and 93 dB, respectively. This translates to an ENOB of 15.1 at 10 kHz, which is compatible with the performance of the AD7982. Table 11 shows the performance of this setup at selected input frequencies.

Table 11. System Performance at Selected Input Frequencies for Driving the AD7982 Differentially

	Results			
Input Frequency (kHz)	SNR (dB)	THD (dBc)	SINAD (dB)	ENOB
1	93	104	93	15.1
10	93	113	93	15.1
20	93	110	93	15.1
50	92	102	91	14.8
100	89	96	88	14.3

LAYOUT CONSIDERATIONS

To ensure optimal performance, careful and deliberate attention must be paid to the board layout, signal routing, power supply bypassing, and grounding.

Ground Plane

It is important to avoid ground in the areas under and around the input and output of the ADA4806-1. Stray capacitance between the ground plane and the input and output pads of a device is detrimental to high speed amplifier performance. Stray capacitance at the inverting input, together with the amplifier input capacitance, lowers the phase margin and can cause instability. Stray capacitance at the output creates a pole in the feedback loop, which can reduce phase margin and cause the circuit to become unstable.

Power Supply Bypassing

Power supply bypassing is a critical aspect in the performance of the ADA4806-1. A parallel connection of capacitors from each power supply pin to ground works best. Smaller value ceramic capacitors offer better high frequency response, whereas larger value ceramic capacitors offer better low frequency performance.

Paralleling different values and sizes of capacitors helps to ensure that the power supply pins are provided with a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier—especially when the amplifier PSRR begins to roll off—because the bypass capacitors can help lessen the degradation in PSRR performance.

Place the smallest value capacitor on the same side of the board as the amplifier and as close as possible to the amplifier power supply pins. Connect the ground end of the capacitor directly to the ground plane.

It is recommended that a 0.1 µF ceramic capacitor with a 0508 case size be used. The 0508 case size offers low series inductance and excellent high frequency performance. Place a 10 µF electrolytic capacitor in parallel with the 0.1 µF capacitor. Depending on the circuit parameters, some enhancement to performance can be realized by adding additional capacitors. Each circuit is different and must be analyzed individually for optimal performance.

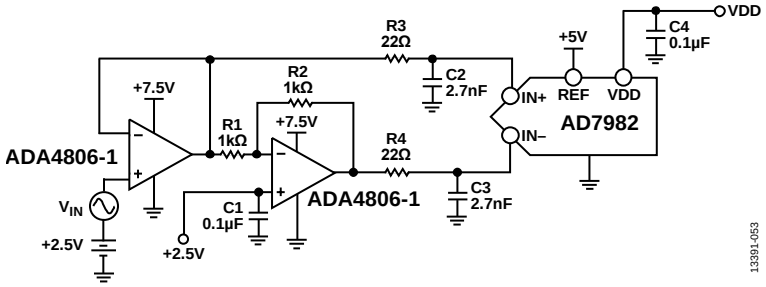
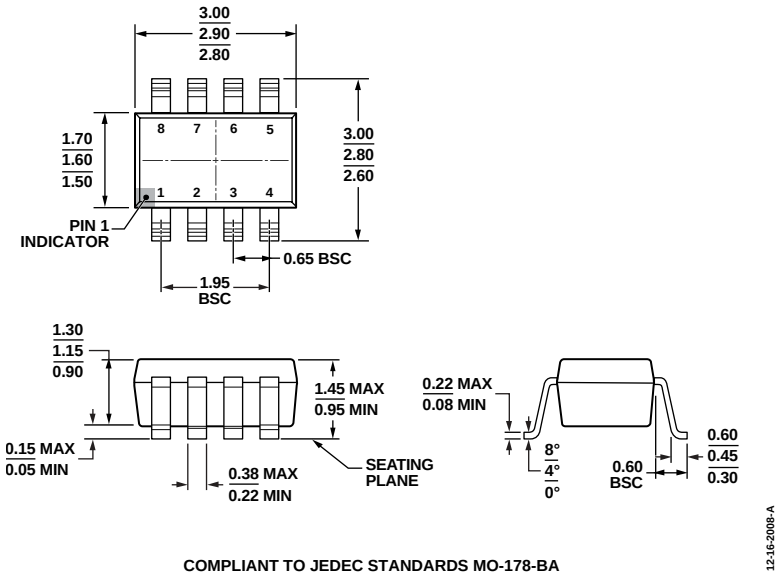


Figure 65. Driving the AD7982 with the ADA4806-1

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 66. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4806-1ARJZ-R2	−40°C to +125°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8
ADA4806-1ARJZ-R7	−40°C to +125°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8
ADA4806-1RJ-EBZ		Evaluation Board for 8-Lead SOT-23	

[1] Z = RoHS Compliant Part.

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