HEF40373B

Octal transparent latch with 3-state outputs

Rev. 4 — 29 June 2018 Product data sheet

1 General description

The HEF40373B is an 8-bit transparent latch with 3-state buffered outputs. The output stages have high current output capability suitable for driving highly capacitive loads. The latch outputs follow the data inputs when the latch enable (E) is HIGH. When E is LOW, the data that meets the set-up times is latched. The 3-state outputs are controlled by the output enable input $\overline{EO}$. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device features hysteresis on the E input to improve noise rejection. Schmitt-trigger action in the E input makes the circuit highly tolerant to slower input rise and fall times.

2 Features and benefits

- Octal bus interface
- 3-state buffers
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF40373BT	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

nexperia

4 Functional diagram

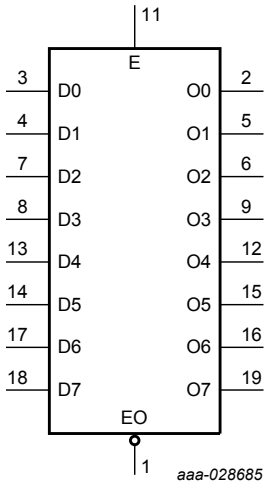


Figure 1. Logic symbol

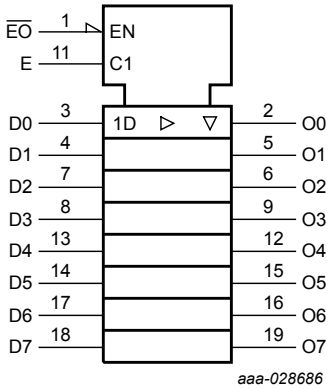


Figure 2. IEC logic symbol

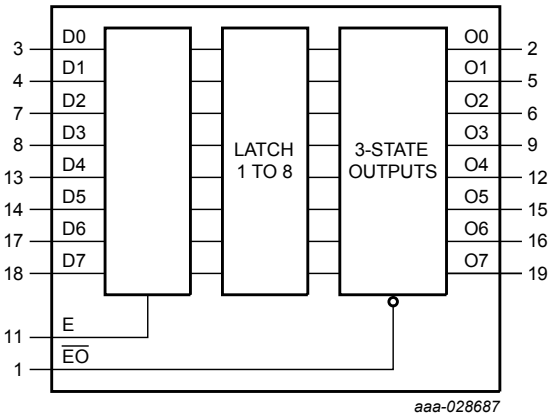


Figure 3. Functional diagram

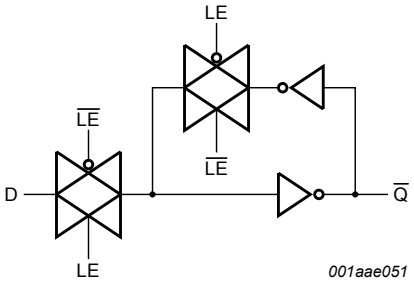


Figure 4. Logic diagram (one latch)

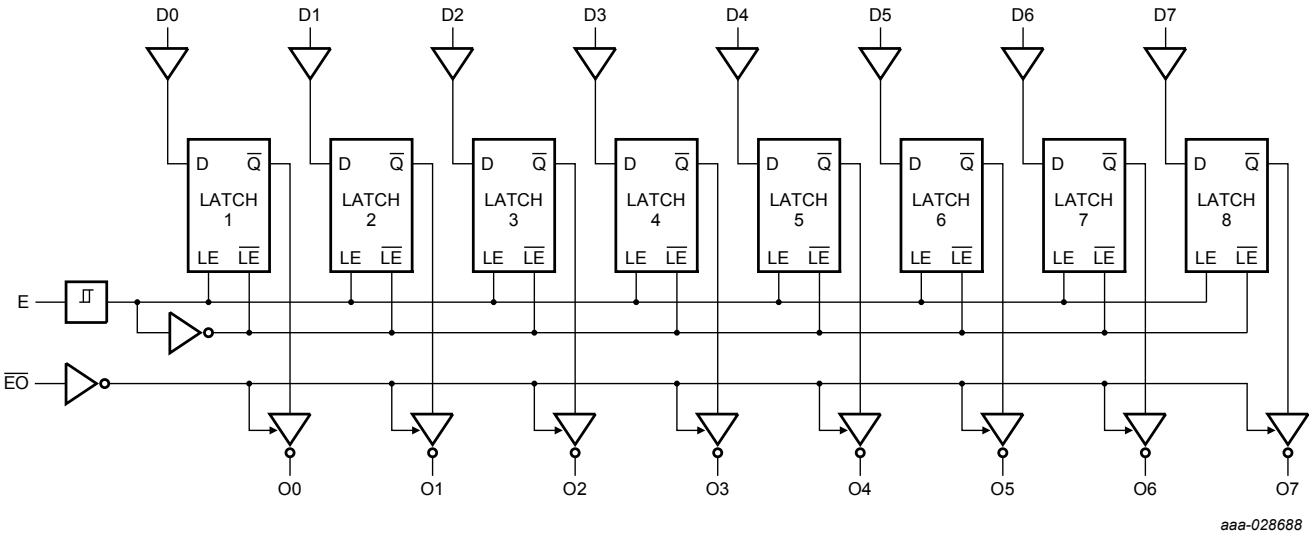


Figure 5. Logic diagram

5 Pinning information

5.1 Pinning

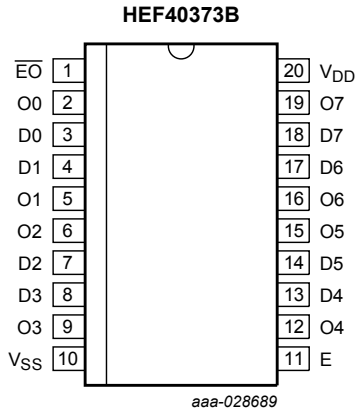


Figure 6. Pin configuration for SO20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{EO}$	1	output enable input (active low)
E	11	latch enable input
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data inputs
O0, O1, O2, O3, O4, O5, O6, O7	2, 5, 6, 9, 12, 15, 16, 19	data outputs
V_{SS}	10	ground supply voltage
V_{DD}	20	supply voltage

6 Functional description

Table 3. Function table [1]

Operating mode	Inputs			Internal latches	Outputs On
	$\overline{EO}$	E	Dn		
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	↓	l	L	L
	L	↓	h	H	H
Hold	L	L	X	NC	NC
Latch register and disable outputs	H	L	X	NC	Z
	H	H	nDn	nDn	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
↓ = HIGH-to-LOW E transition;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW E transition;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW E transition;
X = don't care;
NC = No change;
Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{DD}	supply current		-	±100	mA
I_{IK}	input clamping current		-	±10	mA
I_{OK}	output clamping current		-	±25	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C			
		SO20 package [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SO20 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8 Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	referenced to V_{SS} (usually ground)	3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	3.75	μs/V
		V_{DD} = 10 V	-	0.5	μs/V
		V_{DD} = 15 V	-	0.08	μs/V

9 Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions		T_{amb} = -40 °C		T_{amb} = 25 °C			T_{amb} = 85 °C		Unit
			V_{DD}	Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 μA									
		V_O = 0.5 V or 4.5 V	5 V	3.5	-	3.5	-	-	3.5	-	V
		V_O = 1.0 V or 9.0 V	10 V	7.0	-	7.0	-	-	7.0	-	V
		V_O = 1.5 V or 13.5 V	15 V	11.0	-	11.0	-	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 μA									
		V_O = 0.5 V or 4.5 V	5 V	-	1.5	-	-	1.5	-	1.5	V
		V_O = 1.0 V or 9.0 V	10 V	-	3.0	-	-	3.0	-	3.0	V
		V_O = 1.5 V or 13.5 V	15 V	-	4.0	-	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 μA	5 V	4.95	-	4.95	-	-	4.95	-	V
			10 V	9.95	-	9.95	-	-	9.95	-	V
			15 V	14.95	-	14.95	-	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 μA	5 V	-	0.05	-	-	0.05	-	0.05	V
			10 V	-	0.05	-	-	0.05	-	0.05	V
			15 V	-	0.05	-	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	see Figure 7 and Figure 8.									
		V_{OH} = 3.6 V	5 V	−9.3	-	−10	−24	-	−10.7	-	mA
		V_{OH} = 4.6 V	5 V	−0.75	-	−0.6	−1.2	-	−0.45	-	mA
		V_{OH} = 8.4 V	10 V	−14.4	-	−15	−46	-	−15	-	mA
		V_{OH} = 9.5 V	10 V	−1.85	-	−1.5	−3.0	-	−1.1	-	mA
		V_{OH} = 13.2 V	15 V	−19.5	-	−20	−62	-	−19.8	-	mA
		V_{OH} = 13.5 V	15 V	−14.5	-	−15	−50	-	−15.5	-	mA

Symbol	Parameter	Conditions		T_{amb} = -40 °C		T_{amb} = 25 °C			T_{amb} = 85 °C		Unit
			V_{DD}	Min	Max	Min	Typ	Max	Min	Max	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	5 V	2.9	-	2.3	5.4	-	1.75	-	mA
		V_{OL} = 0.5 V	10 V	9.5	-	7.6	17	-	5.5	-	mA
		V_{OL} = 1.5 V	15 V	30.0	-	25	45	-	19.0	-	mA
I_I	input leakage current	[1]	15 V	-	±0.3	-	-	±0.3	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_O = V_{DD}$	15 V	-	1.6	-	-	1.6	-	12.0	µA
		$V_O = V_{SS}$	15 V	-	−1.6	-	-	−1.6	-	−12.0	µA
I_{DD}	supply current	I_O = 0 A	5 V	-	20.0	-	-	20.0	-	150	µA
			10 V	-	40.0	-	-	40.0	-	300	µA
			15 V	-	80.0	-	-	80.0	-	600	µA
V_H	hysteresis voltage	E input	5 V	-	-	-	220	-	-	-	mV
			10 V	-	-	-	250	-	-	-	mV
			15 V	-	-	-	320	-	-	-	mV
C_I	input capacitance			-	-	-	7.5	-	-	-	pF

[1] Unused inputs must be connected to V_{DD}, V_{SS} or another input.

10 Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified; for waveform and test circuit, see Figure 13.

Symbol	Parameter	Conditions	Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	E to On; see Figure 9. [1]					
		V_{DD} = 5 V	138 ns + (0.24 ns/pF)C_L	-	150	300	ns
		V_{DD} = 10 V	59 ns + (0.01 ns/pF)C_L	-	60	120	ns
		V_{DD} = 15 V	36 ns + (0.07 ns/pF)C_L	-	40	80	ns
t_{PLH}	LOW to HIGH propagation delay	E to On; see Figure 9. [1]					
		V_{DD} = 5 V	122 ns + (0.06 ns/pF)C_L	-	125	250	ns
		V_{DD} = 10 V	48 ns + (0.03 ns/pF)C_L	-	50	100	ns
		V_{DD} = 15 V	39 ns + (0.02 ns/pF)C_L	-	40	60	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{EO}$ to On; see Figure 11.					
		V_{DD} = 5 V		-	65	130	ns
		V_{DD} = 10 V		-	30	60	ns
		V_{DD} = 15 V		-	25	50	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{EO}$ to On; see Figure 11.					
		V_{DD} = 5 V		-	85	170	ns
		V_{DD} = 10 V		-	35	70	ns
		V_{DD} = 15 V		-	25	50	ns

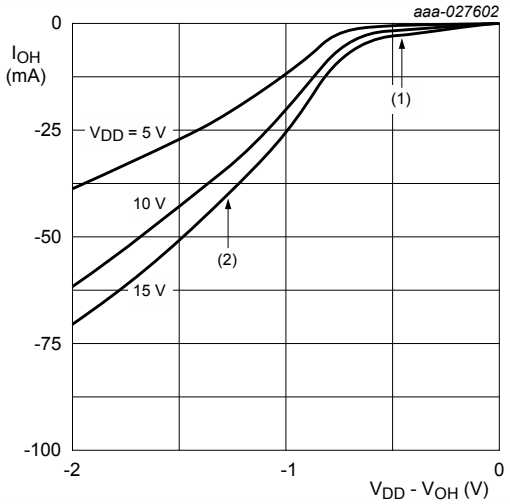
Symbol	Parameter	Conditions	Extrapolation formula	Min	Typ	Max	Unit
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{EO}$ to On; see Figure 11.					
		V_{DD} = 5 V		-	65	130	ns
		V_{DD} = 10 V		-	30	60	ns
		V_{DD} = 15 V		-	25	50	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{EO}$ to On; see Figure 11.					
		V_{DD} = 5 V		-	75	150	ns
		V_{DD} = 10 V		-	40	80	ns
		V_{DD} = 15 V		-	30	60	ns
t_{THL}	HIGH to LOW output transition time	On; see Figure 9 and Figure 10.					
		V_{DD} = 5 V		-	40	80	ns
		V_{DD} = 10 V		-	20	40	ns
		V_{DD} = 15 V		-	15	30	ns
t_{TLH}	LOW to HIGH output transition time	On; see Figure 9 and Figure 10.					
		V_{DD} = 5 V		-	30	60	ns
		V_{DD} = 10 V		-	20	40	ns
		V_{DD} = 15 V		-	15	30	ns
t_{su}	set-up time	Dn to E; see Figure 12.					
		V_{DD} = 5 V		15	7	-	ns
		V_{DD} = 10 V		10	5	-	ns
		V_{DD} = 15 V		10	5	-	ns
t_h	hold time	Dn to E; see Figure 12.					
		V_{DD} = 5 V		25	15	-	ns
		V_{DD} = 10 V		15	4	-	ns
		V_{DD} = 15 V		10	3	-	ns
t_W	pulse width	E; LOW; see Figure 13.					
		V_{DD} = 5 V		60	30	-	ns
		V_{DD} = 10 V		30	15	-	ns
		V_{DD} = 15 V		20	10	-	ns

[1] The typical values of the propagation delay are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation

Symbol	Parameter	V_{DD}	Typical formula	where:
P_D	dynamic power dissipation	5 V	$P_D = 3325 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.
		10 V	$P_D = 14200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	
		15 V	$P_D = 37425 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	

10.1 Waveforms and test circuit



(1) P-channel MOS transistor conducting.

(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

Figure 7. Typical output source current characteristic.

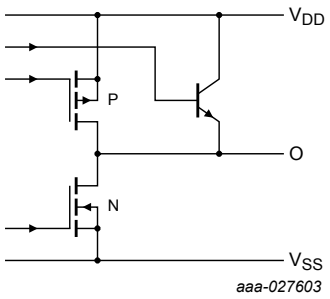
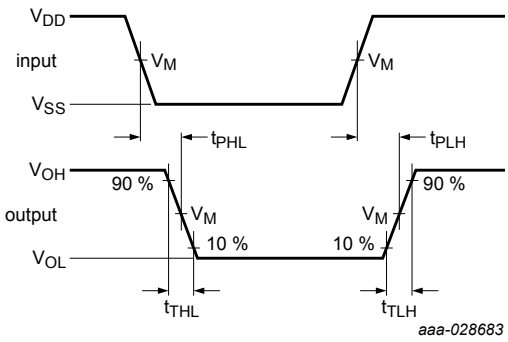


Figure 8. Schematic diagram of output stage.



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 9. Input to output propagation delays and output transition time.

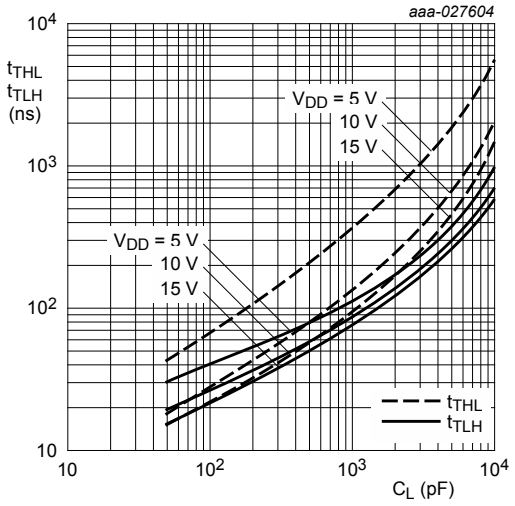
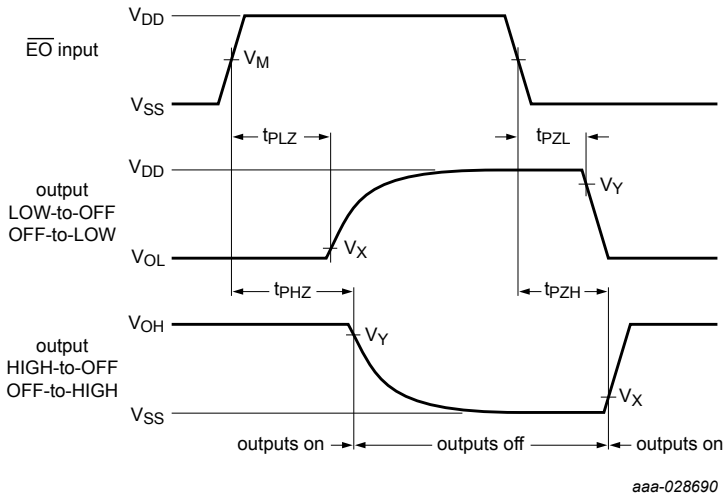


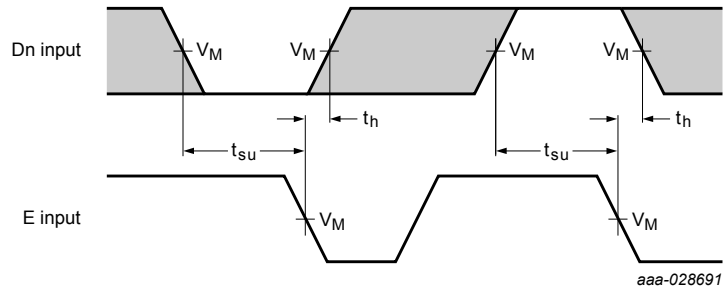
Figure 10. Output transition times as a function of the load capacitance



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 11. 3-state enable and disable times

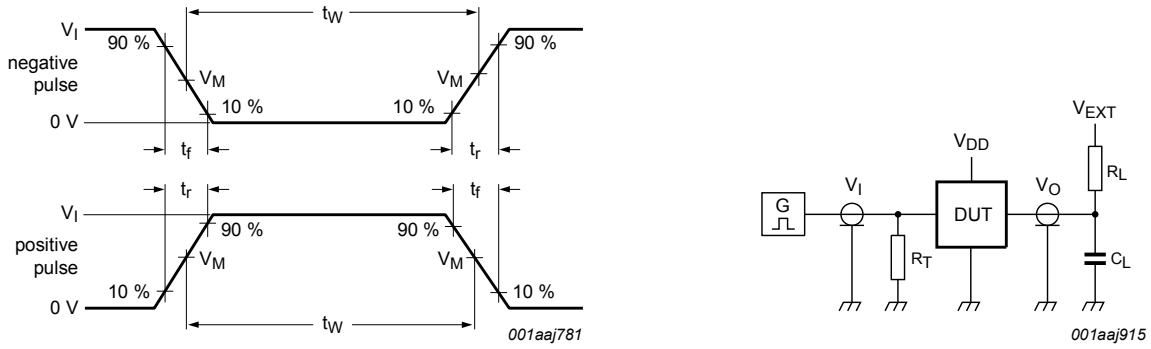


Measurement points are given in Table 9.

Figure 12. Data set-up and hold times for Dn input to E input

Table 9. Measurement points

Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$V_{OL} + 0.1V_{DD}$	$V_{OH} - 0.1V_{DD}$



a. Input waveform

b. Test circuit

Test and measurement data is given in Table 10.

Definitions test circuit:

R_L = Load resistance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

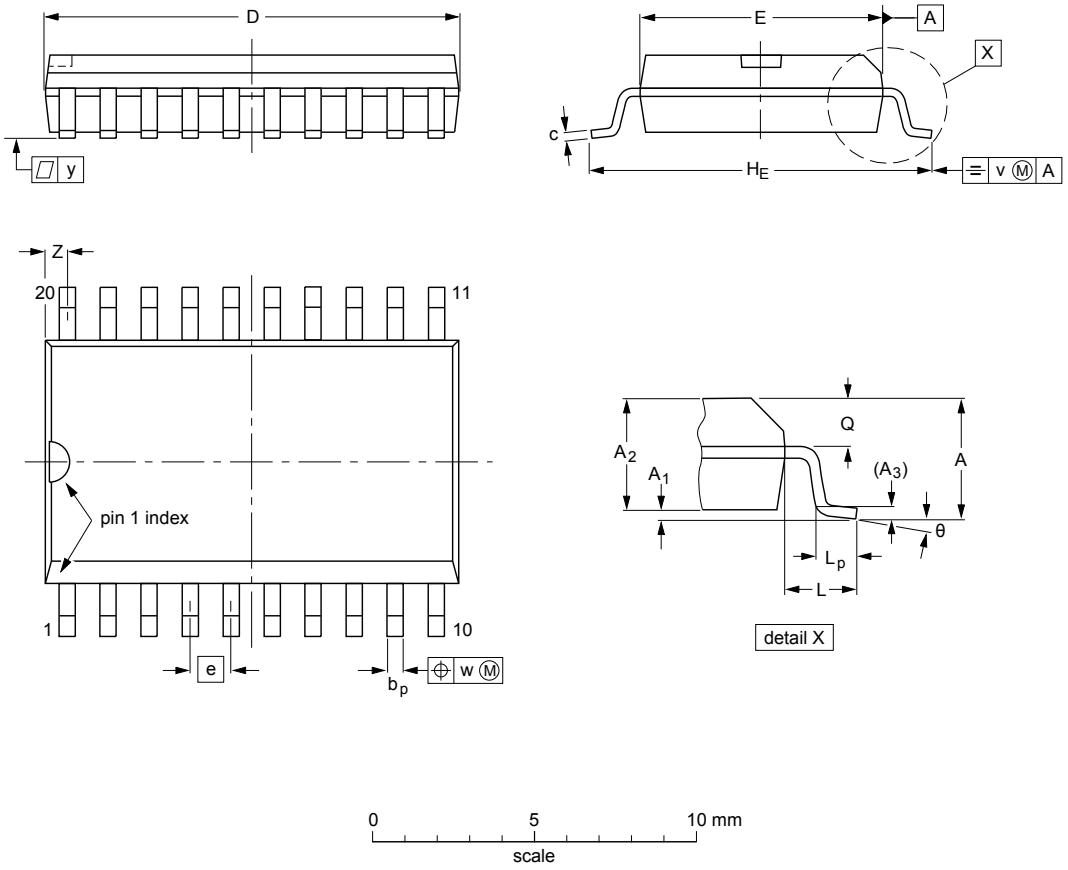
Figure 13. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}
5 V to 15 V	V_{DD}	≤ 20 ns	50 pF	1 kΩ	open	V_{SS}	V_{DD}

11 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Figure 14. Package outline SOT163-1 (SO20)

12 Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test

13 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40373B v.4	20180629	Product data sheet	-	HEF40373B v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
HEF40373B v.3	19950101	Product specification	-	HEF40373B v.2
HEF40373B v.2	19950101	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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