

MC14526B

Presettable 4-Bit Down Counters

The MC14526B binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

This device is presettable, cascadable, synchronous down counter with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Inhibit input allows disabling of the pulse counting function. Inhibit may also be used as a negative edge clock.

This complementary MOS counter can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Design: Incremented on Positive Transition of Clock or Negative Transition of Inhibit
- Asynchronous Preset Enable
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	-0.5 to $V_{DD} + 0.5$	V
Input or Output Current (DC or Transient) per Pin	I_{in}, I_{out}	± 10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Operating Temperature Range	T_A	-55 to +125	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$
Lead Temperature (8-Second Soldering)	T_L	260	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

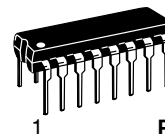
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



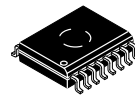
ON Semiconductor®

<http://onsemi.com>

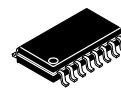
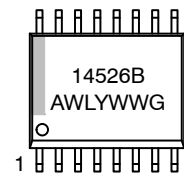
MARKING DIAGRAMS



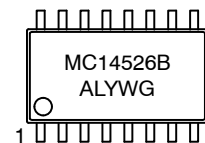
PDIP-16
P SUFFIX
CASE 648



SOIC-16 WB
DW SUFFIX
CASE 751G



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

FUNCTION TABLE

Inputs					Output	Resulting Function
Clock	Reset	Inhibit	Preset Enable	Cascade Feedback	"0"	
X	H	X	L	L	L	Asynchronous reset*
X	H	X	H	L	H	Asynchronous reset
X	H	X	X	H	H	Asynchronous reset
X	L	X	H	X	L	Asynchronous preset
L	L	H	L	X	L	Decrement inhibited
			L	X	L	Decrement inhibited
H	L	L	L	L	L	No change** (inactive edge)
			L	L	L	No change** (inactive edge)
			L	L	L	Decrement**
			L	L	L	Decrement**

X = Don't Care

NOTES:

* Output "0" is low when reset goes high only if PE and CF are low.

** Output "0" is high when reset is low, only if CF is high and count is 0000.

PIN DESCRIPTIONS

Preset Enable (Pin 3) — If Reset is low, a high level on the Preset Enable input asynchronously loads the counter with the programmed values on P0, P1, P2, and P3.

Inhibit (Pin 4) — A high level on the Inhibit input prevents the Clock from decrementing the counter. With Clock (pin 6) held high, Inhibit may be used as a negative edge clock input.

Clock (Pin 6) — The counter decrements by one for each rising edge of Clock. See the Function Table for level requirements on the other inputs.

Reset (Pin 10) — A high level on Reset asynchronously forces Q0, Q1, Q2, and Q3 low and, if Cascade Feedback is high, causes the "0" output to go high.

"0" (Pin 12) — The "0" (Zero) output issues a pulse one clock period wide when the counter reaches terminal count (Q0 = Q1 = Q2 = Q3 = low) if Cascade Feedback is high and Preset Enable is low. When presetting the counter to a value

other than all zeroes, the "0" output is valid after the rising edge of Preset Enable (when Cascade Feedback is high). See the Function Table.

Cascade Feedback (Pin 13) — If the Cascade Feedback input is high, a high level is generated at the "0" output when the count is all zeroes. If Cascade Feedback is low, the "0" output depends on the Preset Enable input level. See the Function Table.

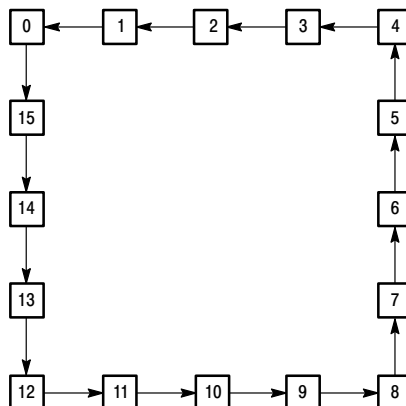
P0, P1, P2, P3 (Pins 5, 11, 14, 2) — These are the preset data inputs. P0 is the LSB.

Q0, Q1, Q2, Q3 (Pins 7, 9, 15, 1) — These are the synchronous counter outputs. Q0 is the LSB.

VSS (Pin 8) — The most negative power supply potential. This pin is usually ground.

VDD (Pin 16) — The most positive power supply potential. VDD may range from 3.0 to 18 V with respect to VSS.

STATE DIAGRAM
MC14526B



MC14526B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level	V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
	"1" Level	V _{IH}	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0 5.0 10 15	-3.0 -0.64 -1.6 -4.2	- - - -	-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8	- - - -	-1.7 -0.36 -0.9 -2.4	- - - -	mAdc
	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current		I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	µAdc
Input Capacitance (V _{in} = 0)		C _{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)			5.0	-	5.0	-	0.005	5.0	-	150	µAdc
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)			5.0	I _T = (1.7 µA/kHz) f + I _{DD}							µAdc
			10	I _T = (3.4 µA/kHz) f + I _{DD}							
			15	I _T = (5.1 µA/kHz) f + I _{DD}							

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

MC14526B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) (Note 5)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ t_{THL} (Figures 4, 5)	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time (Inhibit Used as Negative Edge Clock) Clock or Inhibit to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 135 \text{ ns}$ Clock or Inhibit to "0" $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 155 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	$t_{PLH},$ t_{PHL} (Figures 4, 5, 6)	5.0 10 15	– – –	550 225 160	1100 450 320	ns
		5.0 10 15	– – –	240 130 100	480 260 200	
Propagation Delay Time Pn to Q	$t_{PLH},$ t_{PHL} (Figures 4, 7)	5.0 10 15	– – –	260 120 100	520 240 200	
Propagation Delay Time Reset to Q	t_{PHL} (Figure 8)	5.0 10 15	– – –	250 110 80	500 220 160	ns
Propagation Delay Time Preset Enable to "0"	$t_{PHL},$ t_{PLH} (Figures 4, 9)	5.0 10 15	– – –	220 100 80	440 200 160	ns
Clock or Inhibit Pulse Width	t_w (Figures 5, 6)	5.0 10 15	250 100 80	125 50 40	– – –	ns
Clock Pulse Frequency (with PE = low)	f_{max} (Figures 4, 5, 6)	5.0 10 15	– – –	2.0 5.0 6.6	1.5 3.0 4.0	MHz
Clock or Inhibit Rise and Fall Time	$t_r,$ t_f (Figures 5, 6)	5.0 10 15	– – –	– – –	15 5 4	μs
Setup Time Pn to Preset Enable	t_{su} (Figure 1)	5.0 10 15	90 50 40	40 15 10	– – –	ns
Hold Time Preset Enable to Pn	t_h (Figure 2)	5.0 10 15	30 30 30	–15 –5 0	– – –	ns
Preset Enable Pulse Width	t_w (Figure 3)	5.0 10 15	250 100 80	125 50 40	– – –	ns
Reset Pulse Width	t_w (Figure 8)	5.0 10 15	350 250 200	175 125 100	– – –	ns
Reset Removal Time	t_{rem} (Figure 8)	5.0 10 15	10 20 30	–110 –30 –20	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

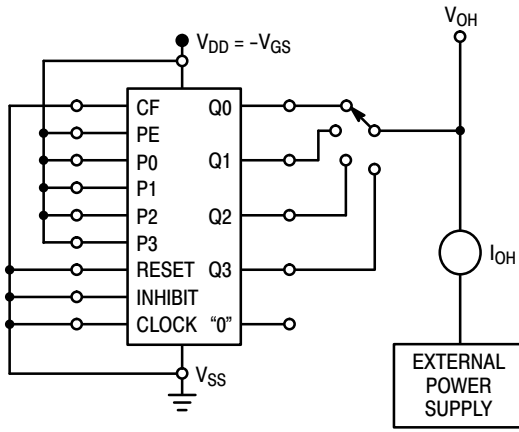


Figure 1. Typical Output Source Characteristics Test Circuit

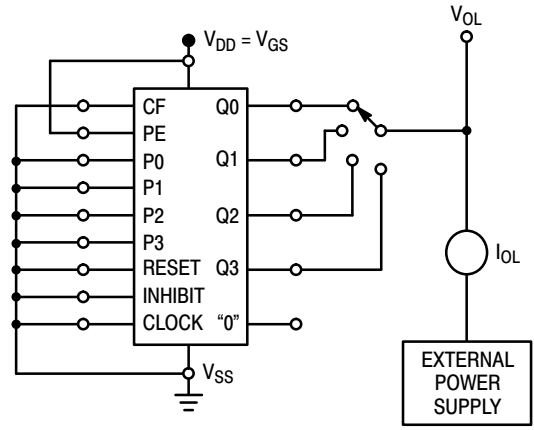


Figure 2. Typical Output Sink Characteristics Test Circuit

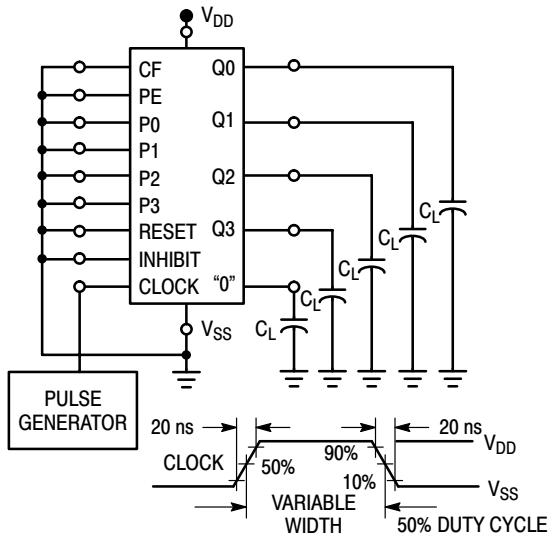
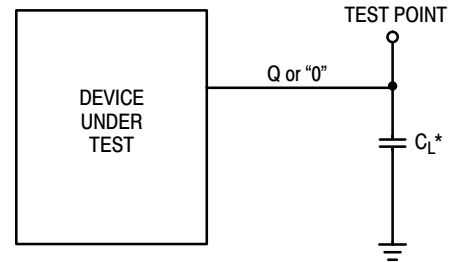


Figure 3. Power Dissipation



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

SWITCHING WAVEFORMS

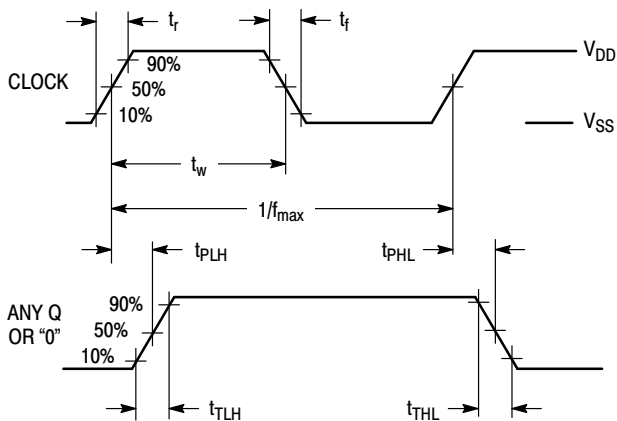


Figure 5.

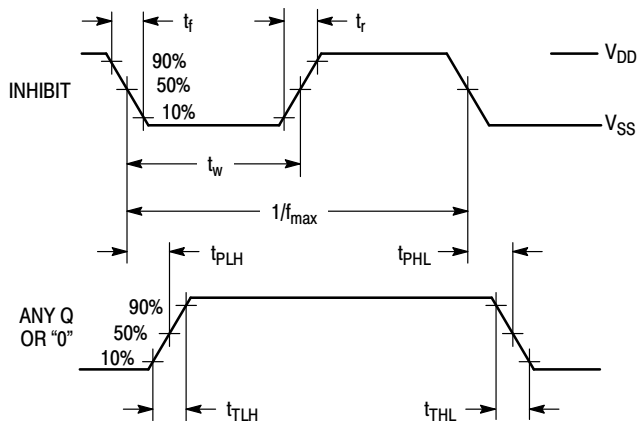


Figure 6.

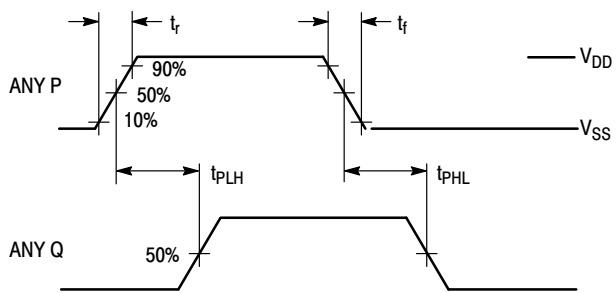


Figure 7.

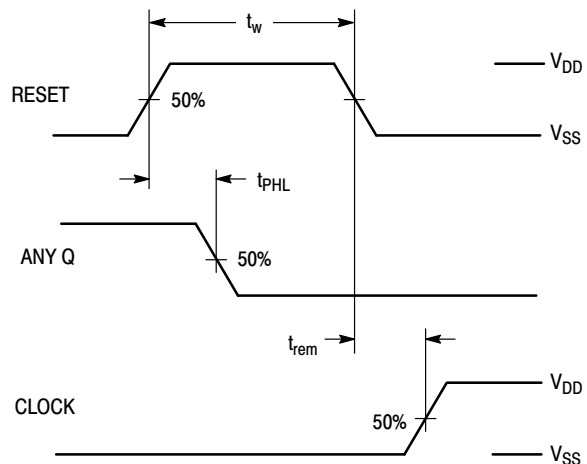


Figure 8.

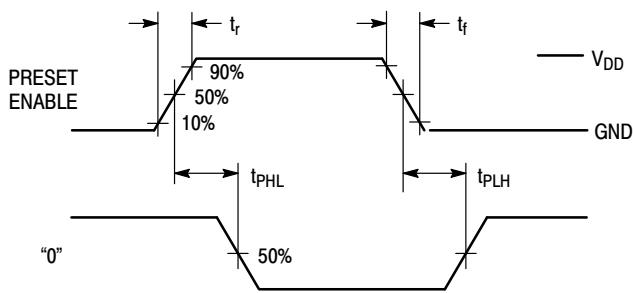


Figure 9.

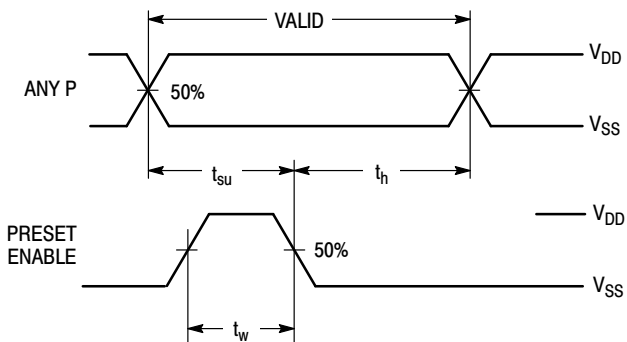
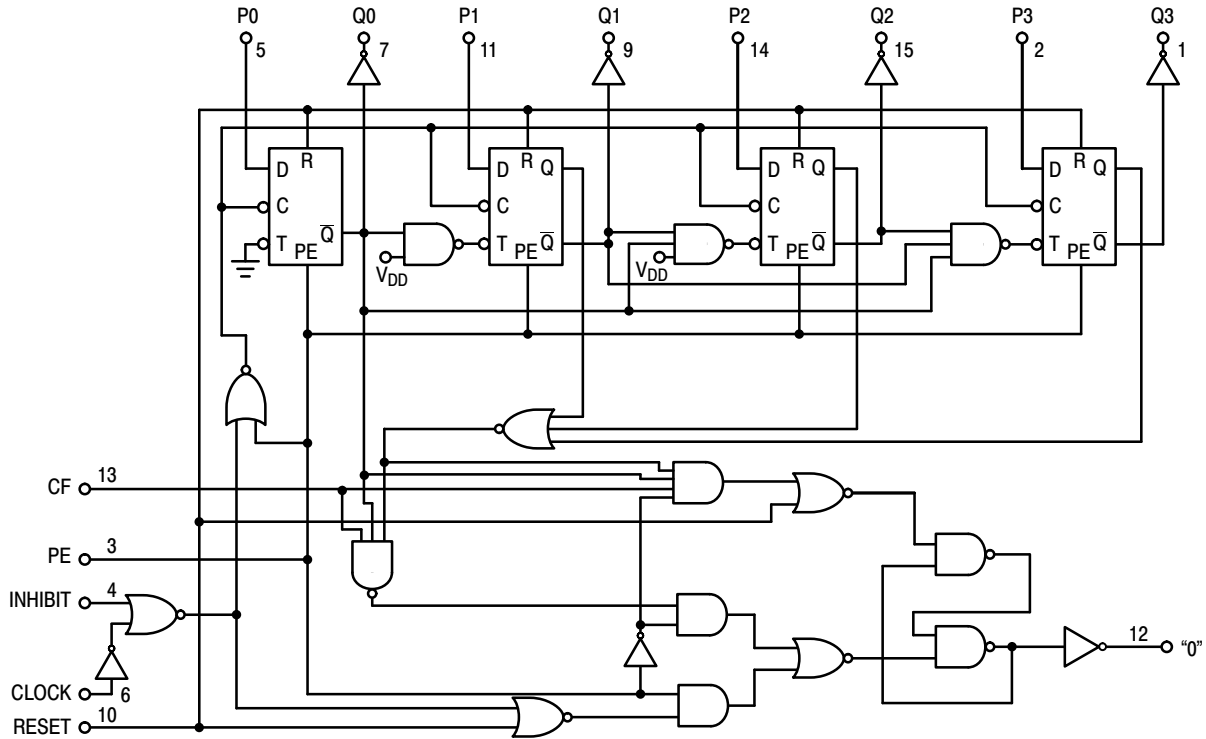


Figure 10.

MC14526B

MC14526B LOGIC DIAGRAM (Binary Down Counter)



APPLICATIONS INFORMATION

Divide-By-N, Single Stage

Figure 11 shows a single stage divide-by-N application.

To initialize counting a number, N is set on the parallel inputs (P0, P1, P2, and P3) and reset is taken high asynchronously. A zero is forced into the master and slave of each bit and, at the same time, the "0" output goes high. Because Preset Enable is tied to the "0" output, preset is enabled. Reset must be released while the Clock is high so the slaves of each bit may receive N before the Clock goes low. When the Clock goes low and Reset is low, the "0" output goes low (if P0 through P3 are unequal to zero).

The counter downcounts with each rising edge of the Clock. When the counter reaches the zero state, an output pulse occurs on "0" which presets N. The propagation delays from the Clock's rising and falling edges to the "0" output's rising and falling edges are about equal, making the "0" output pulse approximately equal to that of the Clock pulse.

The Inhibit pin may be used to stop pulse counting. When this pin is taken high, decrementing is inhibited.

Cascaded, Presettable Divide-By-N

Figure 12 shows a three stage cascade application. Taking Reset high loads N. Only the first stage's Reset pin (least significant counter) must be taken high to cause the preset for all stages, but all pins could be tied together, as shown.

When the first stage's Reset pin goes high, the "0" output is latched in a high state. Reset must be released while Clock is high and time allowed for Preset Enable to load N into all stages before Clock goes low.

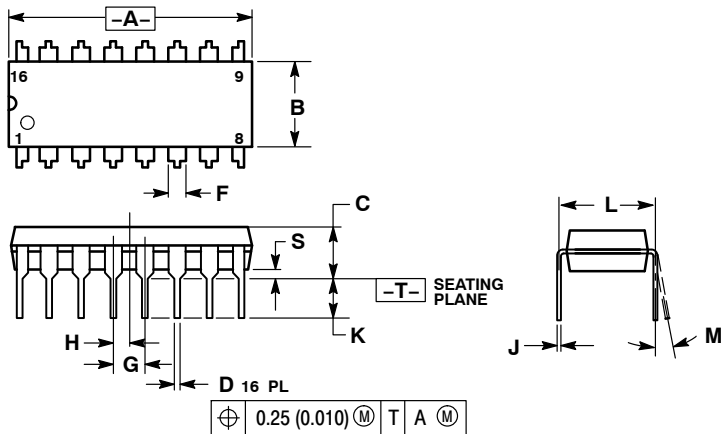
When Preset Enable is high and Clock is low, time must be allowed for the zero digits to propagate a Cascade Feedback to the first non-zero stage. Worst case is from the most significant bit (M.S.B.) to the L.S.B., when the L.S.B. is equal to one (i.e. N = 1).

After N is loaded, each stage counts down to zero with each rising edge of Clock. When any stage reaches zero and the leading stages (more significant bits) are zero, the "0" output goes high and feeds back to the preceding stage. When all stages are zero, the Preset Enable automatically loads N while the Clock is high and the cycle is renewed.

MC14526B

PACKAGE DIMENSIONS

PDIP-16
CASE 648-08
ISSUE T

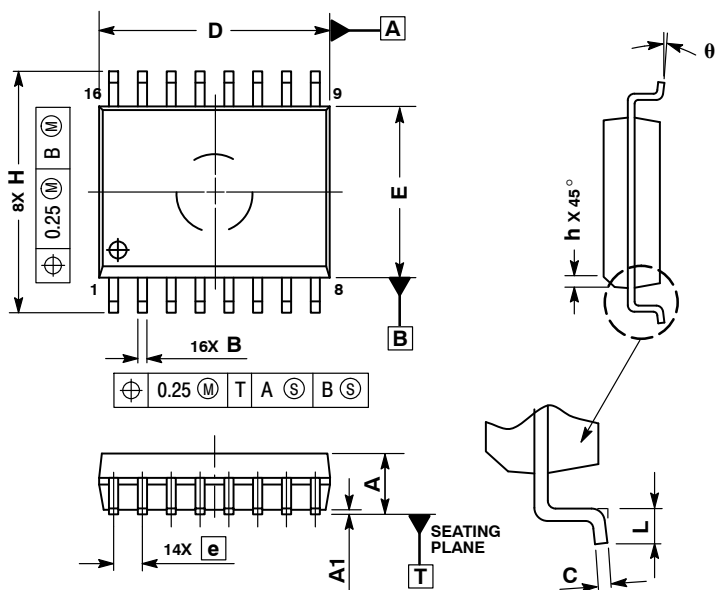


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16WB
CASE 751G-03
ISSUE C



NOTES:

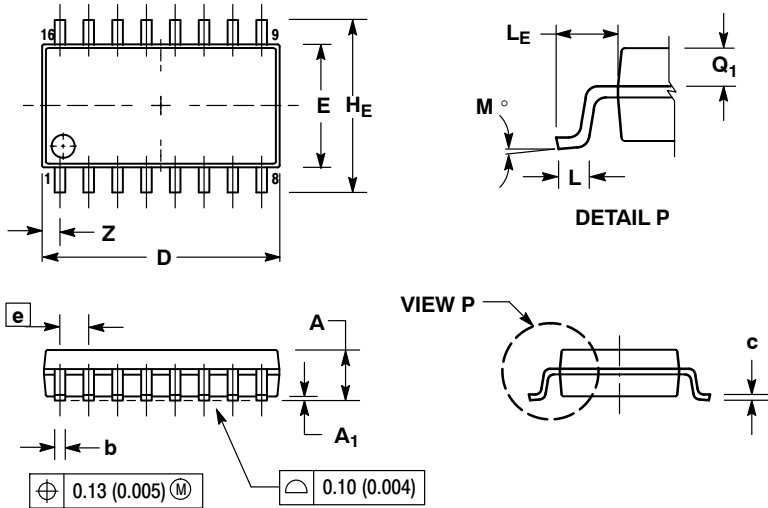
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

MC14526B

PACKAGE DIMENSIONS

SOEIAJ-16
CASE 966-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9