



DrMOS Integrated Power Stage

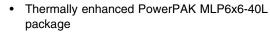
DESCRIPTION

The SiC772 is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency and high power density performance. Packaged in Vishay's proprietary 6 mm x 6 mm MLP package, SiC772 enables voltage regulator design to deliver in excess of 40 A per phase current.

The internal Power MOSFETs utilizes Vishay's state-of-theart TrenchFET Gen IV technology that delivers industry bench-mark performance to significantly reduce switching and conduction losses.

The SiC772 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, and integrated bootstrap Schottky diode; a thermal warning (THWn) alerts the system of excessive junction temperature. This driver is also compatible with wide range of PWM controllers with the support of Tri-state PWM, 5 V PWM Logic, and skip mode (SMOD) for improve light load efficiency.

FEATURES





- Industry benchmark MOSFET with integrated Schottky diode
- Delivers in excess of 40 A continuous current
- 86 % peak efficiency at 19 V to 1 V and 18 A
- High frequency operation up to 1.5 MHz
- Power MOSFETs optimized for 19 V input stage
- 5 V PWM Logic with Tri-state and hold-off
- SMOD logic for light load efficiency boost
- Low PWM propagation delay (< 20 ns)
- Thermal monitor flag
- Faster enable/disenable (10 ns)
- V_{CIN} UVLO
- Compliant with Intel DrMOS 4.0 specification
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

Note:

* This datasheet provides information about parts that are RoHS-compliant and/or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information/tables in this datasheet for details.

APPLICATIONS

- · Synchronous buck converters
- Multi-phase VRDs for CPU, GPU, and memory
- DC/DC POL modules
- Notebook computers

TYPICAL APPLICATION DIAGRAMM

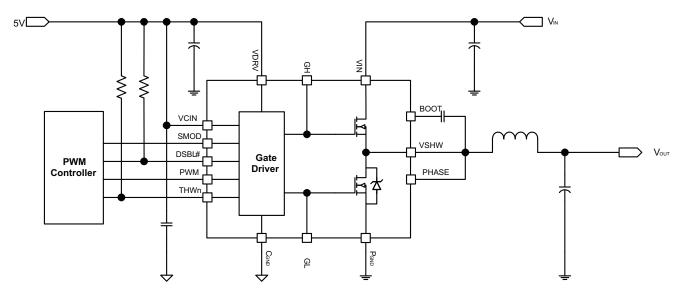


Figure 1: SiC772 Typical Application Diagram

PIN CONFIGURATION

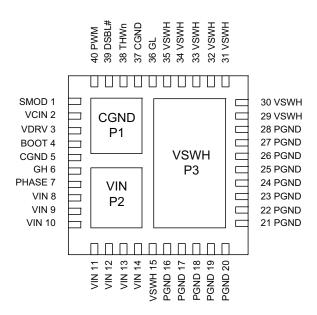


Figure 2 - SiC772 Pin Configuration

PIN DESCRI	PTION	
Pin Number	Symbol	Description
1	SMOD#	LS FET Turn-OFF Logic. Active low
2	V _{CIN}	Supply voltage for internal logic circuitry
3	V_{DRV}	Supply voltage for internal gate driver
4	BOOT	High side driver bootstrap voltage
5, 37, P1	C _{GND}	Analog ground for the driver IC
6	GH	High side gate signal
7	PHASE	Return path of HS Gate Driver
8 to 14, P2	V _{IN}	Power stage input voltage. Drain of high side MOSFET
15, 29 to 35, P3	V _{SWH}	Phase node of the power stage
16 to 28	P_{GND}	Power ground
36	GL	Low side gate signal
38	THWn	Thermal warning open drain output
39	DSBL#	Disable pin. Active low
40	PWM	PWM input logic





ORDERING INFORMATION							
Part Number	Package	Marking Code					
SiC772CD-T1-GE3	PowerPAK MLP66-40L	SiC772CD					
SiC772DB Reference Board							

ABSOLUTE MAXIMUM RATINGS (1)			
Electrical Parameter	Symbol	Limits	Unit
Input Voltage	V _{IN}	- 0.3 to 30	
Control Input Voltage	V _{CIN}	- 0.3 to 7	
Drive Input Voltage	V _{DRV}	- 0.3 to 7	
Switch Node (DC)	V _{SW}	- 0.3 to 30	V
Switch Node (AC) (2)	V _{SW}	- 8 to 35	V
Boot Voltage (DC Voltage)	V _{BS}	- 0.3 to 33	
Boot to Switching Node (DC Voltage)	V _{BS_SW}	- 0.3 to 7	
All Logic Inputs and Outputs (PWM, DSBL, SMOD and THWn)		- 0.3 to V _{CIN} + 0.3	
Max. Operating Junction Temperature	T _J	150	
Ambient Temperature	T _A	- 40 to 125	°C
Storage Temperature		- 65 to 150	

2. The specification values indicated "AC" is V_{SW} to P_{GND} - 8 V (< 20 ns, 10 μ J), min. and 35 V (< 50 ns), max.

RECOMMENDED OPERATING CONDITIONS							
Parameter	Min.	Тур.	Max.	Unit			
Input Voltage (V _{IN})	4.5		24				
Drive Input Voltage (V _{DRV})	4.5	5	5.5				
Control Input Voltage (V _{CIN})	4.5	5	5.5	V			
Switching Node (LX, DC Voltage)			27				
BOOT-SW	4	4.5	5.5				

THERMAL RESISTANCE RATINGS				
Parameter	Min.	Тур.	Max.	Unit
Thermal Resistance from Junction to Case (to P3 PAD (V _{SHW})		2.5		°C/W
Thermal Resistance from Junction to PCB		5		O/ VV

^{1.} Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SiC772CD

Vishay Siliconix



ELECTRICAL SPECIFICATIO	NS							
Parameter	Symbol			$V_{DSBL\#} = V_{SMOD} = 5 \text{ V}, \\ V_{IN} = 19 \text{ V}, V_{DRV} = V_{CIN} = 5 \text{ V}, $ Min.		Тур. ⁽³⁾	Max. ⁽⁵⁾	Unit
Power Supplies								
		$V_{DSBL\#} = 0 V$, no switching		100				
V _{CIN} Control Input Current	I _{VCIN}	$V_{DSBL\#} = 5 \text{ V}$, no switching		300		μΑ		
		$V_{DSBL\#} = 5 \text{ V}, f_s = 300 \text{ kHz}, D = 0.1$		300				
		f _s = 300 kHz, D = 0.1		16	25	mA		
Drive Input Current (Dynamic)	I _{VDRV}	f _s = 1 MHz, D = 0.1		60		ША		
brive input Gurrent (Dynamic)		V _{DSBL#} = 0 V, no switching		30				
		V _{DSBL#} = 5 V, no switching		60		μΑ		
Bootstrap Supply								
Bootstrap Switch Forward Voltage	V _F	V _{CIN} = 5 V, forward bias current 2 mA			0.4	V		
PWM Control Input								
Rising Threshold	PWM _{th_r}		3.4	3.7	4.2			
Falling Threshold	PWM _{th_f}		0.7	0.9	1.2			
Tri-state Voltage	V _{tri}	PWM pin floating		2.3		V		
Tri-state Falling Threshold	$V_{tri_th_f}$		0.9	1.2	1.5			
Tri-state Rising Threshold	V _{tri_th_r}		3	3.4	3.7			
Tri-state Rising Threshold Hysteresis	V _{tri_hys_r}			225		mV		
Tri-state Falling Threshold Hysteresis	V _{tri_hys_f}			325		111 V		
PWM Input Current	V _{PWM} = 5 V 500		500	^				
i www.input Guilent	I _{PWM}	V _{PWM} = 0 V			- 500	μΑ		

^{3.} Typical limits are established by characterization and are not production tested.

^{4.} Guaranteed by design.5. Min. and max. not 100 % production tested.





ELECTRICAL SPECIFICAT	IONS					
Parameter	Symbol	Test Conditions Unless Specified $V_{DSBL\#} = V_{SMOD} = 5 \text{ V},$ $V_{IN} = 19 \text{ V}, V_{VDRV} = V_{VCIN} = 5 \text{ V},$ $T_A = 25 \text{ °C}$	Min.	Тур. ⁽³⁾	Max. ⁽⁵⁾	Unit
DSBL#, SMOD INPUT						
DSBL# Logic Input Voltage	V _{DSBL}	Enable Disenable	2		0.8	
SMOD Logic Input Voltage	V _{SMOD}	High State Low State	2		0.8	V
Protection						
Under Voltage Lockout	V _{UVLO}	Rising, on Threshold Falling, off Threshold	2.7	3.7 3.2	4.3	V
Under Voltage Lockout Hysteresis		<u> </u>		550		mV
THDn Flag Set ⁽⁴⁾				160		
THDn Flag Clear ⁽⁴⁾				135		°C
THDn Flag Hysteresis ⁽⁴⁾				25		
THDn Output Low				0.02		V
Timing Specifications	·					
Tri-State to GH/GL Rising Propagation Delay	t _{pd_r_tri}			20		
Tri-state Hold-off Time	t _{tsho}			150		
GH - Turn off Propagation Delay	t _{pd_off_GH}			20		
GH - Turn on Propagation Delay (Dead Time Rising)	t _{pd_on_GH}	No load, see fig.4		10		ns
GL - Turn off Propagation Delay	t _{pd_off_GL}			10		
GL - Turn on Propagation Delay (Dead Time Falling)	t _{pd_on_GL}			10		

Notes:

- 3. Typical limits are established by characterization and are not production tested.
- 4. Guaranteed by design.
- 5. Min. and max. not 100 % production tested.



DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate Tri-state logic (H, L, and Tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{th_pwm_r}$ the low side is turned OFF and the high side is turned ON. When PWM input is driven below $V_{th\ pwm\ f}$ the high side turns off and the low side turns on. For Tri-state logic, the PWM input operates as above for driving the MOSFETs. However, there is an third state that is entered into as the PWM output of Tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC772 to pull the PWM input into the Tri-state region (see the Tri-state Voltage Threshold Diagram below). If the PWM input stays in this region for the Tri-state hold-off period, t_{TSHO}, both high side and low side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a schottky diode clamp. The PWM and Tri-state regions are separated by hysteresis to prevent false triggering. The SiC772CD incorporates PWM voltage thresholds that are compatible with 5 V logic.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFET. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to C_{GND} and shut down the IC.

Diode Emulation Mode (SMOD) Skip

When SMOD pin is low the diode emulation mode is enabled and GL is turned off. This is a non-synchronous conversion mode that improves light load efficiency reducing switching losses. Conducted losses that occur in synchronous buck regulators when inductor current is negative can also be reduced. Circuitry in the external controller IC detects when inductor current crosses zero and drive SMOD Lo turning the low side MOSFET off. See SMOD Operation diagram for additional details. If SMOD is left unconnected, an internal pull up resistor will pull the pin up to V_{CIN} (Logic High) to disable the SMOD function.

Thermal Shutdown Warning (THDn)

The THDn pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 k Ω to pull this pin up to V_{CIN} . An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THDn flag is set. When the junction temperature drops below 135 °C the device will clear the THDn signal. The SiC772 does not stop operation

when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side Power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The Switch node V_{SWH} is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20.2 k Ω resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the Printed Circuit Board should be such that the inductance separating the $C_{\mbox{\footnotesize GND}}$ and $P_{\mbox{\footnotesize GND}}$ should be a minimum. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin. Shoot-Through Protection and Adaptive Dead Time

Shoot-Through Protection and Adaptive Dead Time

The SiC772 has an internal adaptive logic to avoid shoot through and optimize dead time. The through protection ensures that both high-side and low-side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on until the other's gate voltage is sufficiently low (1 V), that and built in delays ensure the one Power MOS is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.



Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC772 also

incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20.2 $k\Omega$ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

FUNCTIONAL BLOCK DIAGRAM

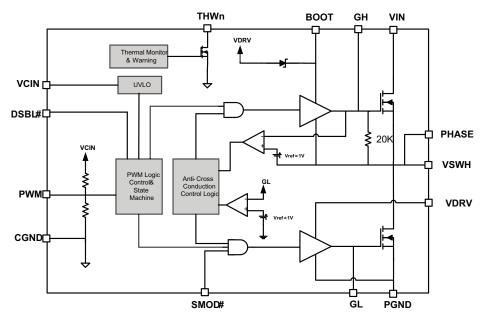


Figure 3: SiC772 Functional Block Diagram

DEVICE TRUTH T	DEVICE TRUTH TABLE								
DSBL#	SMOD	PWM	GH	GL					
Open	Х	Х	L	L					
L	X	X	L	L					
Н	L	L	L	L					
Н	L	Н	Н	L					
Н	Н	Н	Н	L					
Н	Н	L	L	Н					
Н	L	Tri-state	L	L					
Н	Н	Tri-state	L	L					

PWM TIMING DIAGRAM

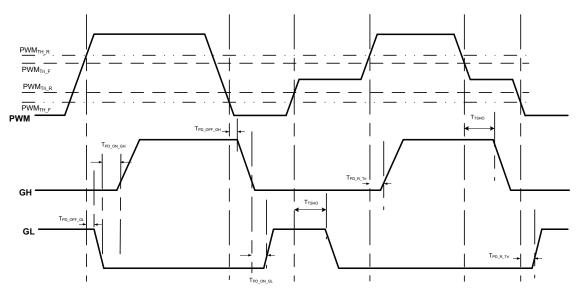


Figure 4: Definition of PWM Logic and Tri-state

SMOD OPERATION DIAGRAM

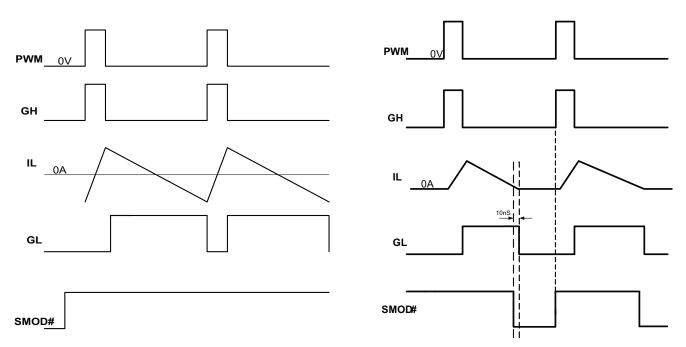
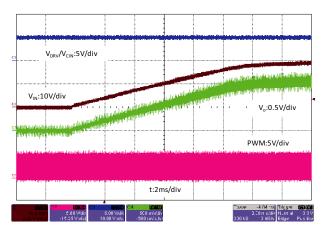


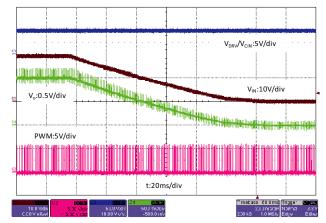
Figure 5: CCM Operation with SMOD# = HIGH

Figure 6: DCM Operation with SMOD# = Active Toggle

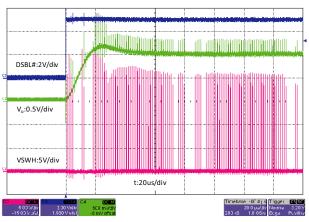
ELECTRICAL CHARACTERISTICS



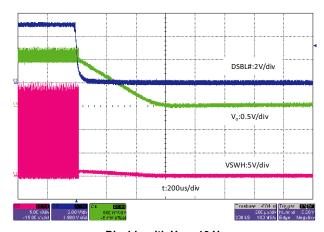
Start-up with V_{IN} Ramping Up $V_{IN} = 19 \text{ V}, V_{OUT} = 1 \text{ V}, f_{SW} = 800 \text{ kHz}, I_{OUT} = 0 \text{ A}$



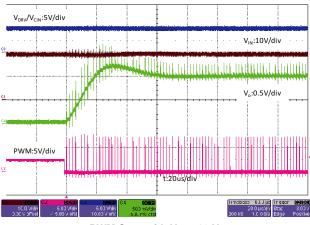
Power Off with V_{IN} Ramping Down $V_{IN} = 19 \text{ V}, V_{OUT} = 1 \text{ V}, f_{SW} = 800 \text{ kHz}, I_{OUT} = 1.2 \text{ A}$



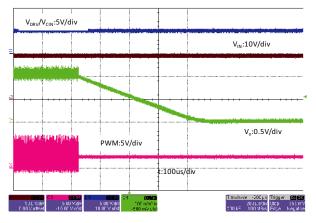
Enable with $V_{IN} = 19 V$, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A



Disable with $V_{IN} = 19 V$, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A

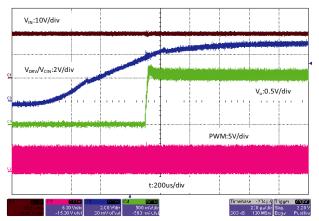


PWM Start with $V_{IN} = 19 V$, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A

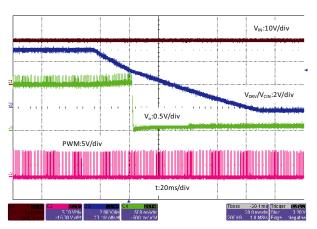


PWM Turn-off with $V_{IN} = 19 V$, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 1.2 A

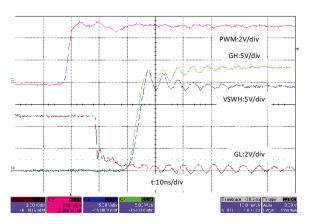
ELECTRICAL CHARACTERISTICS



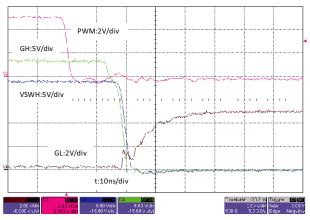
Start-up with V_{DRV}/V_{CIN} Ramping Up $V_{IN} = 19 \text{ V}, V_{OUT} = 1 \text{ V}, f_{SW} = 800 \text{ kHz}, I_{OUT} = 0 \text{ A}$



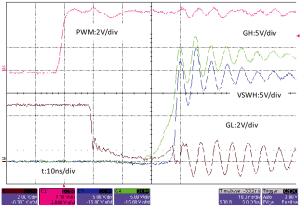
Power off with V_{DRV}/V_{CIN} Ramping Down $V_{IN} = 19 \text{ V}, V_{OUT} = 1 \text{ V}, f_{SW} = 800 \text{ kHz}, I_{OUT} = 1.2 \text{ A}$



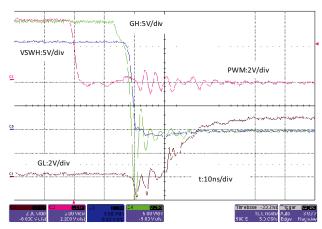
Switching Waveform at PWM Rising Edge $V_{IN} = 19 \text{ V}, V_{OUT} = 1 \text{ V}, f_{SW} = 800 \text{ kHz}, I_{OUT} = 0 \text{ A}$



Switching Waveform at PWM Falling Edge $V_{IN} = 19 \text{ V}, V_{OUT} = 1 \text{ V}, f_{SW} = 800 \text{ kHz}, I_{OUT} = 0 \text{ A}$



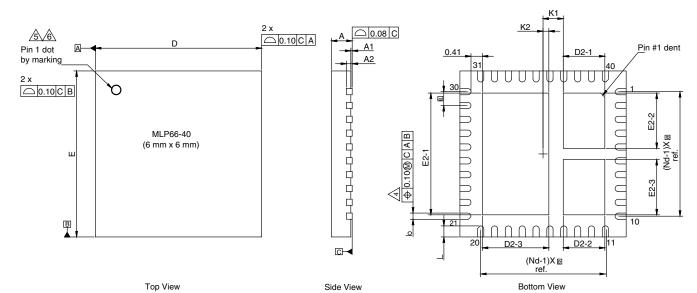
Switching Waveform at PWM Rising Edge V_{IN} = 19 V, V_{OUT} = 1 V, f_{SW} = 800 kHz, I_{OUT} = 30 A



Switching Waveform at PWM Falling Edge $V_{IN} = 19 \text{ V}, V_{OUT} = 1 \text{ V}, f_{SW} = 800 \text{ kHz}, I_{OUT} = 30 \text{ A}$



PACKAGE DIMENSIONS



DIM	MILLIMETERS			INCHES			
DIM	Min.	Nom.	Max.	Min.	Nom.	Max.	
A ⁽⁸⁾	0.70	0.75	0.80	0.027	0.029	0.031	
A1	0.00	-	0.05	0.000	-	0.002	
A2		0.20 ref.			0.008 ref.		
b ⁽⁴⁾	0.20	0.25	0.30	0.078	0.098	0.011	
D		6.00 BSC			0.236 BSC		
е		0.50 BSC			0.019 BSC		
E		6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017	
N ⁽³⁾		40			40		
Nd ⁽³⁾		10			10		
Ne ⁽³⁾		10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061	
D2-2	1.45	1.50	1.55	0.057	0.059	0.061	
D2-3	2.35	2.40	2.45	0.095	0.094	0.096	
E2-1	4.35	4.40	4.45	0.171	0.173	0.175	
E2-2	1.95	2.00	2.05	0.076	0.078	0.080	
E2-3	1.95	2.00	2.05	0.076	0.078	0.080	
K1		0.73 BSC			0.028 BSC		
K2		0.21 BSC					

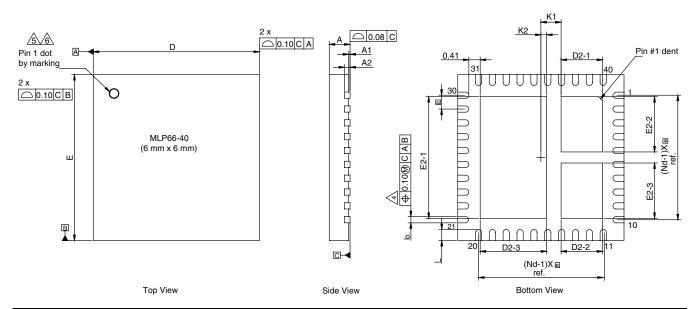
Notes:

- Use millimeters as the primary measurement. 1.
- Dimensioning and tolerances conform to ASME Y14.5M-1994.
- N is the number of terminals.
 - Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction .
- 4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
- The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body .
- Exact shape and size of this feature is optional. 6.
- 7. Package warpage max. 0.08 mm.
- 8. Applied only for terminals.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63822



PowerPAK® MLP66-40 CASE OUTLINE



DIM.	MILLIMETERS			INCHES			
DIWI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A (8)	0.70	0.75	0.80	0.027	0.029	0.031	
A1	0.00	-	0.05	0.000	-	0.002	
A2		0.20 ref.			0.008 ref.		
b ⁽⁴⁾	0.20	0.25	0.30	0.078	0.098	0.011	
D		6.00 BSC			0.236 BSC		
е		0.50 BSC			0.019 BSC		
Е		6.00 BSC 0.236 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017	
N (3)		40			40		
Nd ⁽³⁾		10			10		
Ne ⁽³⁾	10				10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061	
D2-2	1.45	1.50	1.55	0.057	0.059	0.061	
D2-3	2.35	2.40	2.45	0.095	0.094	0.096	
E2-1	4.35	4.40	4.45	0.171	0.173	0.175	
E2-2	1.95	2.00	2.05	0.076	0.078	0.080	
E2-3	1.95	2.00	2.05	0.076	0.078	0.080	
K1	0.73 BSC			0.028 BSC			
K2		0.21 BSC			0.008 BSC		

ECN: T09-0195-Rev. A, 04-May-09

DWG: 5986

Notes

- 1. Use millimeters as the primary measurement
- 2. Dimensioning and tolerances conform to ASME Y14.5M. 1994
- 3. N is the number of terminals. Nd is the number of terminals in Y-direction and Ne is the number of terminals in Y-direction
- Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
- The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- £ Exact shape and size of this feature is optional
- 7. Package warpage max. 0.08 mm
- Applied only for terminals

Document Number: 64846 www.vishay.com 04-May-09 1



Legal Disclaimer Notice

Vishay

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000

ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9