

RoHS Compliant

512MB DDR SDRAM SO-DIMM **Industrial**

Product Specifications

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Version 1.1



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General Description

Apacer **75.963AT.G020C** is 64M x 64 Double Data Rate SDRAM high density memory modules based on first generation of 512Mb DDR SDRAM respectively.

It consists of 8 pieces 64M x8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II (400mil) packages mounted on a 200pin glass-epoxy substrate. Decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. This product is Dual In-line Memory Modules and intended for mounting into 200 pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Ordering Information

| Part Number | Bandwidth | Speed Grade | Max Frequency | CAS Latency |
|----------------|------------|-------------|---------------|-------------|
| 75.963AT.G020C | 3.2 GB/sec | 400 Mbps | 200 MHz | CL3 |

| Density | Organization | Component | Rank |
|---------|--------------|-----------|------|
| 512MB | 64M x 64 | 64M x8*8 | 1 |

Key Parameters

| MT/s | DDR-266 | DDR-266 | DDR-333 | DDR-400 | Unit |
|-------------|---------|---------|---------|---------|------|
| Grade | -CL2 | -CL2.5 | -CL2.5 | -CL3 | |
| tCK (min) | 7.5 | 7.5 | 6 | 5 | ns |
| CAS latency | 2 | 2.5 | 2.5 | 3 | tCK |
| tRC | 9 | 9 | 10 | 11 | tCK |
| tRAS | 6 | 6 | 7 | 8 | tCK |
| CL-tRCD-tRP | 2-3-3 | 2.5-3-3 | 2.5-3-3 | 3-3-3 | tCK |

Specifications:

- ◆ Power supply V_{DD} : 2.6V +/-0.1V
- ◆ MRS cycle with address key programs
- ◆ CAS Latency (Access from column address): 2.5, 3
- ◆ Burst length : 2, 4, 8
- ◆ Data scramble ;Sequential & Interleave
- ◆ Serial presence detect with EEPROM
- ◆ SSTL-2 interface
- ◆ Differential clock input
- ◆ Compliance With RoHS
- ◆ Compliance With CE
- ◆ Auto Refresh and self Refresh Modes 64ms, 8192-cycle refresh
- ◆ Operating Temperature Rang : Industrial $-40^{\circ}\text{C} \leq TA \leq 85^{\circ}\text{C}$

Pin Assignments

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|-------------------------|---------|-------------------------|---------|-------------------------|---------|----------|
| 1 | VREF | 51 | Vss | 101 | A9 | 151 | DQ42 |
| 3 | Vss | 53 | DQ19 | 103 | Vss | 153 | DQ43 |
| 5 | DQ0 | 55 | DQ24 | 105 | A7 | 155 | VDD |
| 7 | DQ1 | 57 | VDD | 107 | A5 | 157 | VDD |
| 9 | VDD | 59 | DQ25 | 109 | A3 | 159 | Vss |
| 11 | DQS0 | 61 | DQS3 | 111 | A1 | 161 | Vss |
| 13 | DQ2 | 63 | Vss | 113 | VDD | 163 | DQ48 |
| 15 | Vss | 65 | DQ26 | 115 | A10/AP | 165 | DQ49 |
| 17 | DQ3 | 67 | DQ27 | 117 | BA0 | 167 | VDD |
| 19 | DQ8 | 69 | VDD | 119 | $\overline{\text{WE}}$ | 169 | DQS6 |
| 21 | VDD | 71 | CB0 | 121 | $\overline{\text{CS0}}$ | 171 | DQ50 |
| 23 | DQ9 | 73 | CB1 | 123 | NC | 173 | Vss |
| 25 | DQS1 | 75 | Vss | 125 | Vss | 175 | DQ51 |
| 27 | Vss | 77 | DQS8 | 127 | DQ32 | 177 | DQ56 |
| 29 | DQ10 | 79 | CB2 | 129 | DQ33 | 179 | VDD |
| 31 | DQ11 | 81 | VDD | 131 | VDD | 181 | DQ57 |
| 33 | VDD | 83 | CB3 | 133 | DQS4 | 183 | DQS7 |
| 35 | CK0 | 85 | NC | 135 | DQ34 | 185 | Vss |
| 37 | $\overline{\text{CK0}}$ | 87 | Vss | 137 | Vss | 187 | DQ58 |
| 39 | Vss | 89 | CK2 | 139 | DQ35 | 189 | DQ59 |
| 41 | DQ16 | 91 | $\overline{\text{CK2}}$ | 141 | DQ40 | 191 | VDD |
| 43 | DQ17 | 93 | VDD | 143 | VDD | 193 | SDA |
| 45 | VDD | 95 | CKE1 | 145 | DQ41 | 195 | SCL |
| 47 | DQS2 | 97 | NC | 147 | DQS5 | 197 | VDDSPD |
| 49 | DQ18 | 99 | A12 | 149 | Vss | 199 | VDDID |

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|-------------------------|---------|-------------------------|
| 2 | VREF | 52 | Vss | 102 | A8 | 152 | DQ46 |
| 4 | Vss | 54 | DQ23 | 104 | Vss | 154 | DQ47 |
| 6 | DQ4 | 56 | DQ28 | 106 | A6 | 156 | VDD |
| 8 | DQ5 | 58 | VDD | 108 | A4 | 158 | $\overline{\text{CK1}}$ |
| 10 | VDD | 60 | DQ29 | 110 | A2 | 160 | CK1 |
| 12 | DM0 | 62 | DM3 | 112 | A0 | 162 | Vss |
| 14 | DQ6 | 64 | Vss | 114 | VDD | 164 | DQ52 |
| 16 | Vss | 66 | DQ30 | 116 | BA1 | 166 | DQ53 |
| 18 | DQ7 | 68 | DQ31 | 118 | $\overline{\text{RAS}}$ | 168 | VDD |
| 20 | DQ12 | 70 | VDD | 120 | $\overline{\text{CAS}}$ | 170 | DM6 |
| 22 | VDD | 72 | CB4 | 122 | $\overline{\text{CS1}}$ | 172 | DQ54 |
| 24 | DQ13 | 74 | CB5 | 124 | NC | 174 | Vss |
| 26 | DM1 | 76 | Vss | 126 | Vss | 176 | DQ55 |
| 28 | Vss | 78 | DM8 | 128 | DQ36 | 178 | DQ60 |
| 30 | DQ14 | 80 | CB6 | 130 | DQ37 | 180 | VDD |
| 32 | DQ15 | 82 | VDD | 132 | VDD | 182 | DQ61 |
| 34 | VDD | 84 | CB7 | 134 | DM4 | 184 | DM7 |
| 36 | VDD | 86 | NC | 136 | DQ38 | 186 | Vss |
| 38 | Vss | 88 | Vss | 138 | Vss | 188 | DQ62 |
| 40 | Vss | 90 | Vss | 140 | DQ39 | 190 | DQ63 |
| 42 | DQ20 | 92 | VDD | 142 | DQ44 | 192 | VDD |
| 44 | DQ21 | 94 | VDD | 144 | VDD | 194 | SA0 |
| 46 | VDD | 96 | CKE0 | 146 | DQ45 | 196 | SA1 |
| 48 | DM2 | 98 | NC | 148 | DM5 | 198 | SA2 |
| 50 | DQ22 | 100 | A11 | 150 | Vss | 200 | NC |

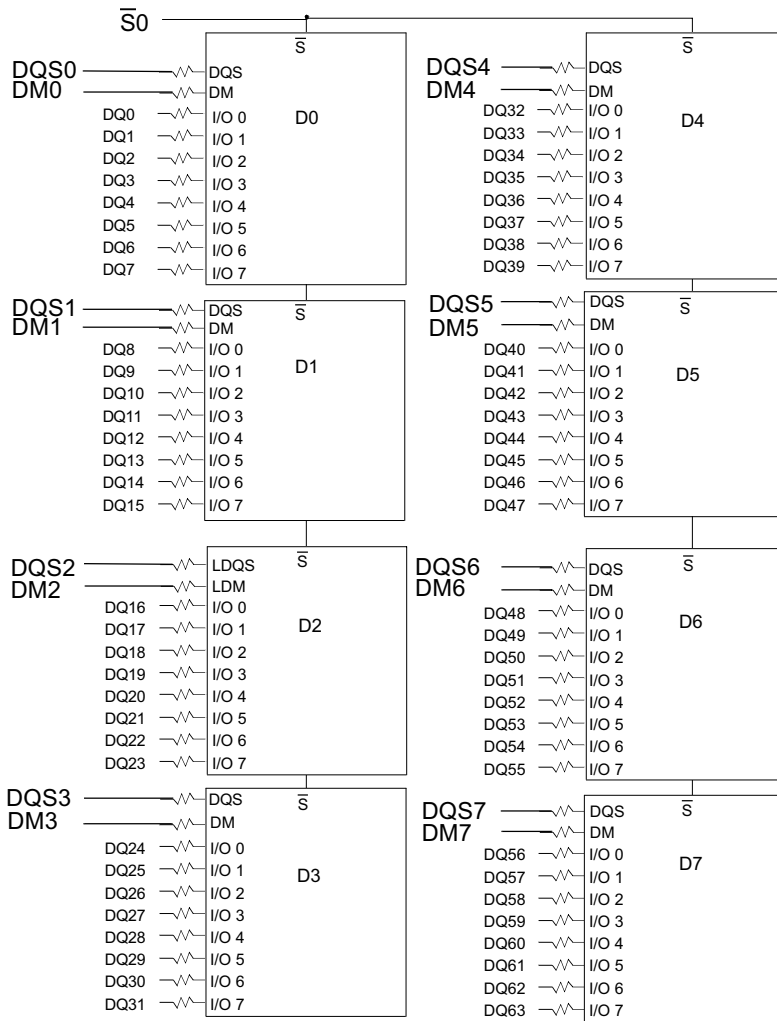
Notes:

1. Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are not used on x64 module, & used on x72 module.

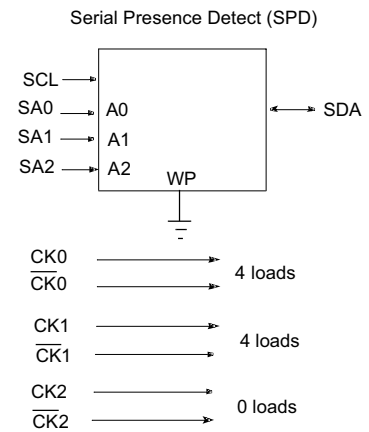
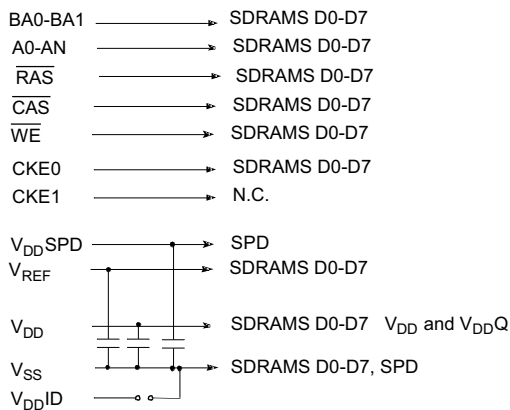
Pin Descriptions

| Pin Name | Description |
|-------------------------|--|
| Ax | SDRAM address bus |
| BAx | SDRAM bank select |
| $\overline{\text{RAS}}$ | SDRAM row address strobe |
| $\overline{\text{CAS}}$ | SDRAM column address strobe |
| $\overline{\text{WE}}$ | SDRAM write enable |
| $\overline{\text{CSx}}$ | DIMM Rank Select Lines |
| CKEx | SDRAM clock enable lines |
| DQx | DIMM memory data bus |
| DQSx | SDRAM data strobes(positive line of differential pair) |
| DMx | SDRAM data masks high data strobes(x8-based X72 DIMMs) |
| CKx | SDRAM clocks(positive line of differential pair) |
| $\overline{\text{CKx}}$ | SDRAM clocks(negative line of differential pair) |
| SCL | I2C serial bus clock for EEPROM |
| SDA | I2C serial bus data line for EEPROM |
| SAX | I2C slave address select for EEPROM |
| VDD | SDRAM core power supply |
| VDDQ | SDRAM I/O Driver power supply |
| VREF | SDRAM I/O reference supply |
| VSS | Power supply return(ground) |
| VDDSPD | Serial EEPROM positive power supply |
| VDDID | VDD identification flag |
| NC | Spare pins(no connect) |

Functional Block Diagram



#Unless otherwise noted, resistor values are $22 \Omega \pm 5\%$



Note: DQ wiring may differ from that described in this drawing; however DQ/DM/DQS relationships are maintained as shown.
 V_{DD}ID strap connections:
 (for memory device V_{DD}, V_{DD}Q)
 Strap out (open): V_{DD} = V_{DD}Q
 Strap in (closed): V_{DD} ≠ V_{DD}Q

Absolute Maximum Ratings

| Parameter | Symbol | Description | Units |
|---|------------------------------------|-----------------|-------|
| Supply Voltage Relative to VSS | V _{DD} | - 1.0 V ~ 3.6 V | V |
| Supply Voltage Relative to VSS | V _{DDQ} | - 1.0 V ~ 3.6 V | V |
| VREF and Inputs Voltage Relative to VSS | V _{IN} , V _{OUT} | - 0.5 V ~ 3.6 V | V |
| Storage Temperature | TSTG | -55 to +100 | °C |

Notes:

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. .

DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Units | Notes |
|--------|--|-----------|-------|-------|
| TA | Operating Temperature Rang: Industrial | -40 to 85 | °C | |

Operating Conditions

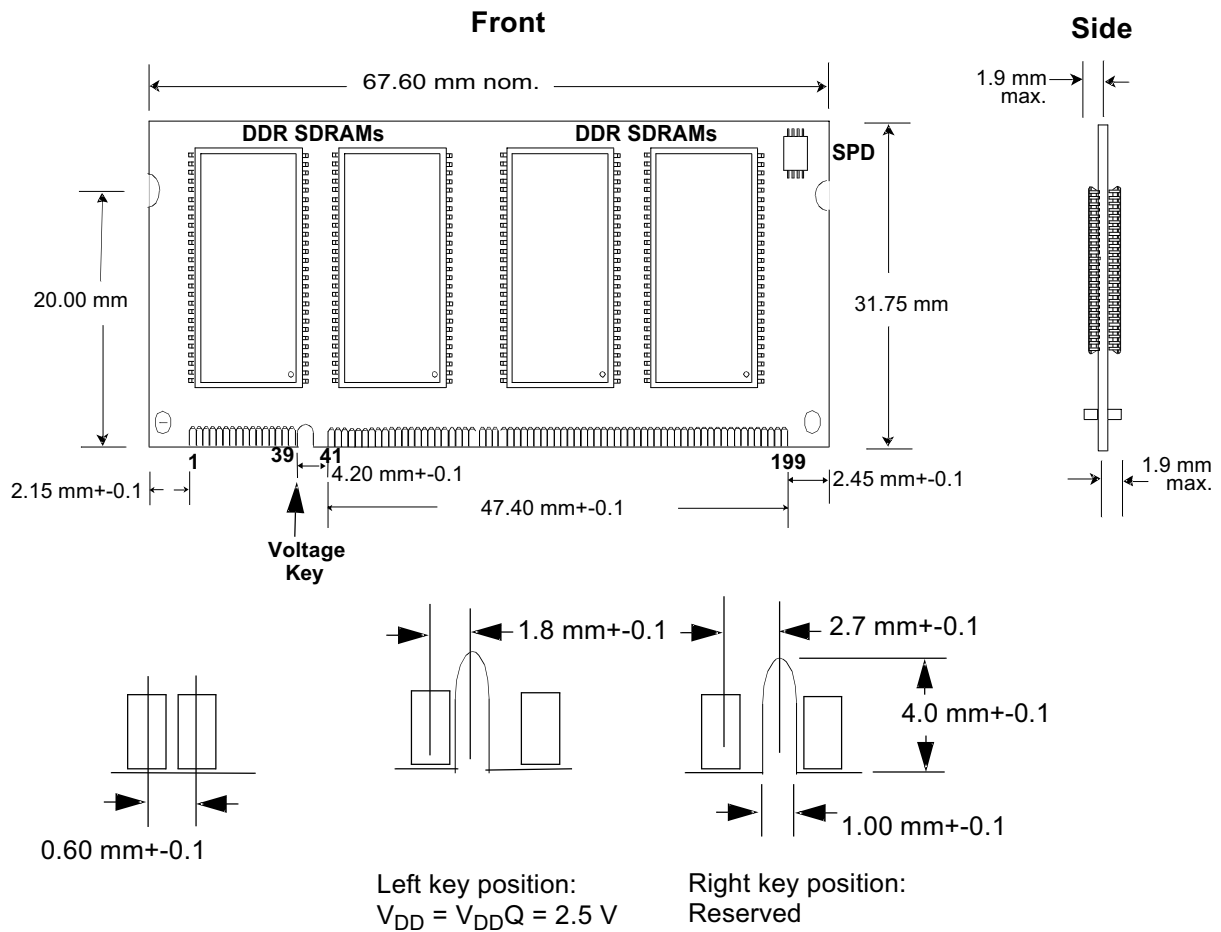
Recommended DC Operating Conditions - DDR (2.6V ± 0.1V) operation

| Symbol | Parameter | Rating | | | Units |
|--------|---------------------------|--------|------|------|-------|
| | | Min. | Typ. | Max. | |
| VDD | Supply Voltage | 2.5 | 2.6 | 2.7 | V |
| VDDQ | Supply Voltage for Output | 2.5 | 2.6 | 2.7 | V |

Notes:

1. VREF is expected to be equal to 0.5 x VDDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CK and the input level on /CK.

Mechanical Drawing



TOLERANCES ON ALL DIMENSIONS \pm 0.13 UNLESS OTHERWISE SPECIFIED.

Revision History

| Revision | Date | Description | Remark |
|-----------------|-------------|------------------------------|---------------|
| 0.9 | 08/28/2012 | Official release | |
| 1.0 | 08/29/2012 | release | |
| 1.1 | 07/23/2013 | Changed headquarters address | |

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