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# ON Semiconductor®

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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (\_), the underscore (\_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (\_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at <a href="www.onsemi.com">www.onsemi.com</a>. Please email any questions regarding the system integration to Fairchild <a href="guestions@onsemi.com">guestions@onsemi.com</a>.

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March 2012

# FDB3632 F085

# N-Channel PowerTrench® MOSFET 100V, 80A, $9m\Omega$

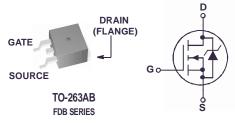
### **Features**

- $r_{DS(ON)} = 7.5 m\Omega$  (Typ.),  $V_{GS} = 10V$ ,  $I_{D} = 80A$
- Q<sub>g</sub>(tot) = 84nC (Typ.), V<sub>GS</sub> = 10V
- Low Miller Charge
- Low Q<sub>RR</sub> Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- · RoHS Compliant



## **Applications**

- DC/DC converters and Off-Line UPS
- · Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Direct Injection / Diesel Injection Systems
- 42V Automotive Load Control
- Electronic Valve Train Systems



# MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
	Drain Current		
I- 1	Continuous ( $T_C < 111^{\circ}C$ , $V_{GS} = 10V$ )	80	А
	Continuous ( $T_{amb} = 25^{\circ}C$ , $V_{GS} = 10V$ , $R_{\theta JA} = 43^{\circ}C/W$ )	12	А
	Pulsed	Figure 4	А
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 1)	338	mJ
	Power dissipation	310	W
$P_{D}$	Derate above 25°C	2.07	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature	-55 to +175	°C

## **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220, TO-263, TO-262	0.48	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220, TO-262 (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in <sup>2</sup> copper pad area	43	°C/W

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Informa	tion
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Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB3632	FDB3632_F085	F085 TO-263AB 330mm		24mm	800 units

# Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted Symbol Parameter Test Condition

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	octeristics					
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100	-	-	V
	Zana Cata Valtana Brain Correct	V <sub>DS</sub> = 80V	-	-	1	
I <sub>DSS</sub> Zero Gate Voltage Drain Current	$V_{GS} = 0V$ $T_{C} = 15$	0°C -	-	250	μΑ	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20V$	-	-	±100	nA

### On Characteristics

V <sub>GS(TH)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2	-	4	V
r <sub>DS(ON)</sub> Drain to Source On Resistance	I <sub>D</sub> =80A, V <sub>GS</sub> =10V	-	0.0075	0.009	0	
	$I_D = 80A, V_{GS} = 10V, T_C = 175^{\circ}C$	-	0.018	0.022	Ω	

## **Dynamic Characteristics**

C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz		-	6000	-	pF
C <sub>OSS</sub>	Output Capacitance			-	820	-	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			-	200	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V <sub>GS</sub> = 0V to 10V		-	84	110	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 2V$	/ <sub>DD</sub> = 50V	-	11	14	nC
	Gate to Source Gate Charge	I	D = 80A	-	30	-	nC
Q <sub>gs</sub> Q <sub>gs2</sub>	Gate Charge Threshold to Plateau	I <sub>g</sub>	g = 1.0mA	-	20	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	]		-	20	-	nC

# **Resistive Switching Characteristics** $(V_{GS} = 10V)$

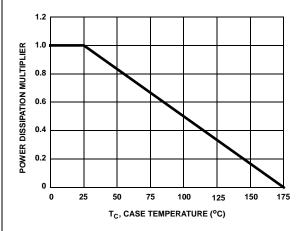
t <sub>ON</sub>	Turn-On Time		-	-	102	ns
t <sub>d(ON)</sub>	Turn-On Delay Time		-	30	-	ns
t <sub>r</sub>		$V_{DD} = 50V, I_{D} = 80A$	-	39	-	ns
t <sub>d(OFF)</sub>	Turn-Off Delay Time	$V_{GS} = 10V, R_{GS} = 3.6\Omega$	-	96	-	ns
t <sub>f</sub>	Fall Time		-	46	-	ns
t <sub>OFF</sub>	Turn-Off Time		-	-	213	ns

## **Drain-Source Diode Characteristics**

V <sub>SD</sub> Source to Drain Diode Voltage	Source to Drain Diade Voltage	I <sub>SD</sub> = 80A	-	-	1.25	V
	I <sub>SD</sub> = 40A	-	-	1.0	V	
t <sub>rr</sub>	Reverse Recovery Time	$I_{SD} = 75A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	64	ns
Q <sub>RR</sub>	Reverse Recovered Charge	$I_{SD} = 75A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	120	nC

Notes: 1: Starting  $T_J$  = 25°C, L = 0.12mH,  $I_{AS}$  = 75A. 2: Pulse Width = 100s





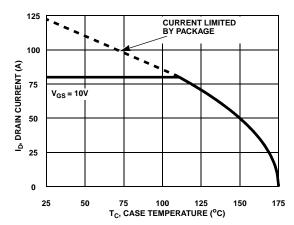


Figure 1. Normalized Power Dissipation vs Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

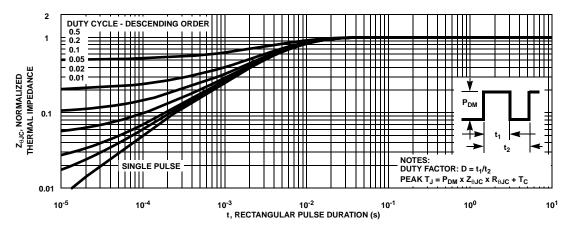


Figure 3. Normalized Maximum Transient Thermal Impedance

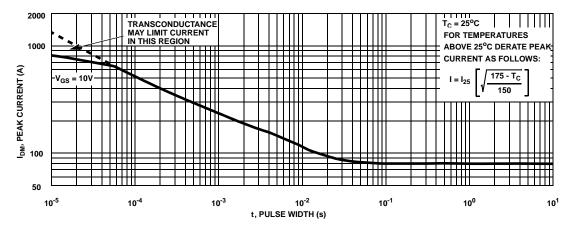
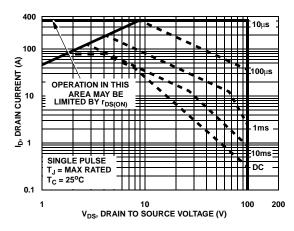


Figure 4. Peak Current Capability





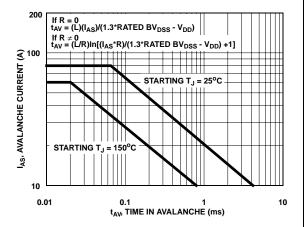
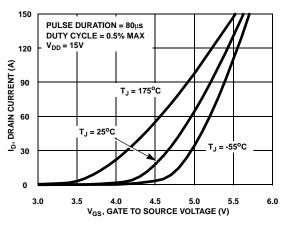


Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability



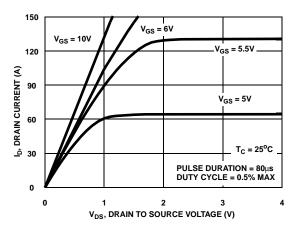
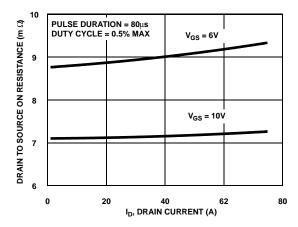


Figure 7. Transfer Characteristics

Figure 8. Saturation Characteristics



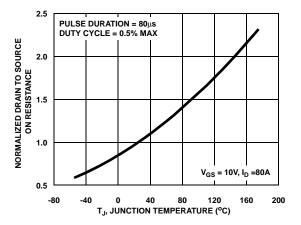


Figure 9. Drain to Source On Resistance vs Drain Current

Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

# **Typical Characteristics** T<sub>A</sub> = 25°C unless otherwise noted

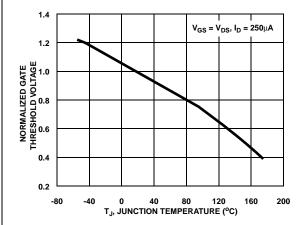


Figure 11. Normalized Gate Threshold Voltage vs
Junction Temperature

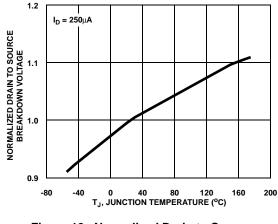


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

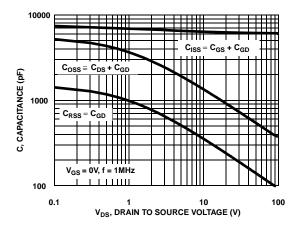


Figure 13. Capacitance vs Drain to Source Voltage

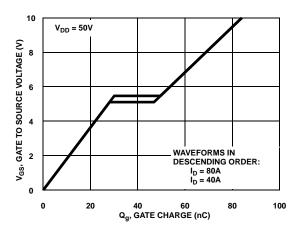
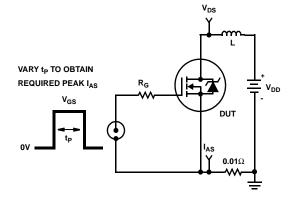


Figure 14. Gate Charge Waveforms for Constant Gate Currents

# **Test Circuits and Waveforms**



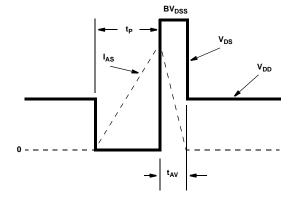


Figure 15. Unclamped Energy Test Circuit

Figure 16. Unclamped Energy Waveforms

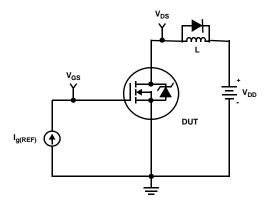


Figure 17. Gate Charge Test Circuit

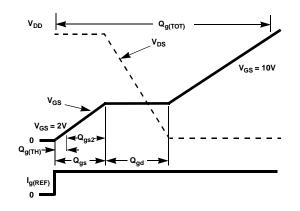


Figure 18. Gate Charge Waveforms

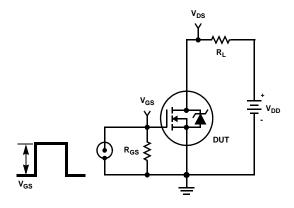


Figure 19. Switching Time Test Circuit

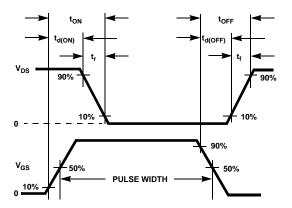


Figure 20. Switching Time Waveforms

# Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  (°C), and thermal resistance  $R_{\theta JA}$  (°C/W) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \tag{EQ. 1}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $\mathsf{P}_{\mathsf{DM}}$  is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- 2. The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)}$$
 (EQ. 2)

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)}$$
 (EQ. 3)

Area in Centimeters Squared

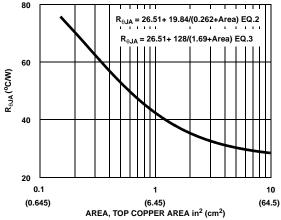
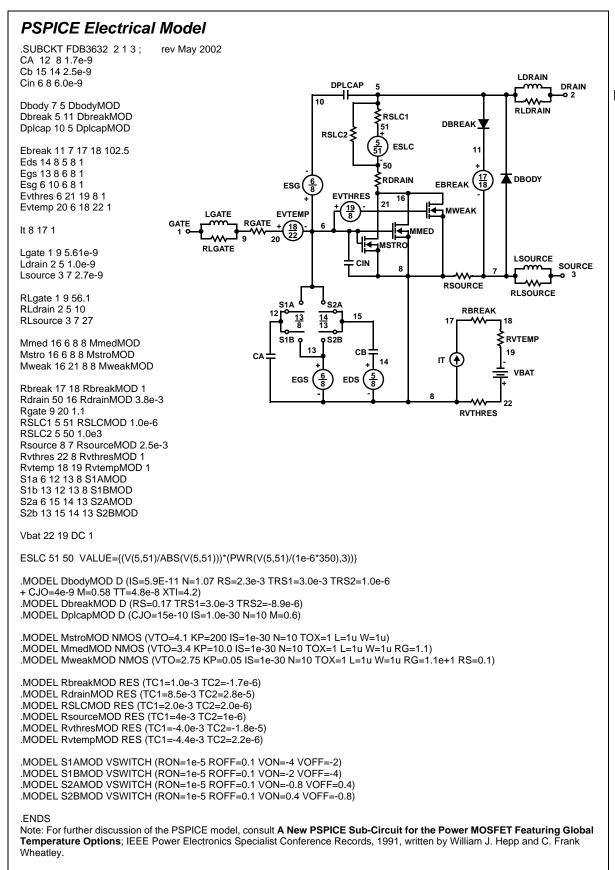
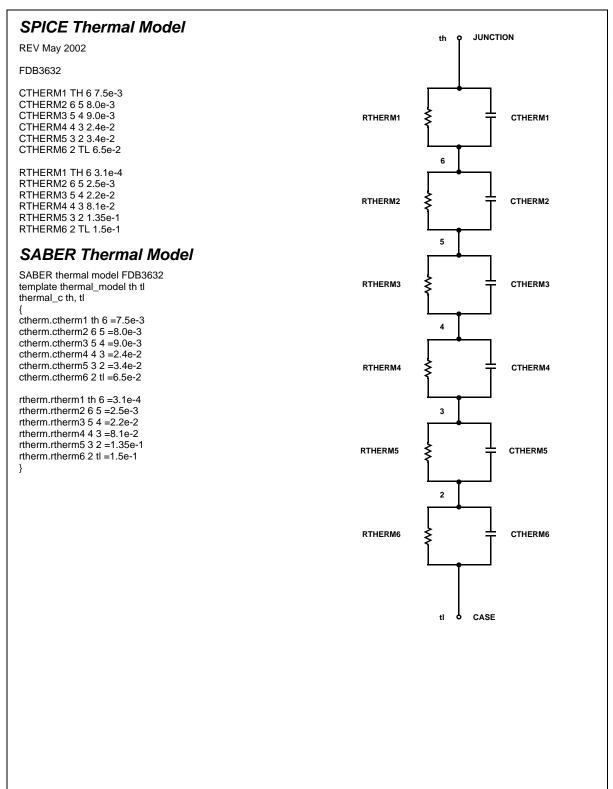


Figure 21. Thermal Resistance vs Mounting
Pad Area



#### SABER Electrical Model REV May 2002 template FDB3632 n2,n1,n3 electrical n2,n1,n3 var i iscl dp..model dbodymod = (isl=5.9e-11,nl=1.07,rs=2.3e-3,trs1=3.0e-3,trs2=1.0e-6,cjo=4e-9,m=0.58,tt=4.8e-8,xti=4.2) dp..model dbreakmod = (rs=0.17.trs1=3.0e-3.trs2=-8.9e-6) dp..model dplcapmod = (cjo=15e-10,isl=10.0e-30,nl=10,m=0.6) m..model mstrongmod = (type=\_n,vto=4.1,kp=200,is=1e-30, tox=1) m..model mmedmod = $(type=_n, vto=3.4, kp=10.0, is=1e-30, tox=1)$ m..model mweakmod = $(type=_n, vto=2.75, kp=0.05, is=1e-30, tox=1, rs=0.1)$ sw\_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-2) I DRAIN sw\_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2,voff=-4) **DPLCAP** DRAIN sw\_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.8,voff=0.4) 10 sw\_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.4,voff=-0.8) RLDRAIN c.ca n12 n8 = 1.7e-9₹RSLC1 c.cb n15 n14 = 2.5e-9 RSLC2 € c.cin n6 n8 = 6.0e-9ISCI dp.dbody n7 n5 = model=dbodymod DBREAK 1 dp.dbreak n5 n11 = model=dbreakmod RDRAIN <u>6</u> 8 dp.dplcap n10 n5 = model=dplcapmod FSG **DBODY EVTHRES** spe.ebreak n11 n7 n17 n18 = 102.5 19 8 **MWEAK** LGATE **EVTEMP** spe.eds n14 n8 n5 n8 = 1 **RGATE** 18 22 EBREAK spe.egs n13 n8 n6 n8 = 1 **▼**MMED spe.esg n6 n10 n6 n8 = 1 **←**MSTRO RLGATE spe.evthres n6 n21 n19 n8 = 1 LSOURCE CIN spe.evtemp n20 n6 n18 n22 = 1 SOURCE **RSOURCE** i.it n8 n17 = 1RLSOURCE I.lgate n1 n9 = 5.61e-9RBREAK 15 I.ldrain n2 n5 = 1.0e-9 I.Isource n3 n7 = 2.7e-9**₹**RVTEMP S2B 19 res.rlgate n1 n9 = 56.1 IT res.rldrain n2 n5 = 10 VBAT res.rlsource n3 n7 = 27 EGS **EDS** m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u **RVTHRES** m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u res.rbreak n17 n18 = 1, tc1=1.0e-3,tc2=-1.7e-6 res.rdrain n50 n16 = 3.8e-3, tc1=8.5e-3,tc2=2.8e-5 res.rgate n9 n20 = 1.1 res.rslc1 n5 n51 = 1.0e-6, tc1=2.0e-3,tc2=2.0e-6 res.rslc2 n5 n50 = 1.0e3res.rsource n8 n7 = 2.5e-3, tc1=4e-3,tc2=1e-6 res.rvthres n22 n8 = 1, tc1=-4.0e-3,tc2=-1.8e-5 res.rvtemp n18 n19 = 1, tc1=-4.4e-3,tc2=2.2e-6 sw vcsp.s1a n6 n12 n13 n8 = model=s1amod sw vcsp.s1b n13 n12 n13 n8 = model=s1bmod sw\_vcsp.s2a n6 n15 n14 n13 = model=s2amod sw\_vcsp.s2b n13 n15 n14 n13 = model=s2bmod v.vbat n22 n19 = dc=1 equations { i (n51->n50) +=iscl iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))\*((abs(v(n5,n51)\*1e6/350))\*\*3))







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Datasheet Identification	Product Status	Definition
Advance Information Formative / In Design		Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary First Production		Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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