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**July 2013** 

## **FDMC7208S**

## Dual N-Channel PowerTrench<sup>®</sup> MOSFET Q1: 30 V, 12 A, 9.0 m $\Omega$ Q2: 30 V, 16 A, 6.4 m $\Omega$

#### **Features**

Q1: N-Channel

■ Max  $r_{DS(on)} = 9.0 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 12 \text{ A}$ 

■ Max  $r_{DS(on)}$  = 11.0 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 11 A

Q2: N-Channel

■ Max  $r_{DS(on)} = 6.4 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 16 \text{ A}$ 

■ Max  $r_{DS(on)} = 7.5 \text{ m}\Omega$  at  $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 13.5 \text{ A}$ 

■ Termination is Lead-free and RoHS Compliant

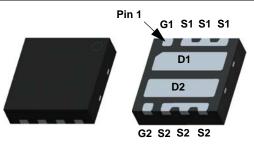


#### **General Description**

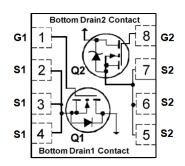
This device includes two 30V N-Channel MOSFETs in a dual Power 33 (3 mm X 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

#### **Applications**

- Computing
- Communications
- General Purpose Point of Load
- Notebook System



Power 33



### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V <sub>DS</sub>	Drain to Source Voltage		30	30	V
$V_{GS}$	Gate to Source Voltage	(Note 4)	±20	±12	V
	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25 °C	22	26	
$I_D$	-Continuous	T <sub>A</sub> = 25 °C	12 <sup>1a</sup>	16 <sup>1b</sup>	Α
	-Pulsed		60	80	
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 3)	21	21	mJ
D	Power Dissipation for Single Operation	T <sub>A</sub> = 25 °C	1.9 <sup>1a</sup>	1.9 <sup>1b</sup>	W
$P_{D}$	Power Dissipation for Single Operation	T <sub>A</sub> = 25 °C	0.8 <sup>1c</sup>	0.8 <sup>1d</sup>	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range			+150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 <sup>1a</sup>	65 <sup>1b</sup>	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	155 <sup>1c</sup>	155 <sup>1d</sup>	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7208S	FDMC7208S	Power 33	13 "	12 mm	3000 units

## **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter Test Conditi		Type	Min	Тур	Max	Units
Off Chara	octeristics						
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$ $I_D = 1 mA, V_{GS} = 0 V$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, referenced to 25 °C $I_D$ = 10 mA, referenced to 25 °C	Q1 Q2		27 21		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	Q1 Q2			1 500	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V V <sub>GS</sub> = 12 V, V <sub>DS</sub> = 0 V	Q1 Q2			100 100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$ $I_D = 1 \text{ mA}, V_{GS} = 0 V$	Q1 Q2	1.2 1.2	1.7 1.6	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C $I_D$ = 10 mA, referenced to 25 °C	Q1 Q2		-5 -3		mV/°C
_	Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 11 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}, T_J = 125 ^{\circ}\text{C}$	Q1		6.7 8.8 9.2	9.0 11.0 12.4	m0
r <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 13.5 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}, T_J = 125 ^{\circ}\text{C}$	Q2		4.7 5.3 6.4	6.4 7.5 6.8	mΩ
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 12 \text{ A}$ $V_{DS} = 5 \text{ V}, I_{D} = 16 \text{ A}$	Q1 Q2		53 80		S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	Q1: V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHZ	Q1 Q2		848 1685	1130 2245	pF
C <sub>oss</sub>	Output Capacitance	Q2:	Q1 Q2		270 432	360 575	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHZ}$	Q1 Q2		36 42	55 65	pF
R <sub>g</sub>	Gate Resistance		Q1 Q2	0.1 0.1	1.1 1.0	2.5 2.5	Ω

## **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time			Q1 Q2	6 7	12 14	ns
t <sub>r</sub>	Rise Time	Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 12	Q1 Q2	2	10 10	ns	
t <sub>d(off)</sub>	Turn-Off Delay Time	Q2: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 16	SA Roon = 6.0	Q1 Q2	16 23	29 36	ns
t <sub>f</sub>	Fall Time	To v, ij = 10	Q1 Q2	2 2	10 10	ns	
Qg	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V		Q1 Q2	13 26	18 36	nC
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0 V to 5 V	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 12 A	Q1 Q2	6.7 14	9.4 20	nC
$Q_{gs}$	Gate to Source Gate Charge		Q2 Vpp = 15 V	Q1 Q2	2.3 3.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 16 A		Q1 Q2	1.8 2.7		nC

## **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

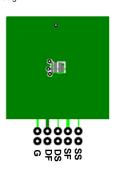
**Parameter** 

Drain-S	Source Diode Characteristics						
V <sub>SD</sub> Sou		$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	Q1	0.72	1.2	
	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 12 \text{ A}$	(Note 2)	Q1	0.82	1.2	V
	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	Q2	0.70	1.2	V
		$V_{GS} = 0 \text{ V}, I_{S} = 16 \text{ A}$	(Note 2)	Q2	0.82	1.2	
	Dayaraa Daaayar / Tima	Q1		Q1	21	34	
<sup>L</sup> rr	Reverse Recovery Time	$I_F = 12 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu$	ıs	Q2	21	33	ns
0	Daylaraa Daasyari, Charga	Q2	=	Q1	6	12	
Q <sub>rr</sub>	Reverse Recovery Charge	$I_F = 16 \text{ A}, \text{ di/dt} = 300 \text{ A/}\mu\text{s}$		Q2	16	28	nC

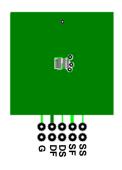
**Test Conditions** 

**Symbol** 

1.1. R<sub>0,IA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0,IC</sub> is guaranteed by design while R<sub>0,CA</sub> is determined by the user's board design.



a. 65 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 65 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

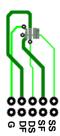
Туре

Min

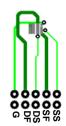
Тур

Max

Units



c. 155 °C/W when mounted on a minimum pad of 2 oz copper



d. 155 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%. 3. Q1: E<sub>AS</sub> of 21 mJ is based on starting T<sub>J</sub> = 25 °C, L = 0.3 mH, I<sub>AS</sub> = 12 A, V<sub>DD</sub> = 27 V, V<sub>GS</sub> = 10 V. 100% tested at L = 3 mH, I<sub>AS</sub> = 5.2 A. Q1: E<sub>AS</sub> of 21 mJ is based on starting T<sub>J</sub> = 25 °C, L = 0.3 mH, I<sub>AS</sub> = 12 A, V<sub>DD</sub> = 27 V, V<sub>GS</sub> = 10 V. 100% tested at L = 3 mH, I<sub>AS</sub> = 5.4 A. 4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied

3

## Typical Characteristics (Q1 N-Channel) T<sub>J</sub> = 25°C unless otherwise noted

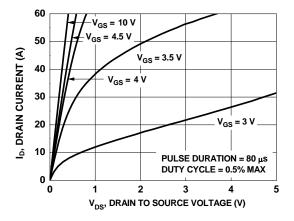


Figure 1. On Region Characteristics

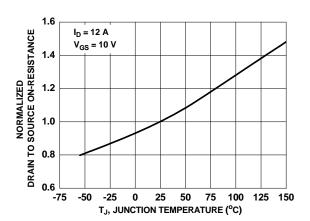


Figure 3. Normalized On Resistance vs Junction Temperature

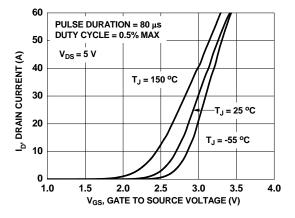


Figure 5. Transfer Characteristics

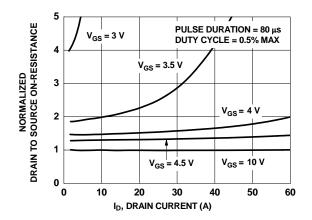


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

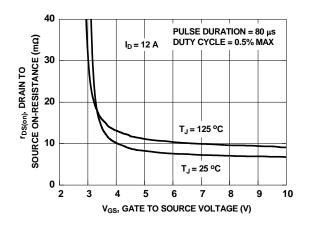


Figure 4. On-Resistance vs Gate to Source Voltage

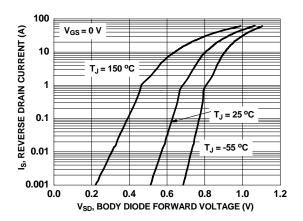


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics (Q1 N-Channel) $T_J = 25$ °C unless otherwise noted

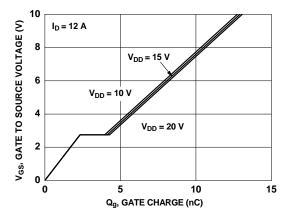


Figure 7. Gate Charge Characteristics

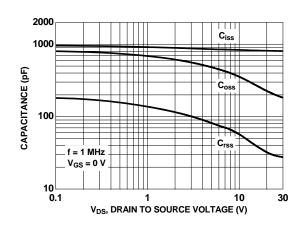


Figure 8. Capacitance vs Drain to Source Voltage

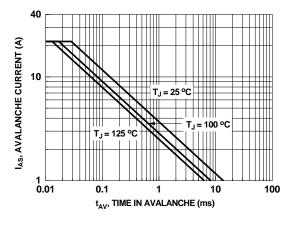


Figure 9. Unclamped Inductive Switching Capability

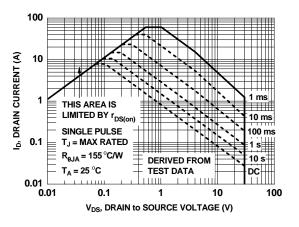


Figure 10. Forward Bias Safe Operating Area

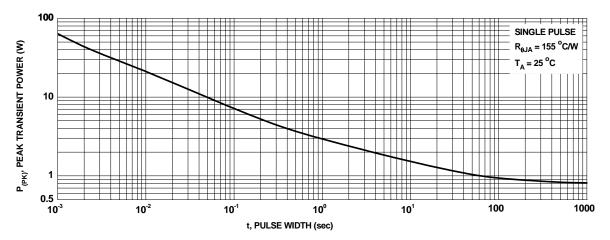


Figure 11. Single Pulse Maximum Power Dissipation

## Typical Characteristics (Q1 N-Channel) $T_J = 25$ °C unless otherwise noted

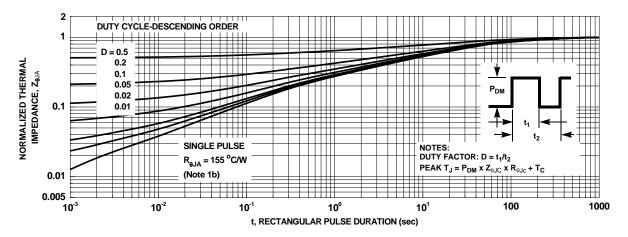


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

## Typical Characteristics (Q2 N-Channel) T<sub>J</sub> = 25 °C unless otherwise noted

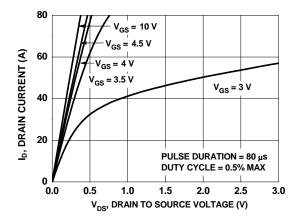


Figure 14. On-Region Characteristics

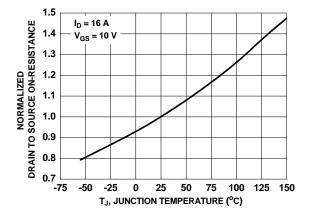


Figure 16. Normalized On-Resistance vs Junction Temperature

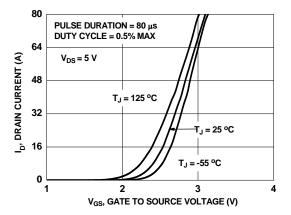


Figure 18. Transfer Characteristics

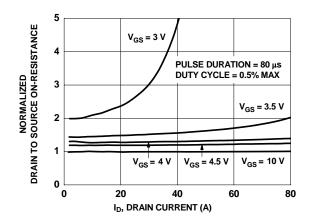


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

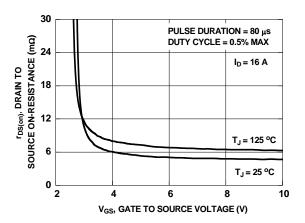


Figure 17. On-Resistance vs Gate to Source Voltage

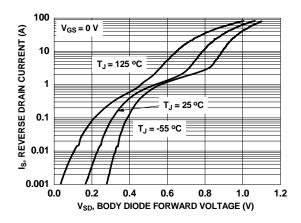


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

### Typical Characteristics (Q2 N-Channel) T<sub>J</sub> = 25°C unless otherwise noted

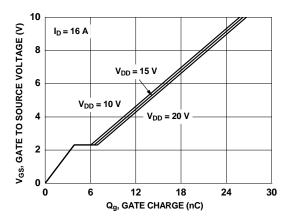


Figure 20. Gate Charge Characteristics

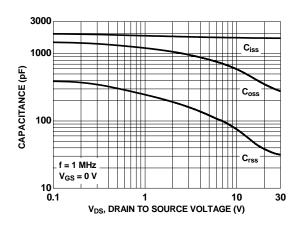


Figure 21. Capacitance vs Drain to Source Voltage

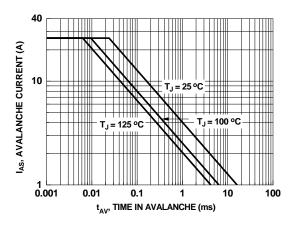


Figure 22. Unclamped Inductive Switching Capability

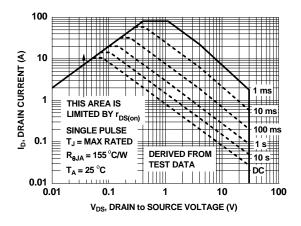


Figure 23. Forward Bias Safe Operating Area

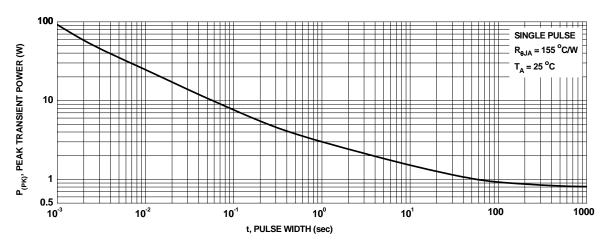


Figure 24. Single Pulse Maximum Power Dissipation

## Typical Characteristics (Q2 N-Channel) $T_J = 25$ °C unless otherwise noted

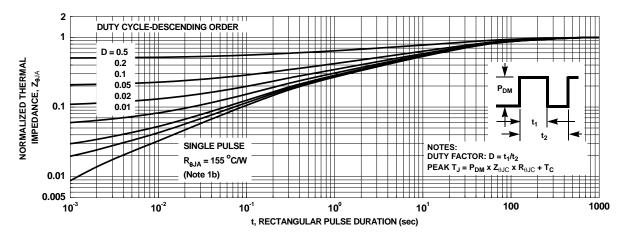


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

## Typical Characteristics (continued)

## SyncFET<sup>TM</sup> Schottky body diode Characteristics

Fairchild's SyncFET<sup>TM</sup> process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverses recovery characteristic of the FDMC7208S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

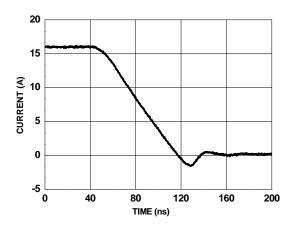


Figure 27. FDMC7208S SyncFET<sup>TM</sup> body diode reverse recovery characteristic

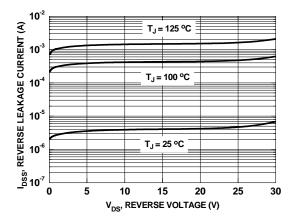
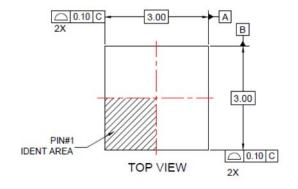
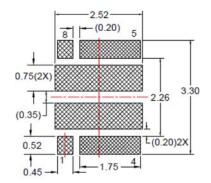
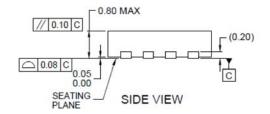


Figure 28. SyncFET<sup>TM</sup> body diode reverses leakage versus drain-source voltage

## **Dimensional Outline and Pad Layout**



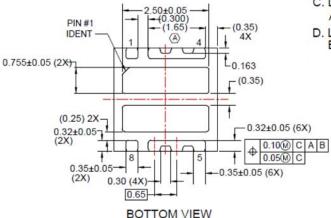




RECOMMENDED LAND PATTERN

#### NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY







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