

TVS Diode

Transient Voltage Suppressor Diodes

ESD24VL1B Series

Low Capacitance Bi-directional ESD / Transient Protection Diode

ESD24VL1B-02LS
ESD24VL1B-02LRH

Data Sheet

Revision 1.1, 2012-05-04
Final

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Revision History: Rev. 1.0, 2011-12-06

Page or Item	Subjects (major changes since previous revision)
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Revision 1.1, 2012-05-04

7 + 8	ESD air and contact discharge change
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8	Parameter V_{BR} inserted in Table 3-2
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1 Low Capacitance Bi-directional ESD / Transient Protection Diode

1.1 Features

- ESD / transient protection according to:
 - IEC61000-4-2 (ESD): ± 20 kV (air), ± 18 kV (contact)
 - IEC61000-4-4 (EFT): 40 A (5/50 ns)
 - IEC61000-4-5 (surge): 1 A (8/20 μ s)
- Bi-directional, working voltage up to $V_{RWM} = \pm 24$ V
- Low capacitance: $C_L = 2.5$ pF (typical)
- Very low reverse current. $I_R = < 1$ nA (typical)
- Pb-free (RoHS compliant) and halogen free package



1.2 Application Examples

- ESD protection of USB-battery charger interface
- LCD Backlight protection
- NFC antenna protection
- Protection of high speed bus rated up to ± 24 V

2 Product Description

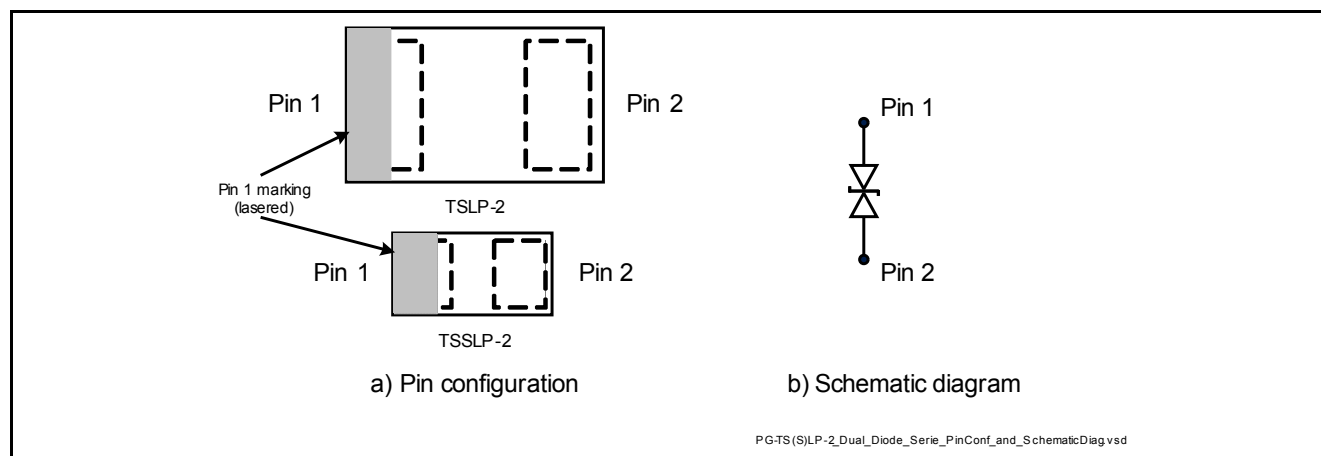


Figure 2-1 Pin Configuration and Schematic Diagram

Table 2-1 Ordering Information

Type	Package	Configuration	Marking code
ESD24VL1B-02LS	PG-TSSLP-2-1	1 line, bi-directional	n
ESD24VL1B-02LRH	PG-TSLP-2-17	1 line, bi-directional	n

3 Characteristics

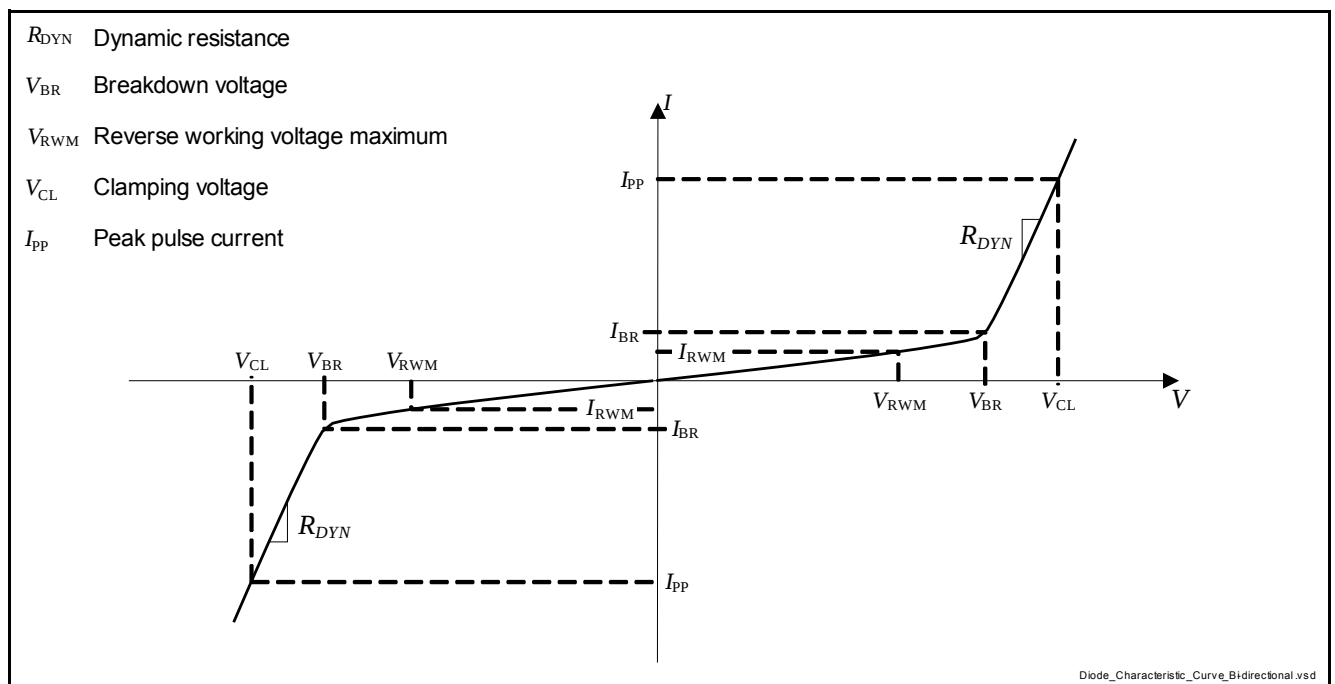
Table 3-1 Maximum Ratings at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD air discharge ¹⁾	V_{ESD}	-20	–	20	kV
ESD contact discharge ¹⁾		-18	–	18	
Peak pulse current ($t_p = 8/20\text{ }\mu\text{s}$) ²⁾	I_{PP}	-1	–	1	A
Operating temperature range	T_{OP}	-55	–	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-65	–	150	$^\circ\text{C}$

1) V_{ESD} according to IEC61000-4-2

2) I_{PP} according to IEC61000-4-5

3.1 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified


Figure 3-1 Definitions of electrical characteristics
Table 3-2 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-24	–	24	V	
Breakdown voltage	V_{BR}	24.3	25	–		$I_{\text{R}} = 1\text{ mA}$
Reverse current	I_{R}	–	<1	50	nA	$V_{\text{R}} = 24\text{ V}$

Table 3-3 RF Characteristics at $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

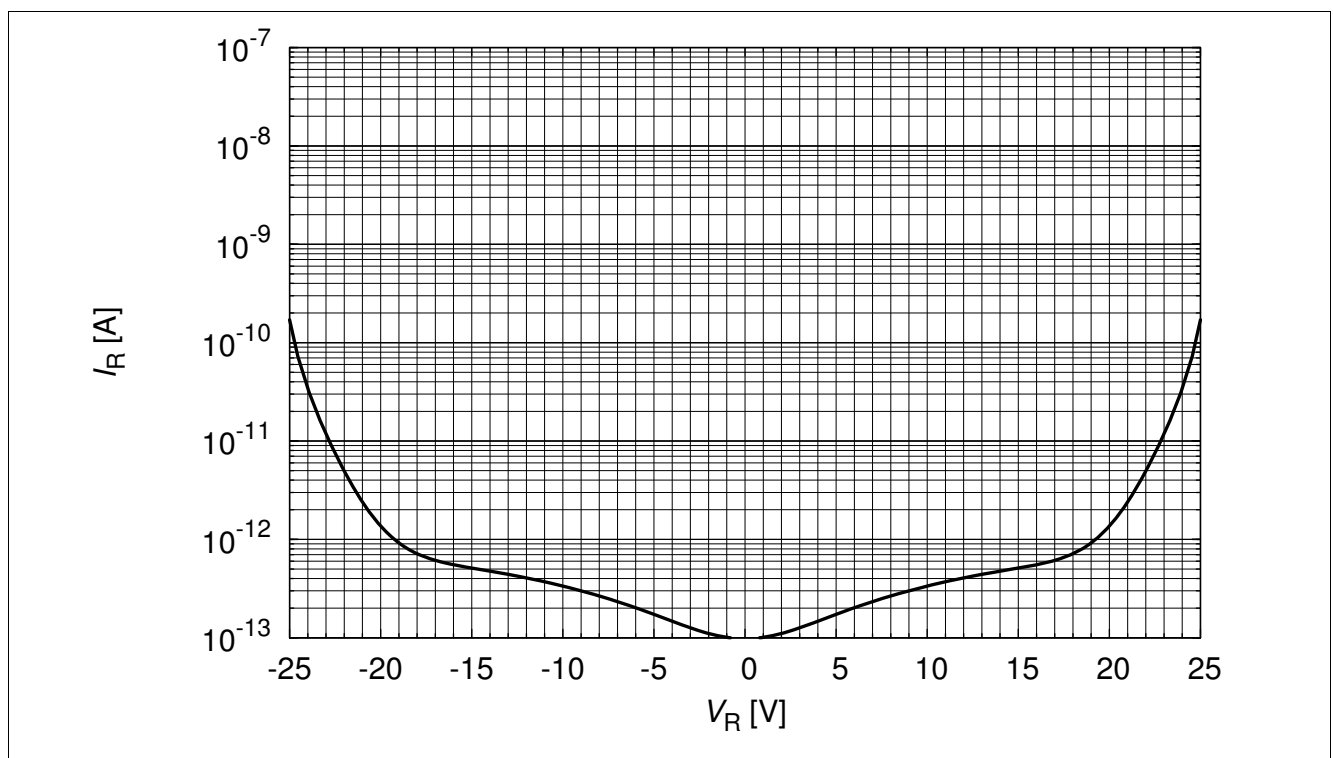
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	2.5	3.5	pF	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$

Table 3-4 ESD Characteristics at $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ¹⁾	V_{CL}	–	55	–	V	$I_{PP} = 16\text{ A}$
Dynamic resistance ¹⁾	R_{DYN}	–	1.0	–	Ω	

1)Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$, averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 10\text{ A}$ and $I_{PP2} = 40\text{ A}$.

3.2 Typical Characteristics at $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified


Figure 3-2 Reverse current: $I_R = f(V_R)$

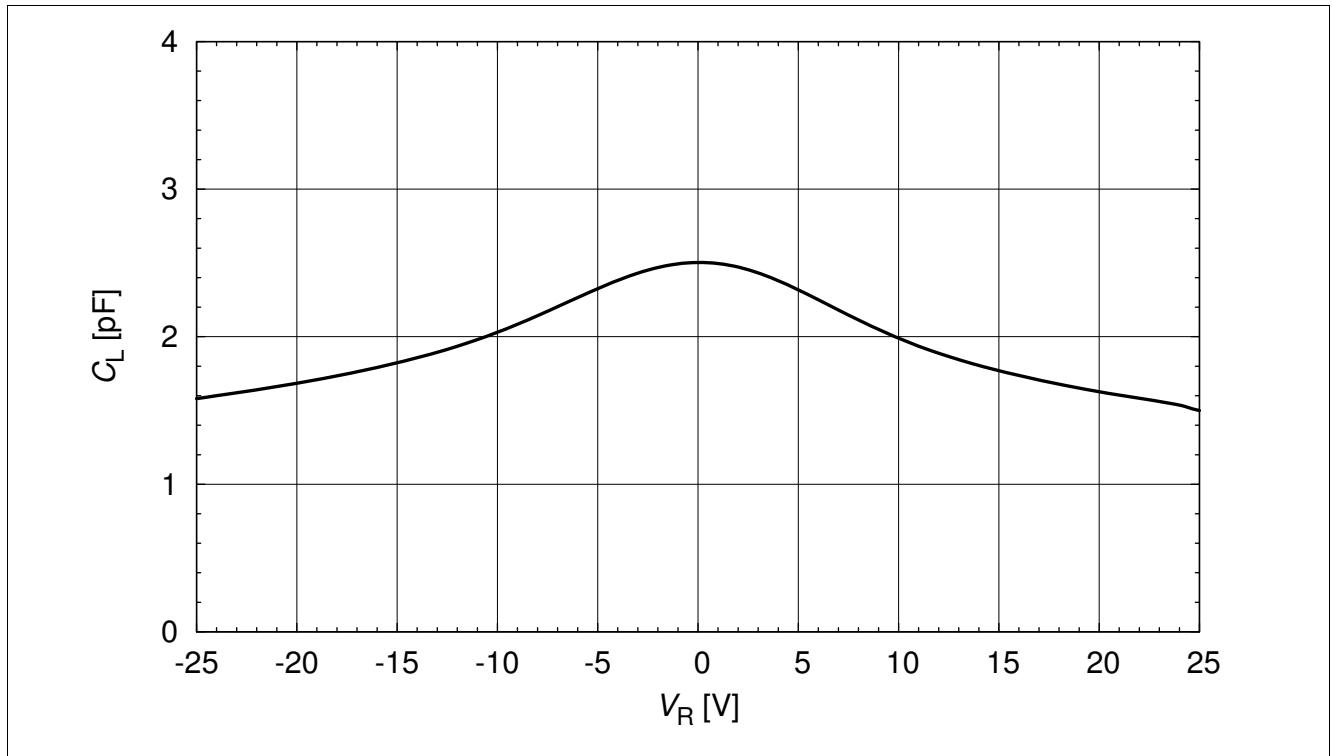


Figure 3-3 Line capacitance: $C_L = f(V_R)$, $f = 1\text{MHz}$

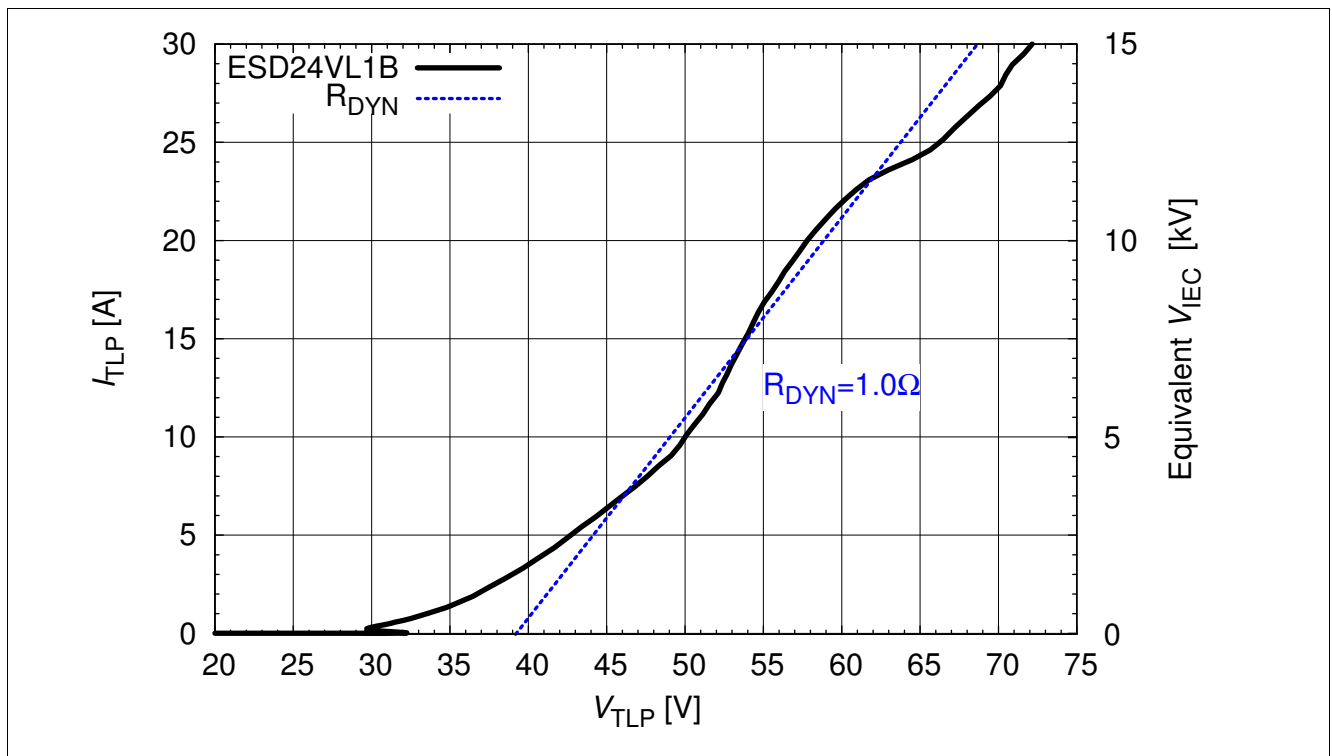


Figure 3-4 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1]

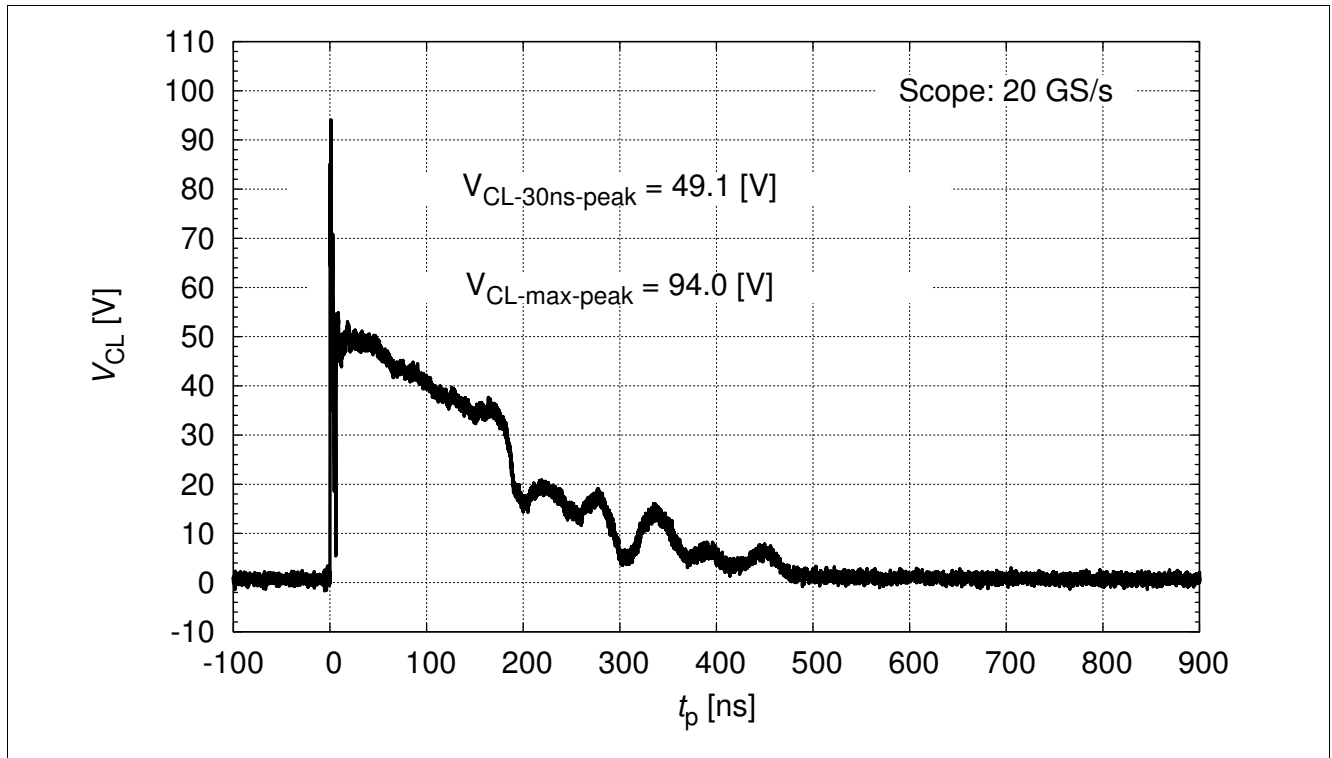


Figure 3-5 IEC61000-4-2 : $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

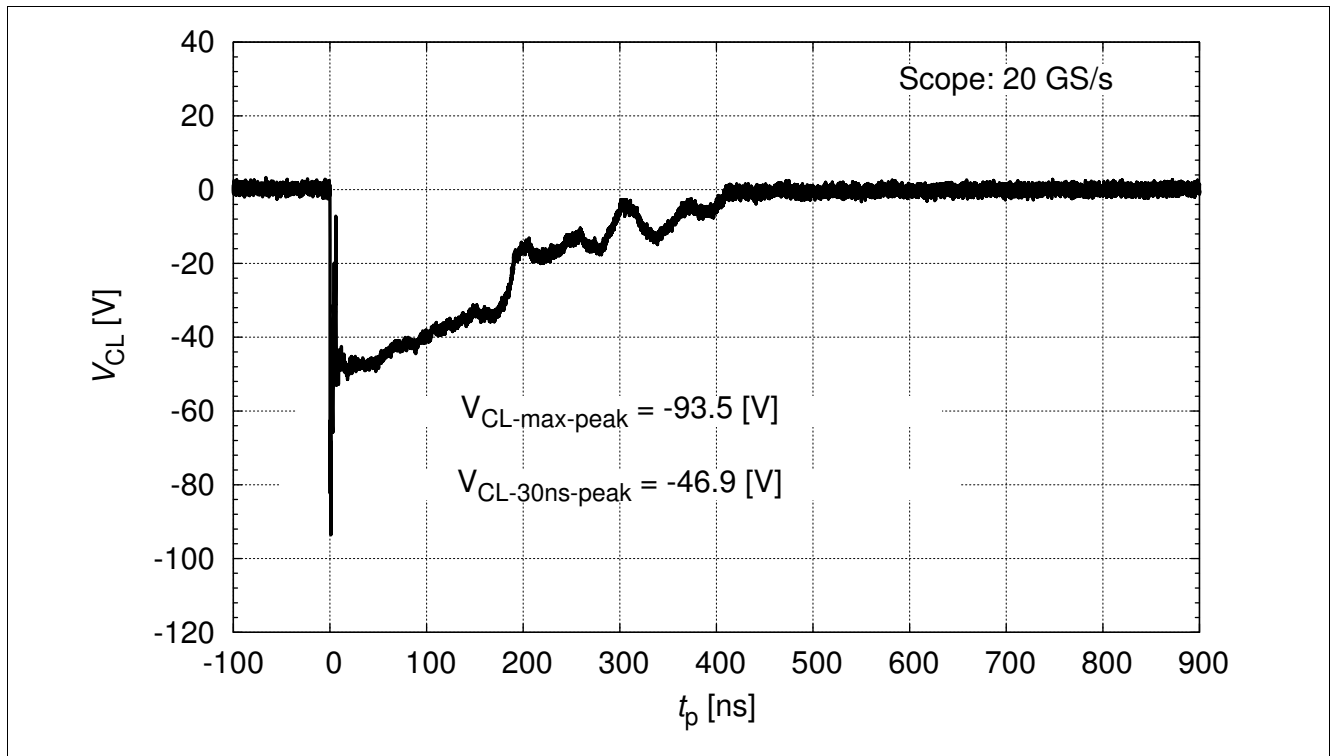


Figure 3-6 IEC61000-4-2 : $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

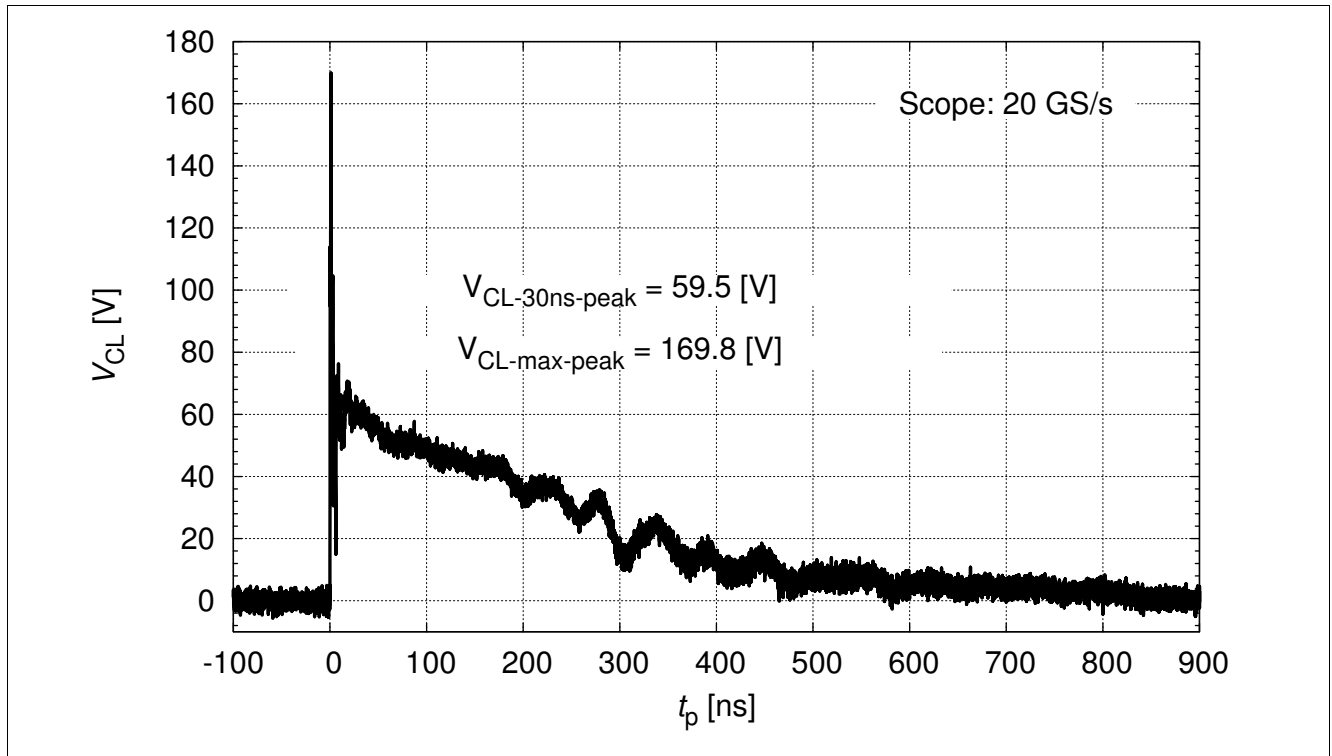


Figure 3-7 IEC61000-4-2 : $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

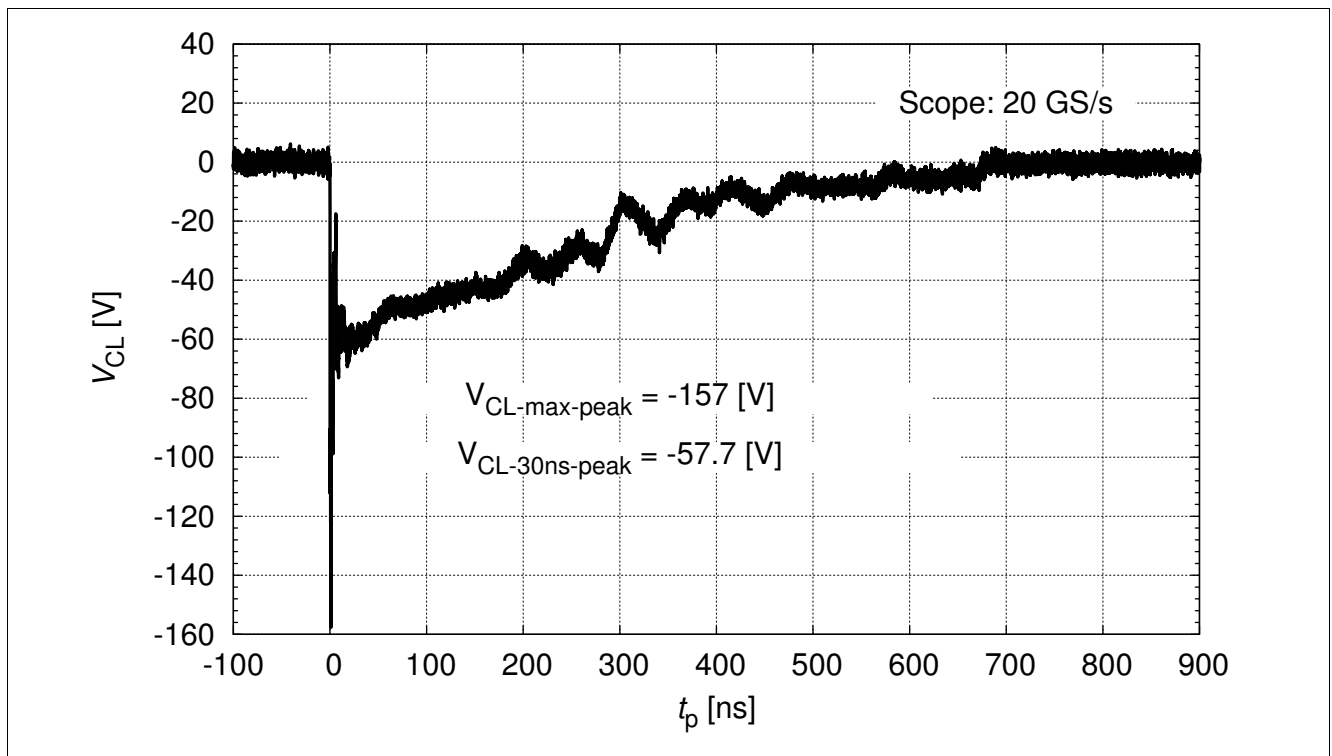


Figure 3-8 IEC61000-4-2 : $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

4 Application Information

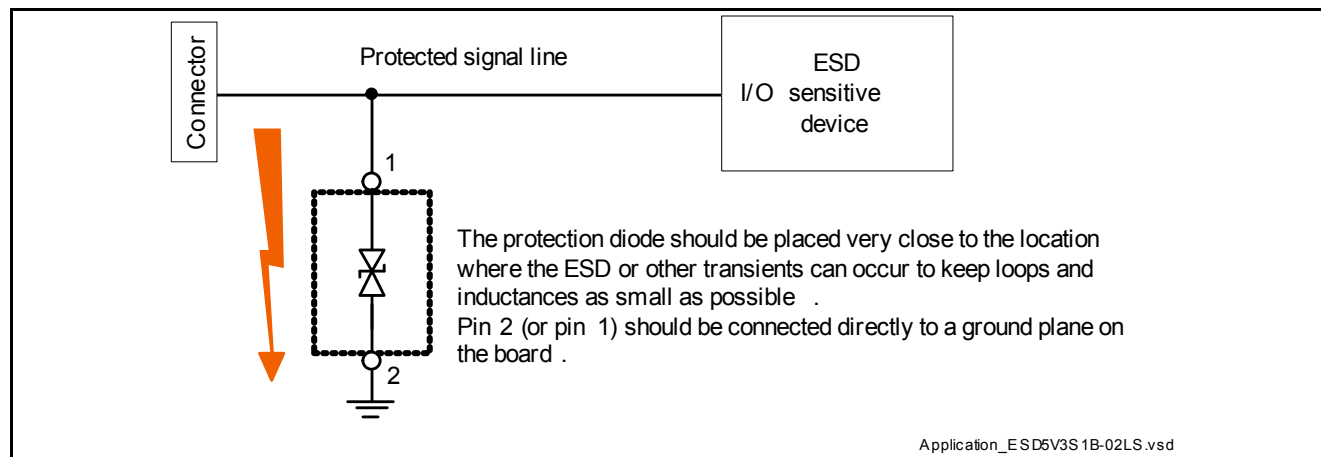


Figure 4-1 Single line, bi-directional ESD / Transient protection

5 Ordering Information Scheme (Examples)

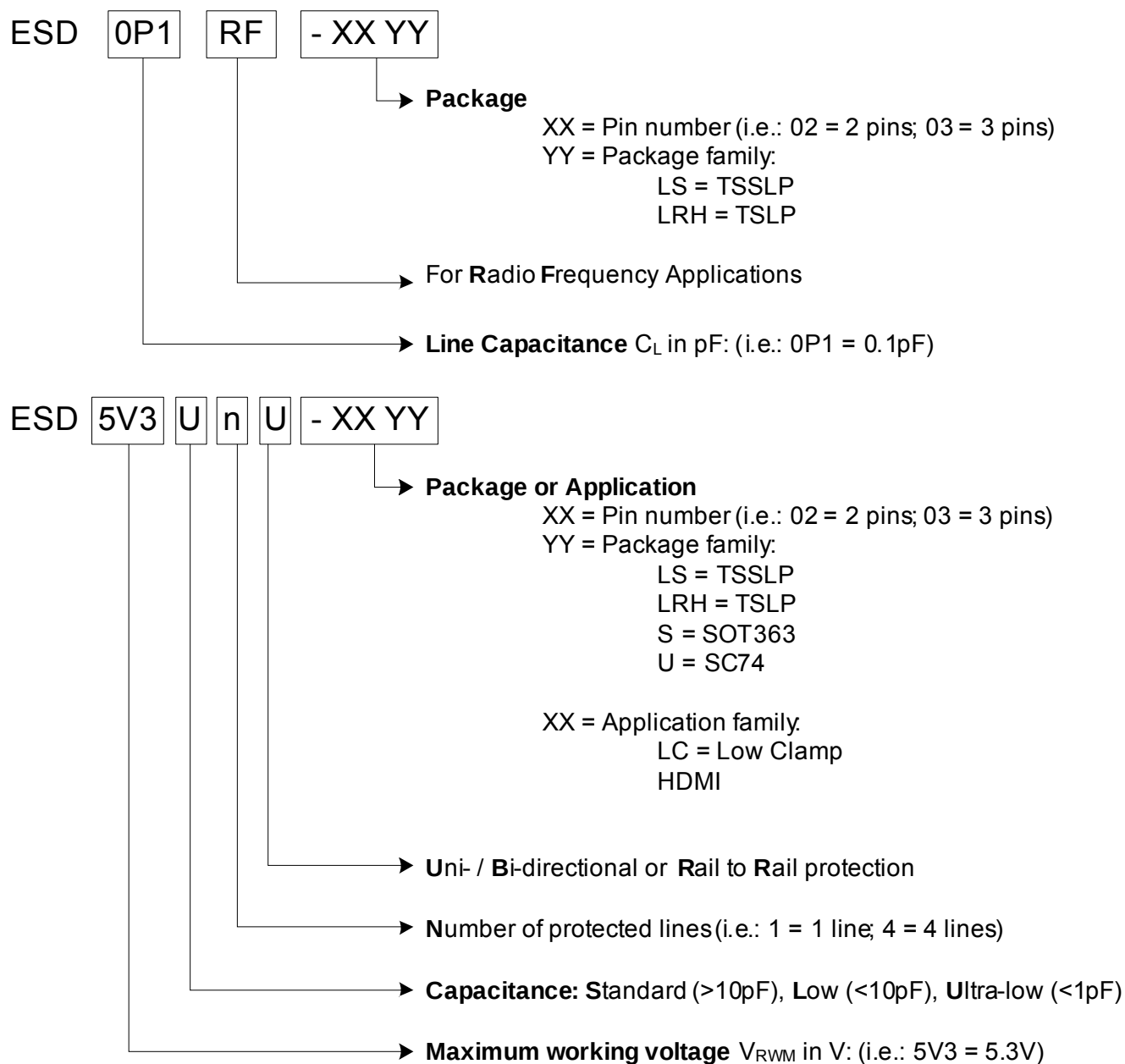


Figure 5-1 Ordering information scheme

6 Package Information

6.1 PG-TSLP-2-17 (mm) [2]

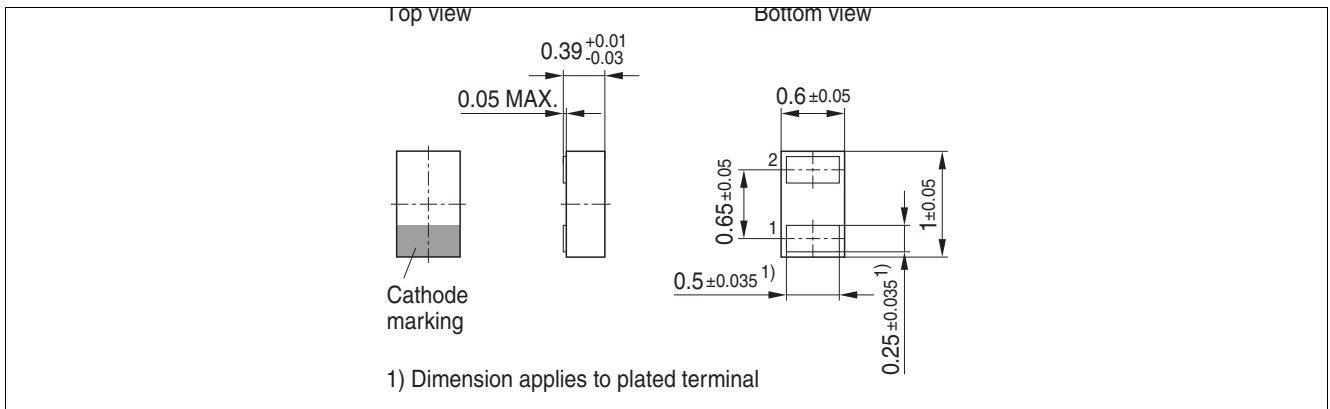


Figure 6-1 PG-TSLP-2-17: Package overview

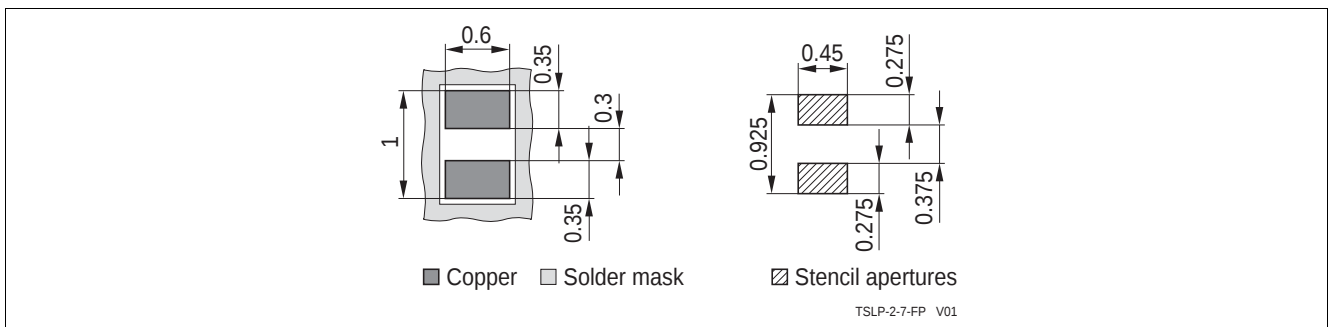


Figure 6-2 PG-TSLP-2-17: Footprint

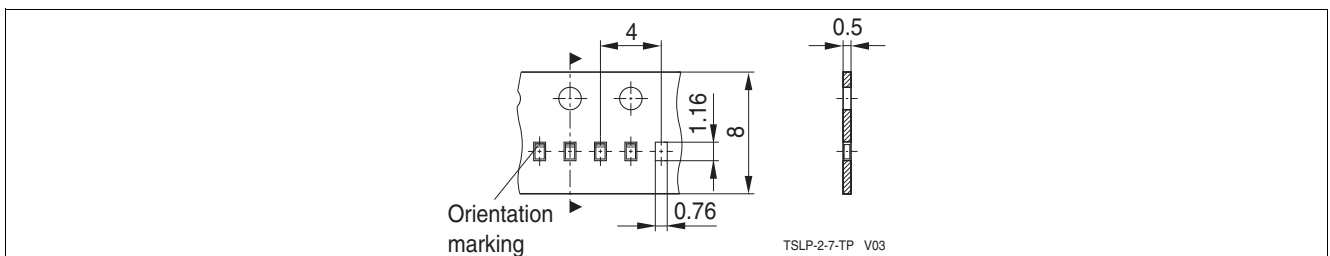


Figure 6-3 PG-TSLP-2-17: Packing

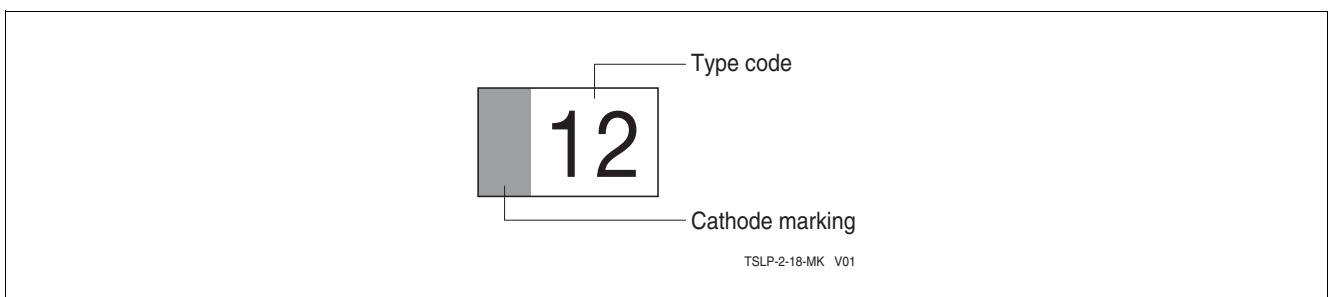


Figure 6-4 PG-TSLP-2-17: Marking (example)

6.2 PG-TSSLP-2-1 (mm) [2]

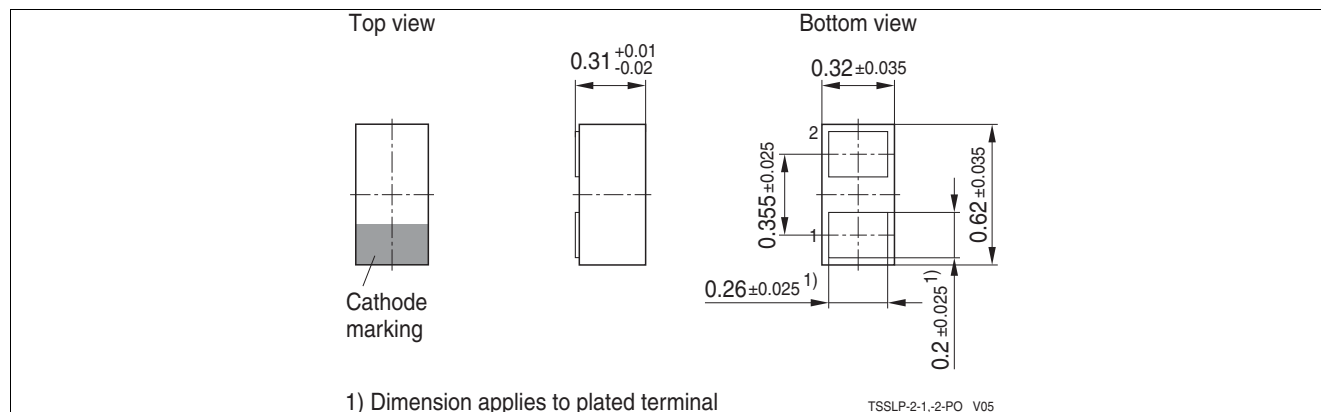


Figure 6-5 PG-TSSLP-2-1: Package overview

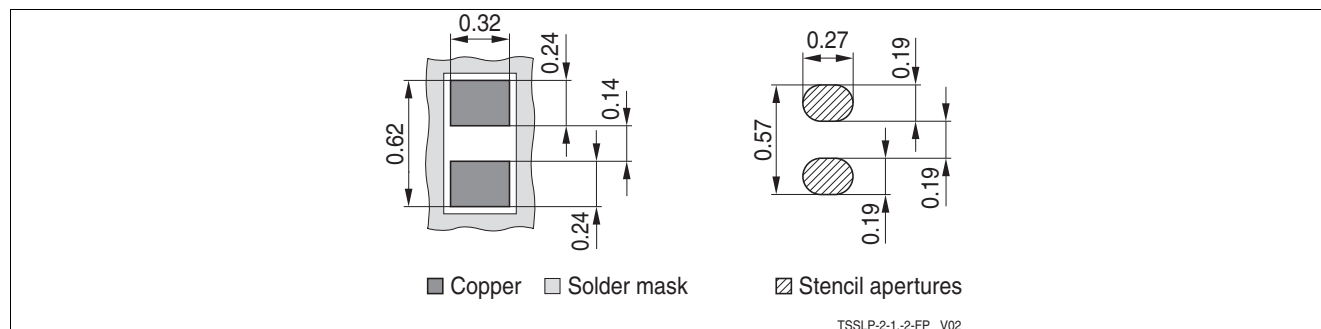


Figure 6-6 PG-TSSLP-2-1: Footprint

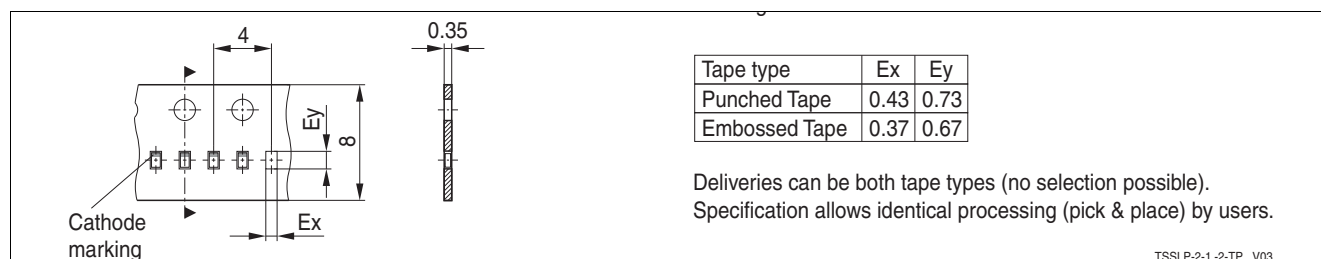


Figure 6-7 PG-TSSLP-2-1: Packing

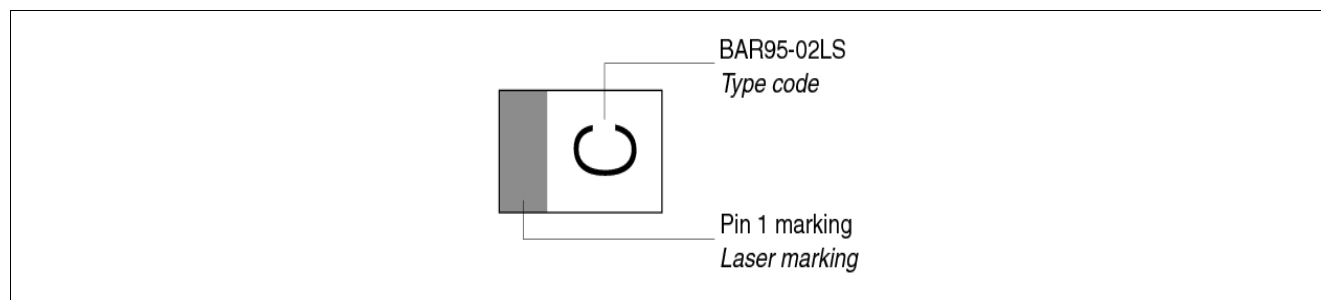


Figure 6-8 PG-TSSLP-2-1: Marking (example)

References

- [1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

Terminology

C_L	Line capacitance
DSC	Digital Still Camera
EFT	Electrical Fast Transient
ESD	Electrostatic Discharge
I_{PP}	Peak pulse current
I_R	Reverse current
LCD	Liquid Crystal Display
P_{PK}	Peak pulse power
R_{DYN}	Dynamic resistance
RoHs	Restriction of Hazardous Substance directive
STB	Set-Top-Box
T_A	Ambient temperature
T_{OP}	Operation temperature
t_p	Pulse duration
T_{stg}	Storage temperature
V_{BR}	Breakdown voltage
V_{CL}	Reverse clamping voltage
V_{ESD}	Electrostatic discharge voltage
V_R	Reverse voltage
V_{RWM}	Reverse working voltage maximum

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[illegible]

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