

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7W74FU, TC7W74FK

## D-Type Flip Flop with Preset and Clear

The TC7W74 is a high speed C<sup>2</sup>MOS D Flip Flop fabricated with silicon gate C<sup>2</sup>MOS technology.

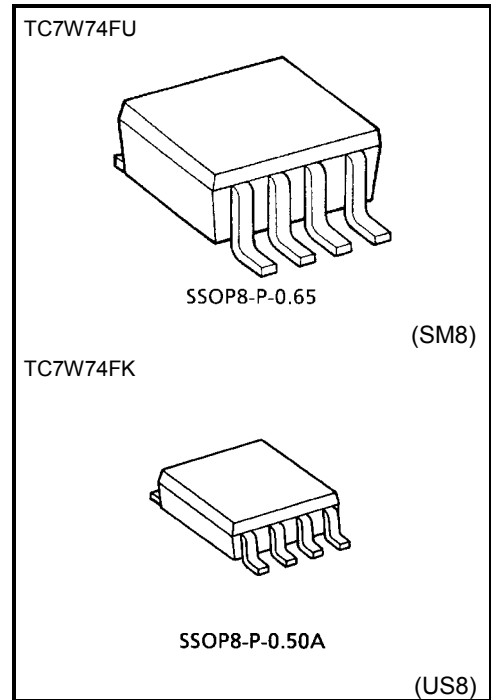
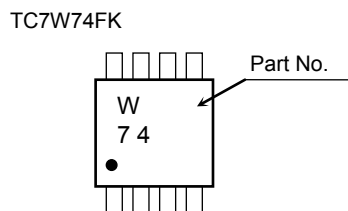
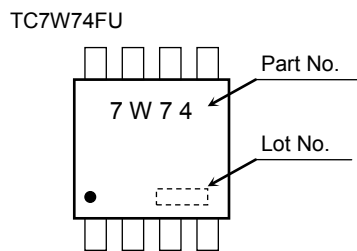
It achieves the high speed operation similar to equivalent LSTTL while maintaining the C<sup>2</sup>MOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse CLEAR and PRESET are independent of the CLOCK and are accomplished by setting the appropriate input to an "L" level Input is equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{MAX} = 77 \text{ MHz (typ.) at } V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 2 \mu\text{A (max) at } T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4 \text{ mA (min)}$
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$

### Marking



Weight  
 SSOP8-P-0.65: 0.02 g (typ.)  
 SSOP8-P-0.50A: 0.01 g (typ.)

Start of commercial production  
1992-02

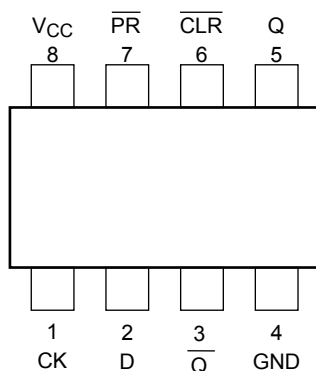
## Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7	V
DC input voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±25	mA
Power dissipation	P <sub>D</sub>	300 (SM8)	mW
		200 (US8)	
Storage temperature range	T <sub>stg</sub>	-65 to 150	°C
Lead temperature (10 s)	T <sub>L</sub>	260	°C

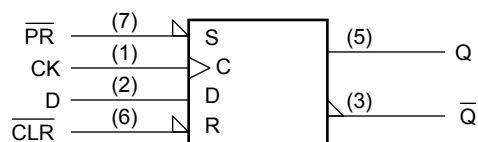
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Pin Configuration (top view)



## Logic Diagram



## Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	$\bar{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	$\uparrow$	L	H	—
H	H	H	$\uparrow$	H	L	—
H	H	X	$\downarrow$	Qn	$\bar{Q}n$	No Change

## Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature range	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V)	ns
		0 to 500 ( $V_{CC} = 4.5$ V)	
		0 to 400 ( $V_{CC} = 6.0$ V)	

## Electrical Characteristics

### DC Electrical Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$		Unit					
			$V_{CC}$ (V)	Min	Typ.	Max	Min		Max				
Input voltage	High level	—	2.0	1.5	—	—	1.5	—	V				
			4.5	3.15	—	—	3.15	—					
			6.0	4.2	—	—	4.2	—					
	Low level		2.0	—	—	0.5	—	0.5					
			4.5	—	—	1.35	—	1.35					
			6.0	—	—	1.8	—	1.8					
Output voltage	High level	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V			
				4.5	4.4	4.5	—	4.4	—				
				6.0	5.9	6.0	—	5.9	—				
				$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	—	4.13		—		
					6.0	5.68	5.80	—	5.63		—		
					Low level	$V_{OL}$	$I_{OL} = 20 \mu\text{A}$	2.0	—		0	0.1	—
	4.5		—	0				0.1	—		0.1		
	6.0		—	0				0.1	—		0.1		
	$I_{OL} = 4 \text{ mA}$		4.5	—				0.17	0.26		—	0.33	
			$I_{OL} = 5.2 \text{ mA}$	4.5				—	0.18		0.26	—	0.33
				6.0				—	0.18		0.26	—	0.33
	Input leakage current		$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	$\pm 0.1$	—		$\pm 1.0$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	2.0	—	20.0	$\mu\text{A}$				

### Timing Requirements (input $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width (CLOCK)	t <sub>W</sub> (L) t <sub>W</sub> (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	t <sub>W</sub> (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	t <sub>s</sub>	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t <sub>h</sub>	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	t <sub>rem</sub>	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	4	5	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

### AC Characteristics (C<sub>L</sub> = 15 pF, V<sub>CC</sub> = 5 V, Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t <sub>TLH</sub> t <sub>THL</sub>	—	—	6	12	ns
Propagation delay time (CLOCK-Q, $\overline{\text{Q}}$ )	t <sub>pLH</sub> t <sub>pHL</sub>	—	—	13	26	ns
Propagation delay time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ -Q, $\overline{\text{Q}}$ )	t <sub>pLH</sub> t <sub>pHL</sub>	—	—	14	26	ns
Maximum clock frequency	f <sub>MAX</sub>	—	36	77	—	MHz

**AC Electrical Characteristics (C<sub>L</sub> = 50 pF, input t<sub>r</sub> = t<sub>f</sub> = 6 ns)**

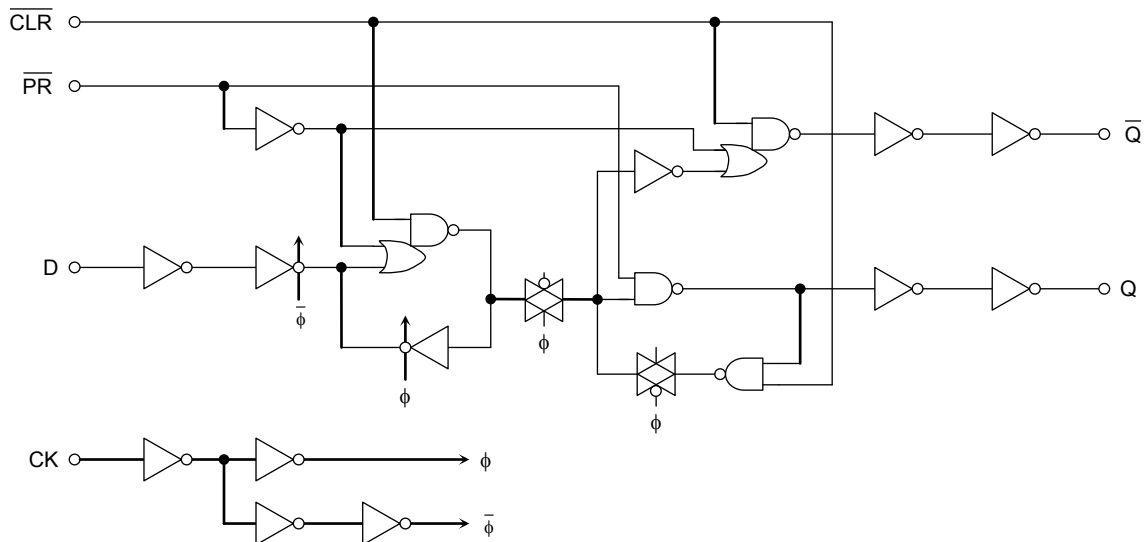
Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Output transition time	t <sub>TLH</sub> t <sub>THL</sub>	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CLOCK-Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	48	150	—	190	ns
			4.5	—	16	30	—	38	
			6.0	—	13	26	—	32	
Propagation delay time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ -Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	51	150	—	190	ns
			4.5	—	17	30	—	38	
			6.0	—	15	26	—	32	
Maximum clock frequency	f <sub>MAX</sub>	—	2.0	6	21	—	5	—	MHz
			4.5	31	63	—	25	—	
			6.0	36	67	—	29	—	
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub>	(Note)	—	34	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

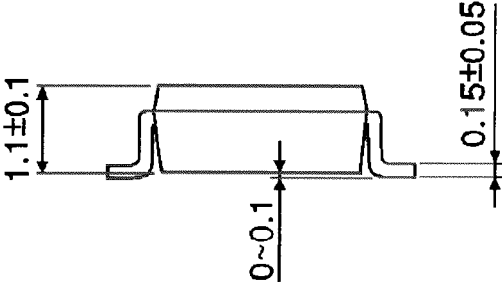
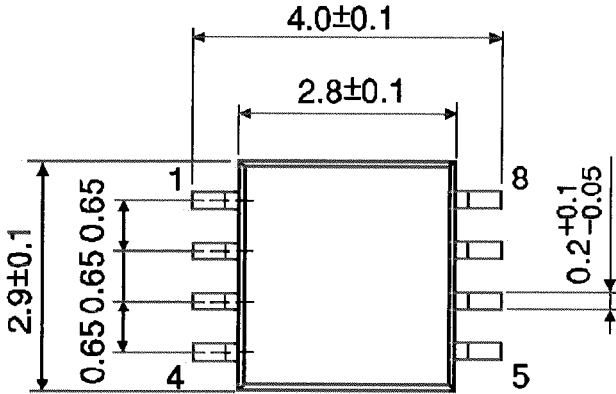
**System Diagram**



**Package Dimensions**

SSOP8-P-0.65

Unit : mm

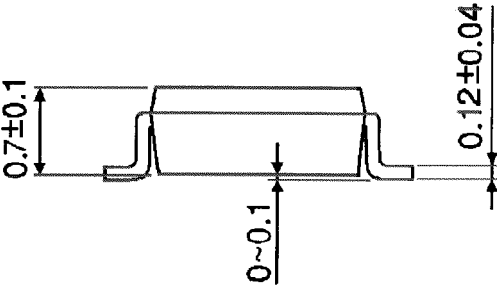
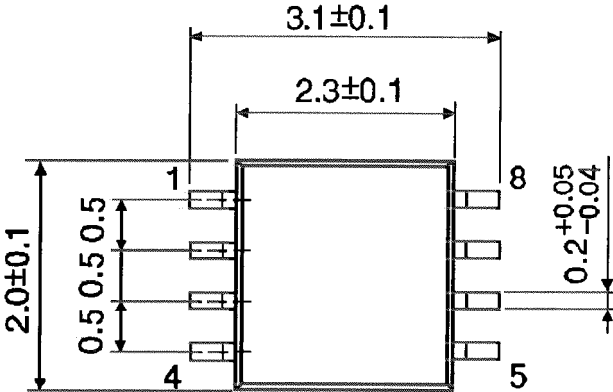


Weight: 0.02 g (typ.)

**Package Dimensions**

SSOP8-P-0.50A

Unit : mm



Weight: 0.01 g (typ.)

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