# TVS Diode

Transient Voltage Suppressor Diodes

# ESD206-B1-02 Series

Ultra Low Clamping Bi-directional ESD / Transient / Surge Protection Diode

ESD206-B1-02ELS
ESD206-B1-02EL

## Data Sheet

Revision 1.5, 2013-12-19
Final

Power Management & Multimarket

| Revision History, Rev 1.4, 2013-11-26 | |
|---|---|
| **Page or Item** | **Subjects (major changes since previous revision)** |
| **Revision 1.5, 2013-12-19** | |
| 5 | Update of Table 2-2) |
| | |
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| | |

# 1 Ultra Low Clamping Bi-directional ESD / Transient / Surge Protection Diode

## 1.1 Features

- ESD/Transient/Surge protection of one data / $V_{bus}$ line exceeding standard:
  - **IEC61000-4-2 (ESD): ±30 kV (air/contact discharge)**
  - **IEC61000-4-4 (EFT): ±50 A (5/50 ns)**
  - **IEC61000-4-5 (surge): ±6 A (8/20 µs)**
- Medium capacitance: $C_L$ **= 12 pF (typ.)**
- Bi-directional symmetrical working voltage: **-5.5 V to +5.5 V**
- Low leakage current
- Very low ESD clamping voltage: **8 V** (typ.)
- Very low dynamic resistance: **0.13 Ω** (typ.)
- Pb-free (RoHS compliant) and halogen free package

## 1.2 Application Examples

- Audio Line, Speaker, Headset, Microphone Protection
- Human Interface Devices (Keyboard, Touchpad, Buttons)

## 1.3 Product Description

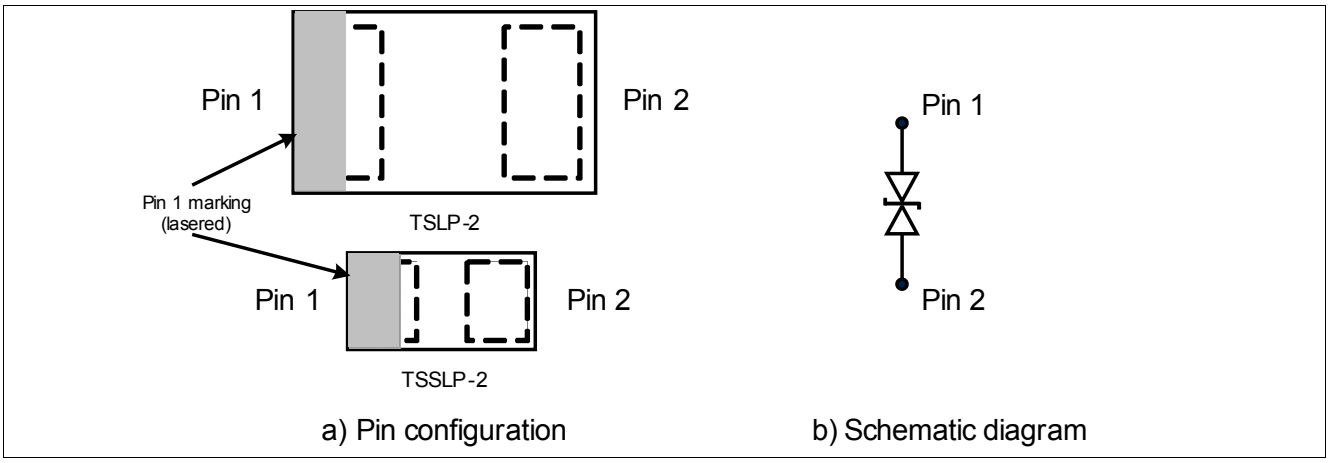


**Figure 1-1 Pin Configuration and Schematic Diagram**

**Table 1-1 Ordering Information**

| Type | Package | Configuration | Marking code |
|---|---|---|---|
| ESD206-B1-02ELS | TSSLP-2-3 | 1 line, bi-directional | r |
| ESD206-B1-02EL | TSLP-2-19 | 1 line, bi-directional | A3 |

# 2 Characteristics

## 2.1 Maximum Ratings

**Table 2-1 Maximum Ratings** at $T_A$ = 25 °C, unless otherwise specified[1)]

| Parameter | Symbol | Values | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| ESD[2)]air / contact discharge | $V_{ESD}$ | - | - | 30 | kV |
| Peak pulse current ($t_p$ = 8/20 µs)[3)] | $I_{PP}$ | - | - | 6 | A |
| Operating temperature range | $T_{OP}$ | -55 | - | 125 | °C |
| Storage temperature | $T_{stg}$ | -65 | - | 150 | °C |

1) Device is electrically symmetrical
2) $V_{ESD}$ according to IEC61000-4-2
3) $I_{PP}$ according to IEC61000-4-5

***Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.***

## 2.2 Electrical Characteristics at $T_A$ = 25 °C, unless otherwise specified

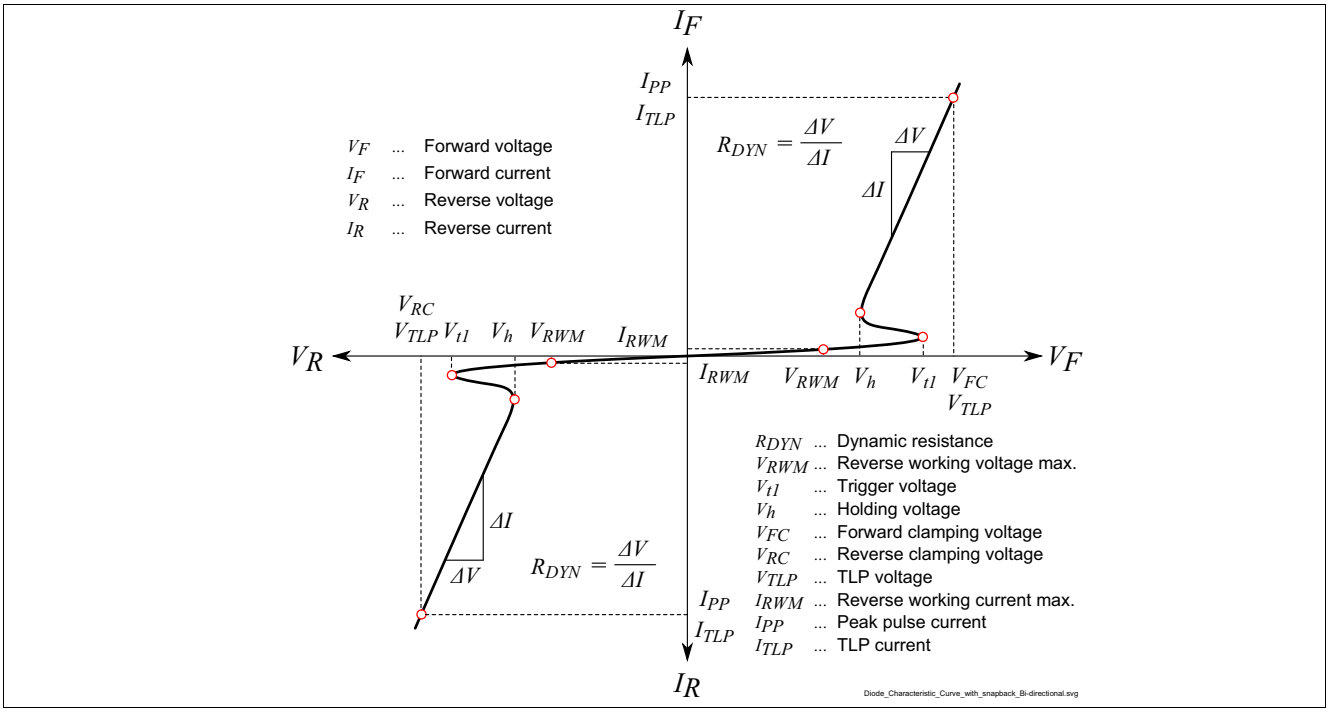


**Figure 2-1 Definitions of electrical characteristics**

**Table 2-2 DC Characteristics** at $T_A$ = 25 °C, unless otherwise specified[1)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Reverse working voltage | $V_{RWM}$ | - | - | 5.5 | V | |
| Reverse current | $I_R$ | - | - | 50 | nA | $V_R$ = 5.5 V |
| Trigger voltage | $V_{t1}$ | 6.1 | - | - | V | |
| Holding voltage | $V_h$ | 6.1 | 8 | 9.5 | V | $I_R$ = 10 mA |

1) Device is electrically symmetrical

**Table 2-3 AC Characteristics** at $T_A$ = 25 °C, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Line capacitance | $C_L$ | - | 12 | 20 | pF | $V_R$ = 0 V, $f$ = 1 MHz |

**Table 2-4 ESD and Surge Characteristics** at $T_A$ = 25 °C, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clamping voltage[1)] Pin 1 to GND | $V_{CL}$ | - | 8 | - | V | $I_{TLP}$ = 16 A |
| | | - | 10.8 | - | | $I_{TLP}$ = 30 A |
| Clamping voltage[1)] GND to Pin1 | | | 8.5 | | | $I_{TLP}$ = 16 A |
| | | | 12.5 | | | $I_{TLP}$ = 30 A |
| Clamping voltage[2)] | | - | 7.5 | - | | $I_{PP}$ = 1 A, $t_p$ = 8/20 µs |
| | | - | 9.6 | - | | $I_{PP}$ = 6 A, $t_p$ = 8/20 µs |
| Dynamic resistance[1)] | $R_{DYN}$ | - | 0.13 | - | Ω | Pin 1 to GND |
| | | | 0.16 | | | GND to Pin 1 |

1) ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitive Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 0.6 ns, $I_{TLP}$ and $V_{TLP}$ averaging window: $t_1$ = 30 ns to $t_2$ = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between $I_{TLP1}$ = 10 A and $I_{TLP2}$ = 40 A. Please refer to Application Note AN210[1].

2) $I_{PP}$ according to IEC61000-4-5 ($t_p$ = 8/20 µs)

# 3 Typical Characteristics at $T_A$ = 25 °C, unless otherwise specified

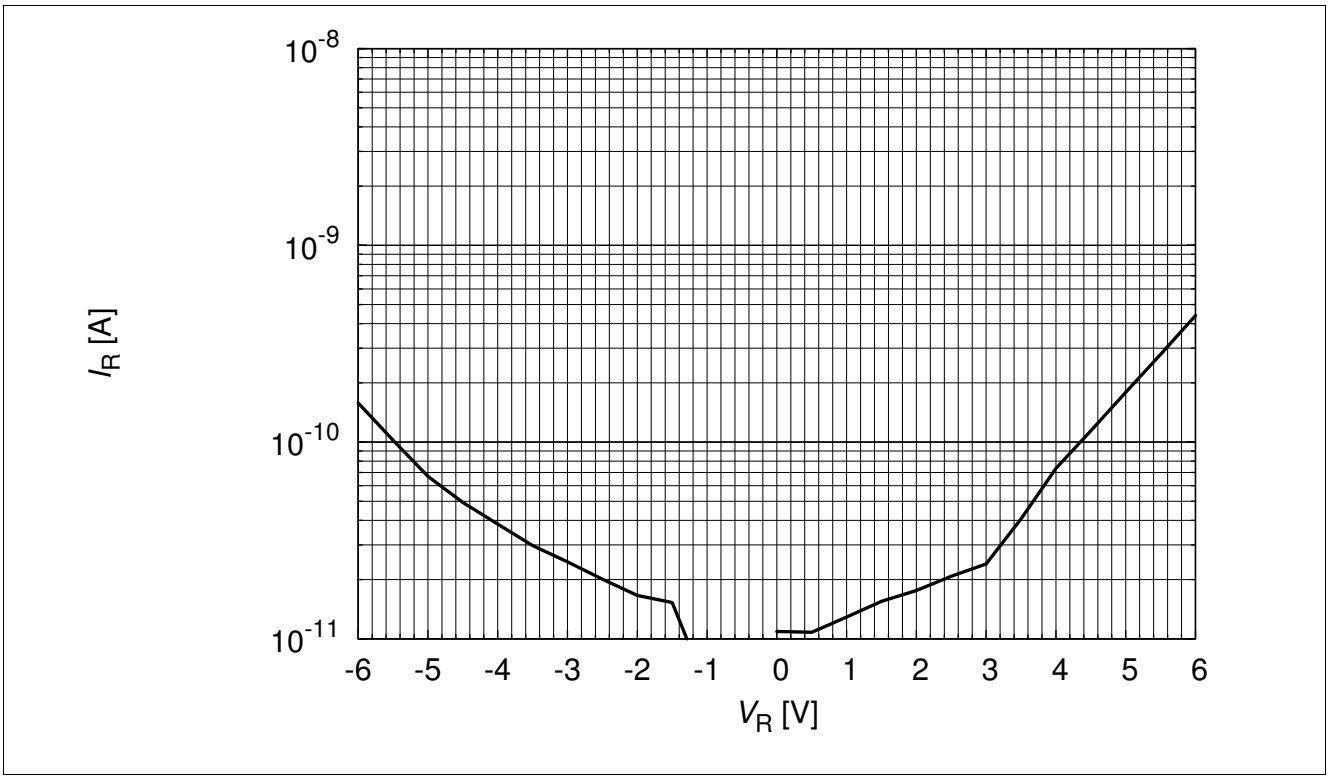


**Figure 3-1 Reverse current: $I_R = f(V_R)$**

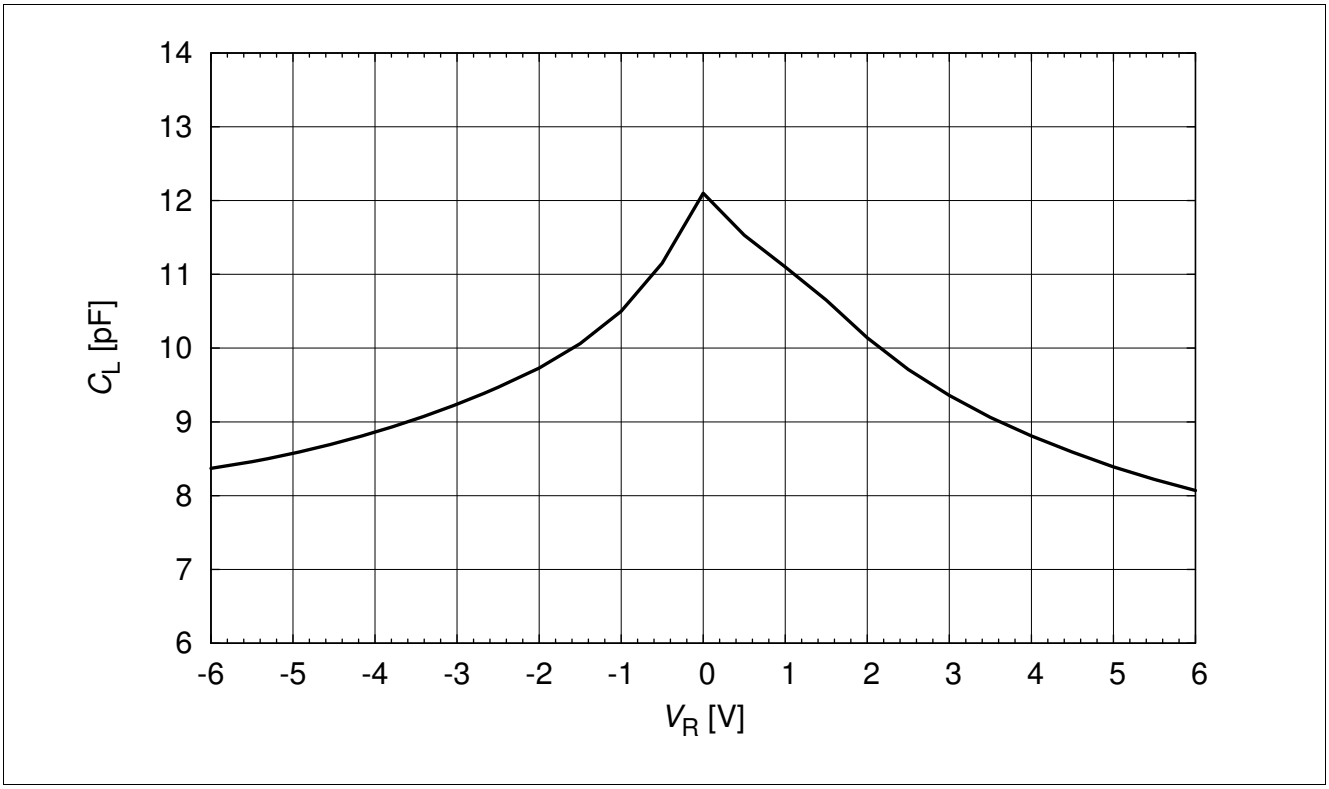


**Figure 3-2 Line capacitance: $C_L = f(V_R)$, $f$ = 1MHz**

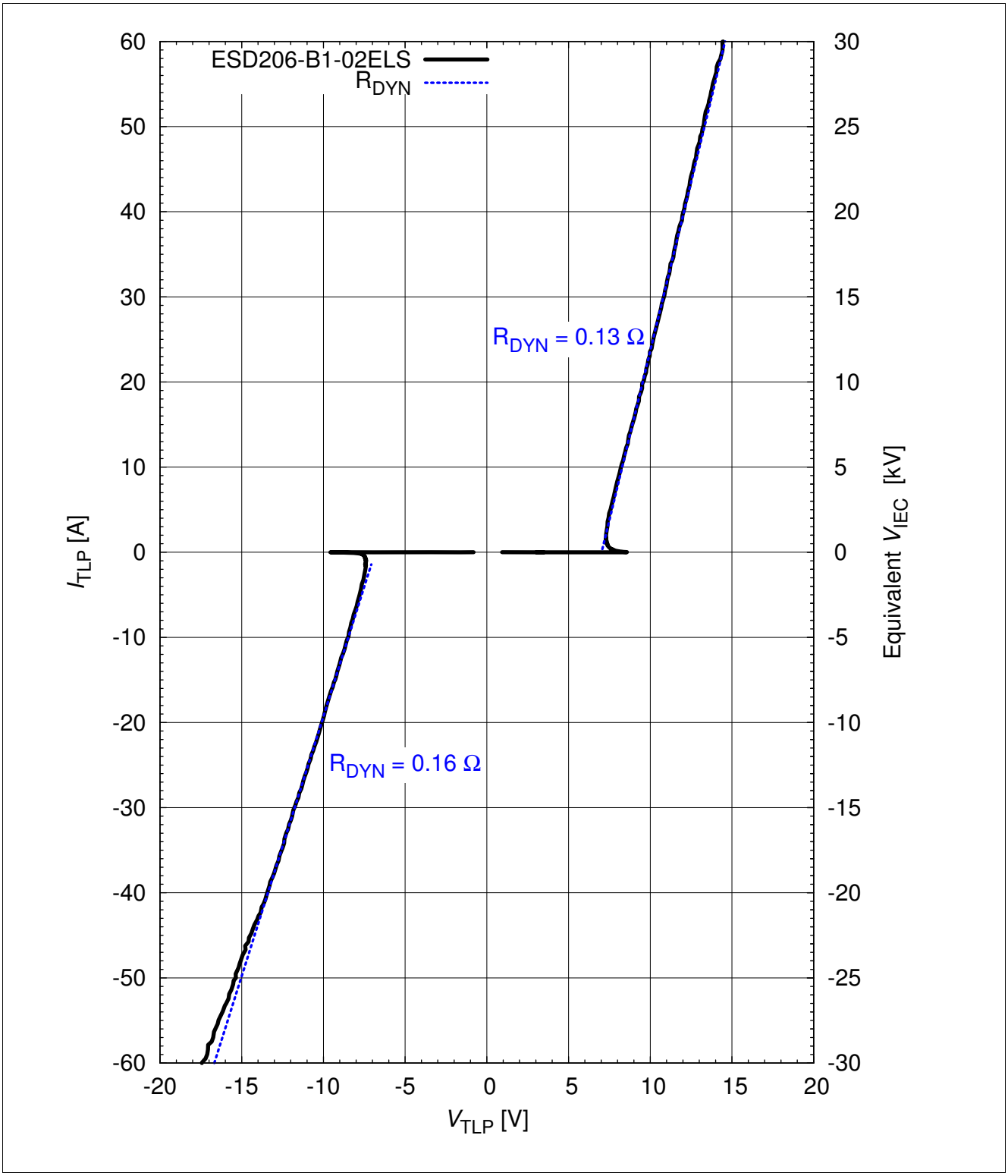


**Figure 3-3 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 0.6 ns, $I_{TLP}$ and $V_{TLP}$ averaging window: $t_1$ = ns to $t_2$ = 60 ns, extraction of dynamic resistance using squares fit to TLP characteristics between $I_{TLP1}$ = 10 A and $I_{TLP2}$ = 40 A. Please refer to Application Note AN210 [1]**

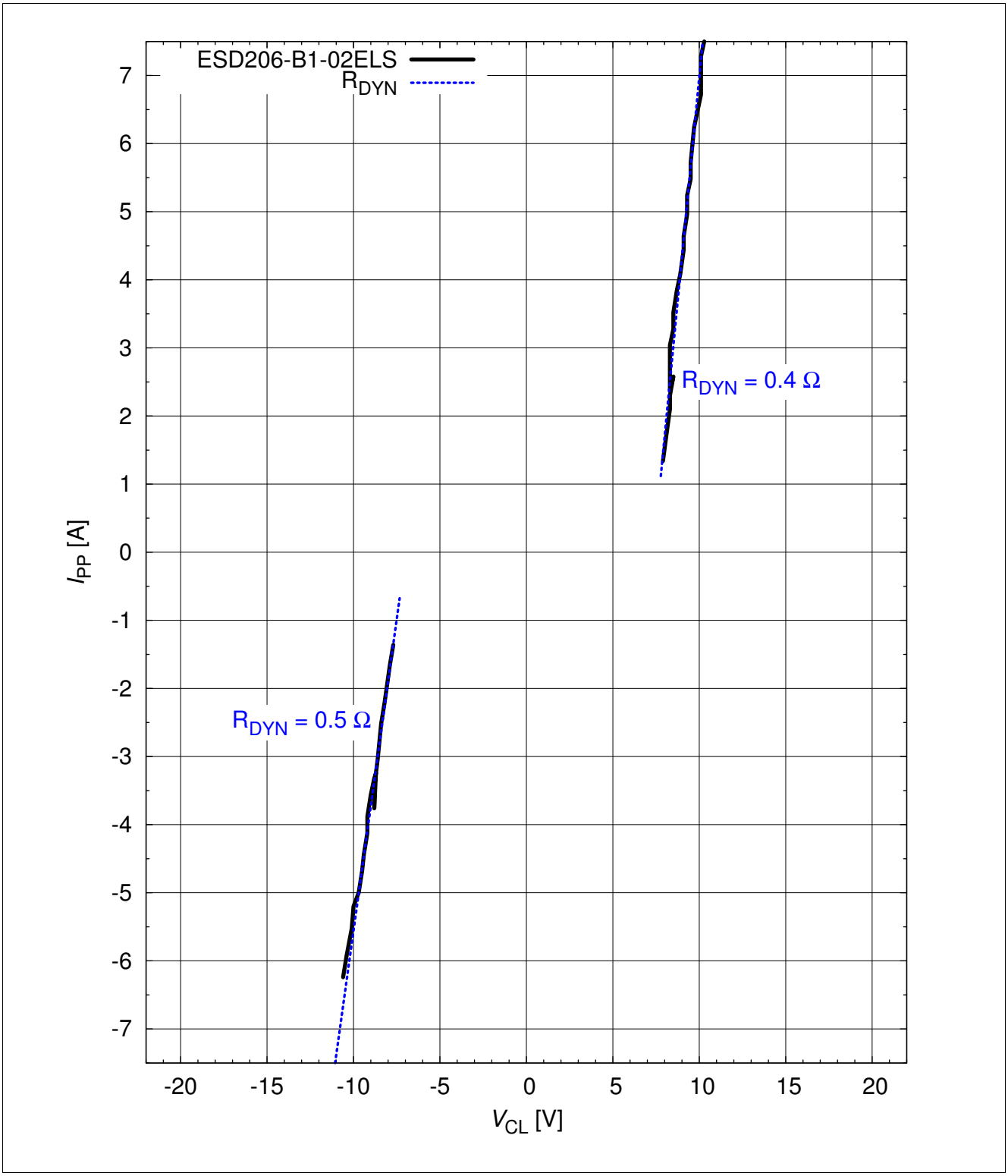


**Figure 3-4 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$**

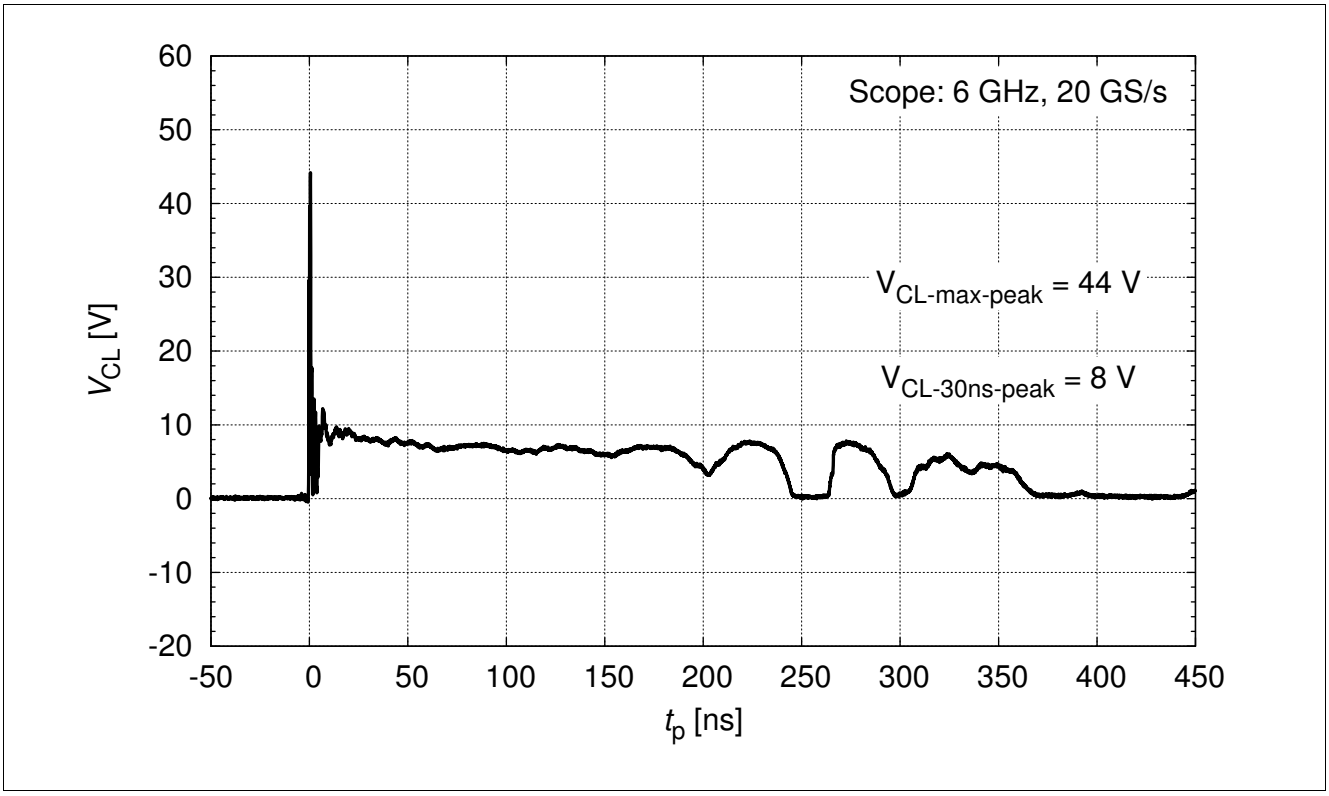


**Figure 3-5 IEC61000-4-2 : $V_{CL}$ = $f(t)$, 8 kV positive pulse from pin 1 to pin 2**

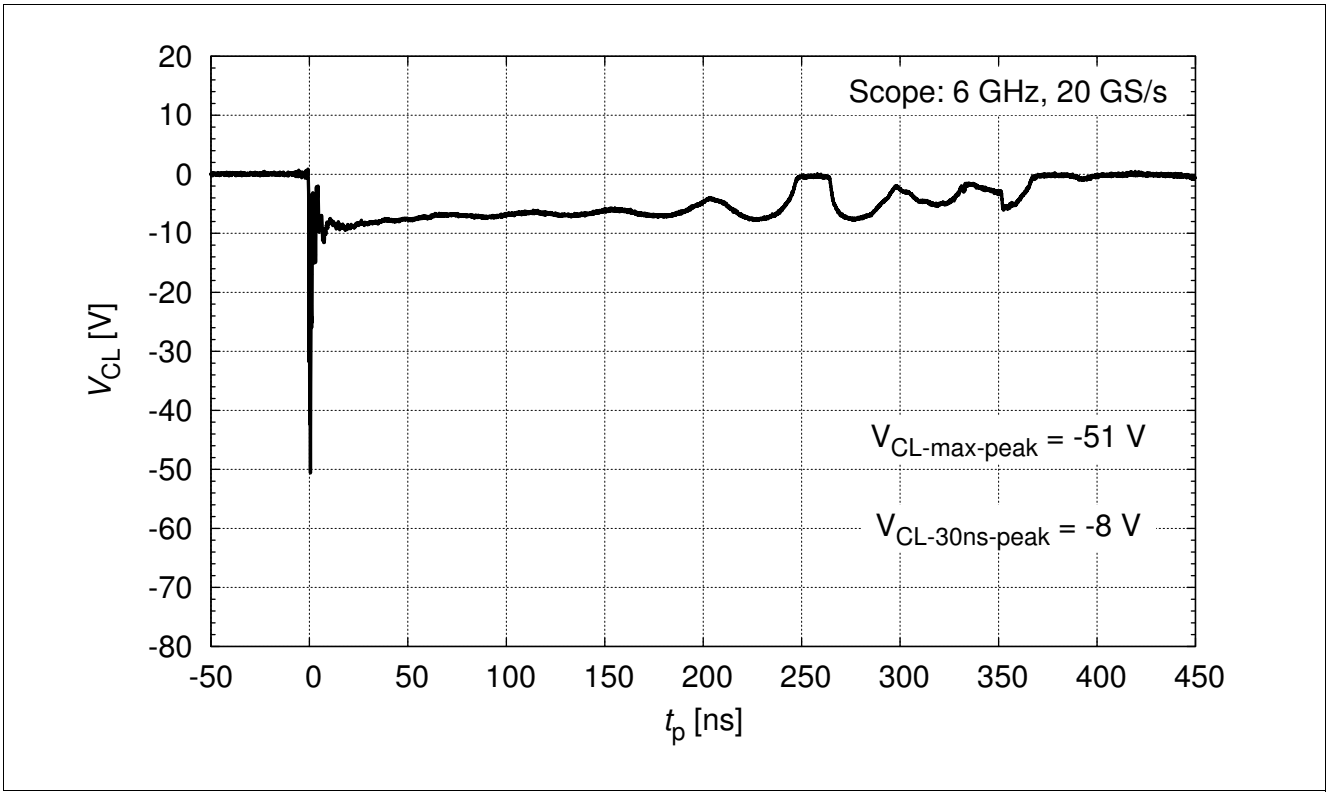


**Figure 3-6 IEC61000-4-2 : $V_{CL}$ = $f(t)$, 8 kV negative pulse from pin 1 to pin 2**

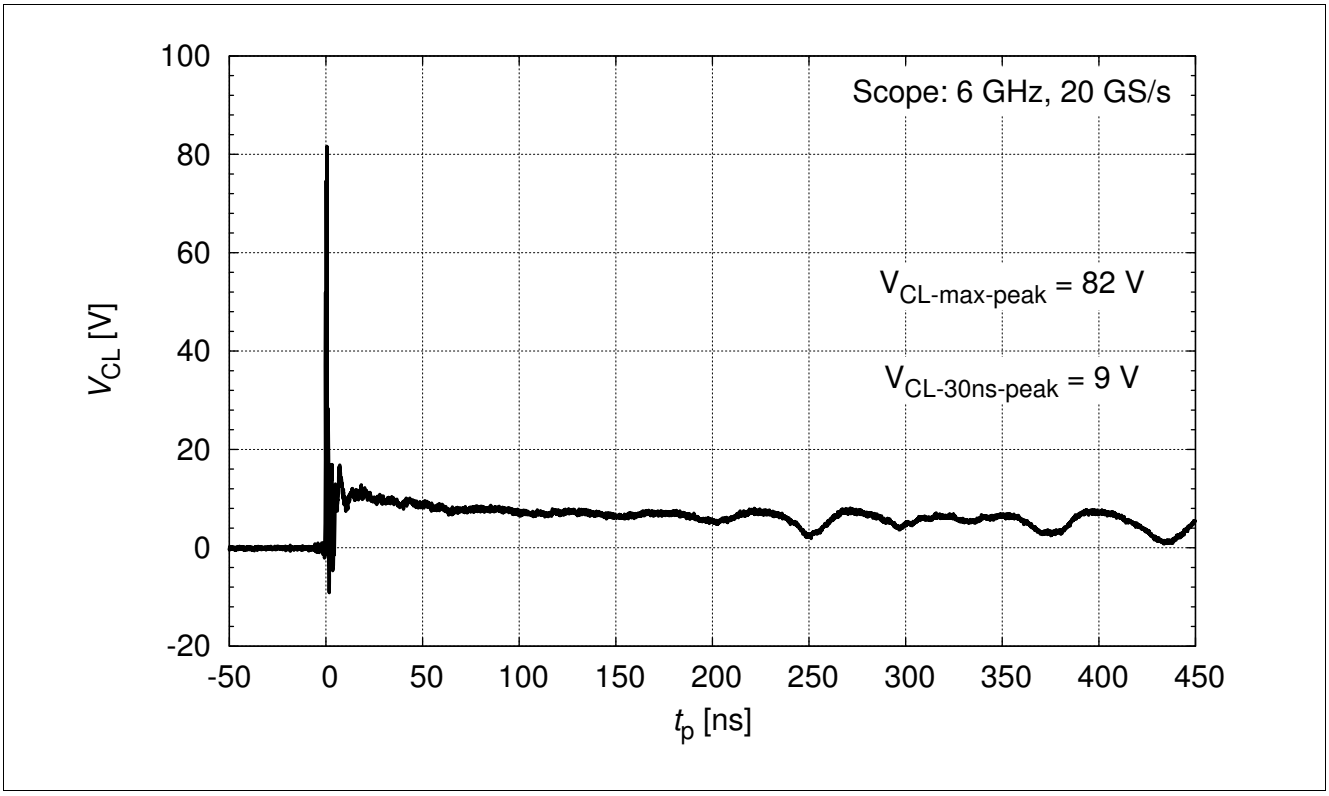


**Figure 3-7 IEC61000-4-2 : $V_{CL}$ = $f(t)$, 15 kV positive pulse from pin 1 to pin 2**

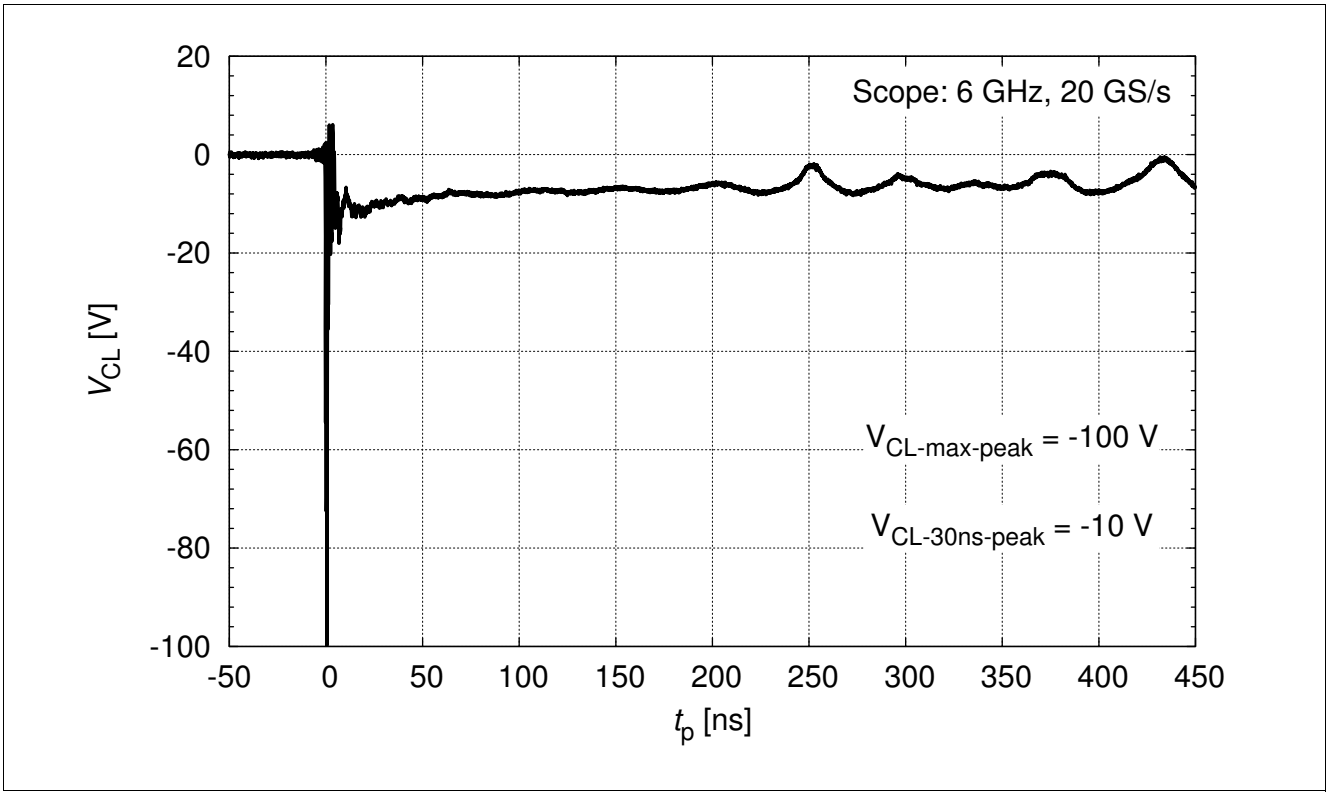


**Figure 3-8 IEC61000-4-2 : $V_{CL}$ = $f(t)$, 15 kV negative pulse from pin 1 to pin 2**

# 4 Package Information

## 4.1 TSSLP-2-3

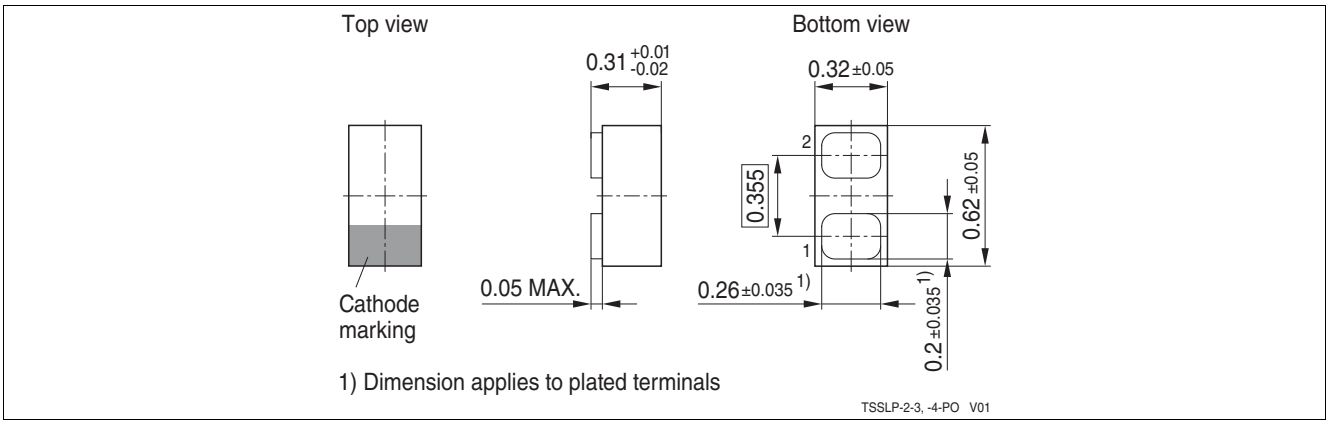


**Figure 4-1 TSSLP-2-3: Package outline (dimension in mm)**

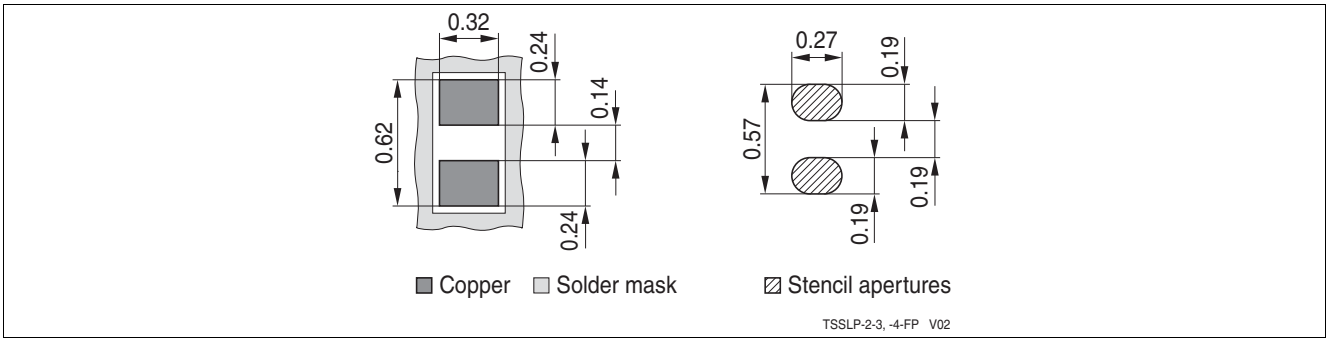


**Figure 4-2 TSSLP-2-3: Footprint (dimension in mm)**

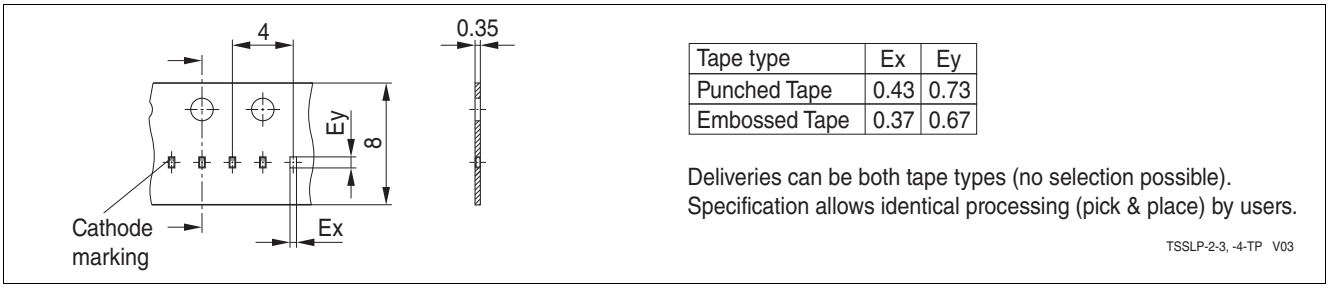


**Figure 4-3 TSSLP-2-3: Tape and reel (dimension in mm)**

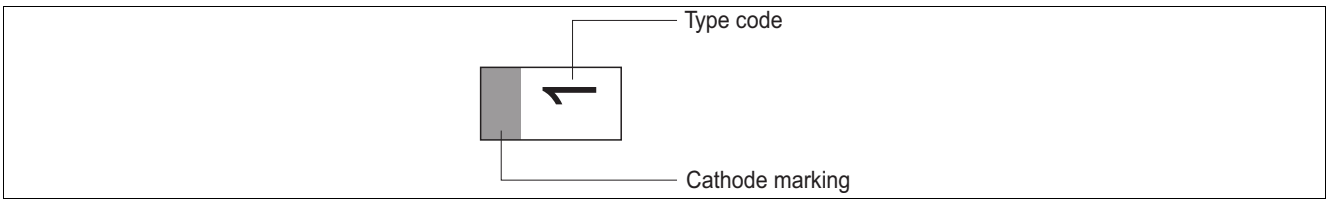


**Figure 4-4 TSSLP-2-3: Marking example**

## 4.2 TSLP-2-19

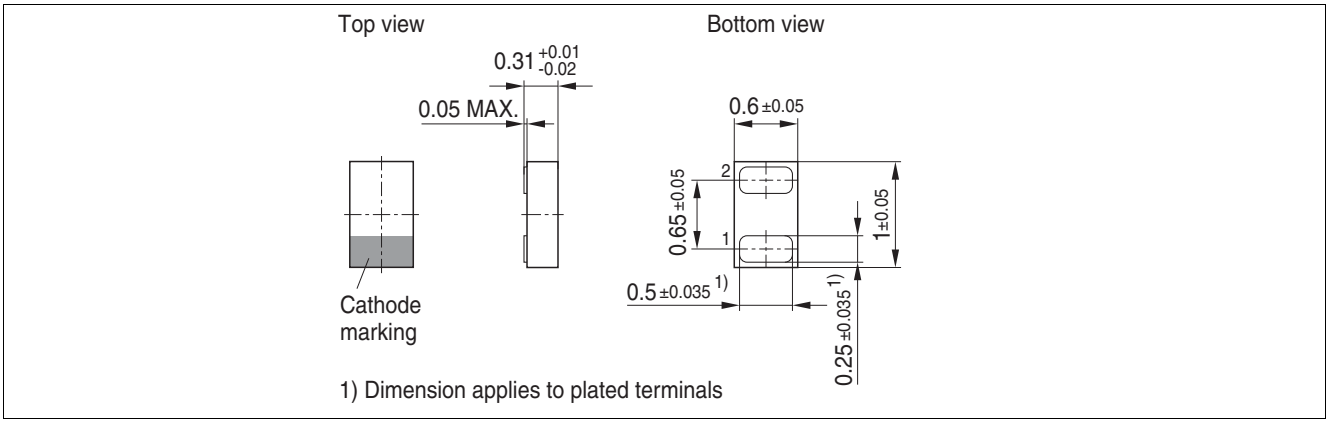


**Figure 4-5 TSLP-2-19: Package outline (dimension in mm)**

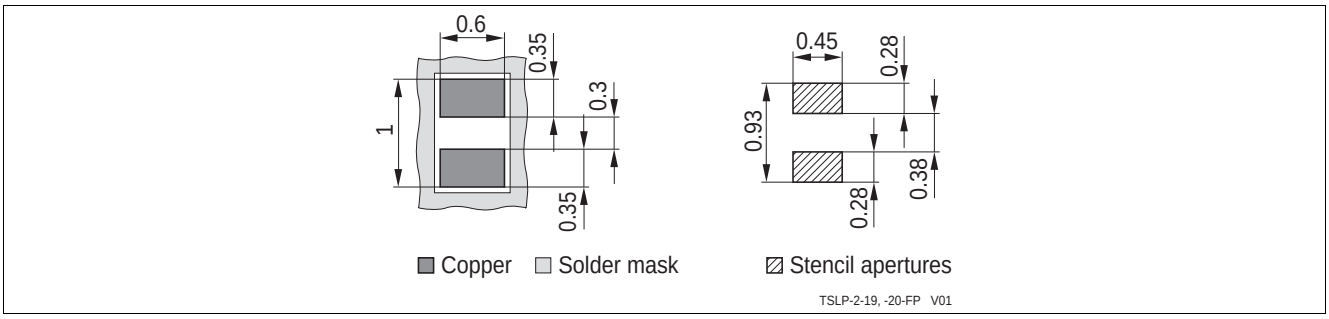


**Figure 4-6 TSLP-2-19: Footprint (dimension in mm)**

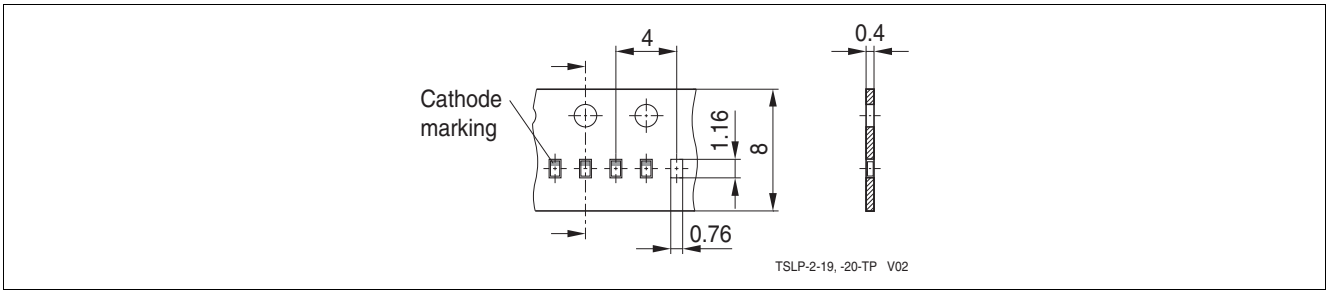


**Figure 4-7 TSLP-2-19: Tape and reel (dimension in mm)**

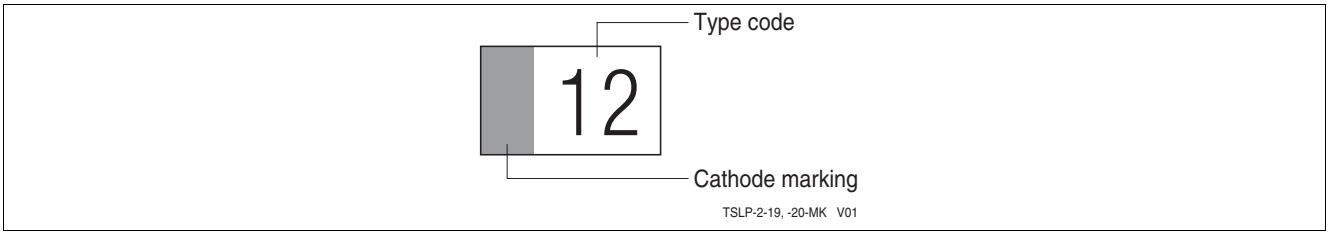


**Figure 4-8 TSLP-2-19: Marking example**

# References

[1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

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Published by Infineon Technologies AG

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