AT17F16

FPGA Configuration Flash Memory

DATASHEET

Features

- Programmable 16,777,216 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
- 3.3V Output Capability
- 5.0V Tolerant I/O Pins
- Program Support using the Atmel ATDH2200E System, ATDH2225 ISP Cable, or Third-party Programmers
- In-System Programmable (ISP) via 2-wire Bus
- Simple Interface to SRAM FPGAs
- Compatible with Atmel AT40K and AT94K Devices, Altera® FLEX®, APEX™ Devices, Lucent® ORCA® FPGAs, Xilinx® XC3000, XC4000, XC5200, Spartan®, Virtex® FPGAs, Motorola® MPA1000 FPGAs
- Cascadable Read-back to Support Additional Configurations or Higher-density Arrays
- Low-power CMOS FLASH Process
- Available in 8-pad LAP (Pin-compatible with 8-lead SOIC/VOIC Footprint Packages) and 20-lead PLCC Packages
- Emulation of the Atmel AT24C Serial EEPROMs
- Low-power Standby Mode
- Single Device Capable of Holding Four Bitstream Files Allowing Simple System Reconfiguration
- Fast Serial Download Speeds up to 33MHz
- Endurance: 10,000 Write Cycles Typical
- Green (Pb/Halide-free/RoHS Compliant) Packages

Description

The Atmel® AT17F16 In-System Programmable Configuration PROMs (Configurators) provide an easy-to-use, cost-effective configuration memory solutions for FPGAs. The AT17F16 is packaged in the 8-pad LAP and 20-lead PLCC packages (Table 1). The AT17F16 uses a simple serial-access procedure to configure one or more FPGA devices.

The AT17F16 can be programmed with industry-standard programmers, the Atmel ATDH2200E Programming Kit, or the Atmel ATDH2225 ISP Cable.

Table 1. AT17F16 Packages

Package	AT17F16
8-pad LAP	Yes
20-lead PLCC	Yes

1. Pin Configurations

Table 1-1. Pin Descriptions

Pin	Description
DATA(1)	**Three-state DATA output for FPGA Configuration**. Open-collector bi-directional pin for configuration programming.
CLK(1)	**Clock Input.** Used to increment the internal address and bit counter for reading and programming.
PAGE_EN(2)	**Enable Page Download Mode Input.** When PAGE_EN is high, the configuration download address space is partitioned into four equal pages. This gives users the ability to easily store and retrieve multiple configuration bitstreams from a single configuration device. This input works in conjunction with the PAGESEL inputs. PAGE_EN must be remain low if paging is not desired. When SER_EN is Low (ISP mode) this pin has no effect.
PAGESEL[1:0](2)	**Page Select Inputs.** Used to determine which of the four memory pages are targeted during a serial configuration download. The address space for each of the pages is shown in Table 1-2. When $\overline{\text{SER\_EN}}$ is Low (ISP mode) these pins have no effect.
$\overline{\text{RESET}}$/OE(1)	**Output Enable (Active High) and RESET (Active Low) when $\overline{\text{SER\_EN}}$ is High**. A Low level on $\overline{\text{RESET}}$/$\overline{\text{OE}}$ resets both the address and bit counters. A High level (with $\overline{\text{CE}}$ Low) enables the data output driver.
$\overline{\text{CE}}$(1)	**Chip Enable Input (Active Low)**. A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the 2-wire Serial Programming mode ($\overline{\text{SER\_EN}}$ Low).
GND	**Ground**. A 0.2µF decoupling capacitor between V_{CC} and GND is recommended.
$\overline{\text{CEO}}$	**Chip Enable Output (when $\overline{\text{SER\_EN}}$ is High).** This output goes Low when the internal address counter has reached its maximum value. If the PAGE_EN input is set High, the maximum value is the highest address in the selected partition. The PAGESEL[1:0] inputs are used to make the four partition selections. If the PAGE_EN input is set Low, the device is not partitioned and the address maximum value is the highest address in the device (Table 1-2). In a daisy chain of AT17F Series devices, the $\overline{\text{CEO}}$ pin of one device must be connected to the $\overline{\text{CE}}$ input of the next device in the chain. It will stay Low as long as $\overline{\text{CE}}$ is Low and OE is High. It will then follow $\overline{\text{CE}}$ until OE goes Low; thereafter, $\overline{\text{CEO}}$ will stay High until the entire EEPROM is read again.
A2(1)	**Device Selection Input, (when $\overline{\text{SER\_EN}}$ Low).** The input is used to enable (or chip select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low). Refer to the AT17F(A) Programming Specification available at www.atmel.com for additional details.
READY	**Open Collector Reset State Indicator**. Driven Low during power-up reset, released when power-up is complete. (Recommend 4.7kΩ pull-up on this pin if used).
$\overline{\text{SER\_EN}}$(1)	**Serial Enable Input.** Must remain High during FPGA configuration operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the 2-Wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER\_EN}}$ should be tied to V_{CC}.
V_{CC}	**Device Power Supply.** +3.3V (±10%)

Notes:
1. Internal 20KΩ pull-up resistor
2. Internal 30KΩ pull-up resistor

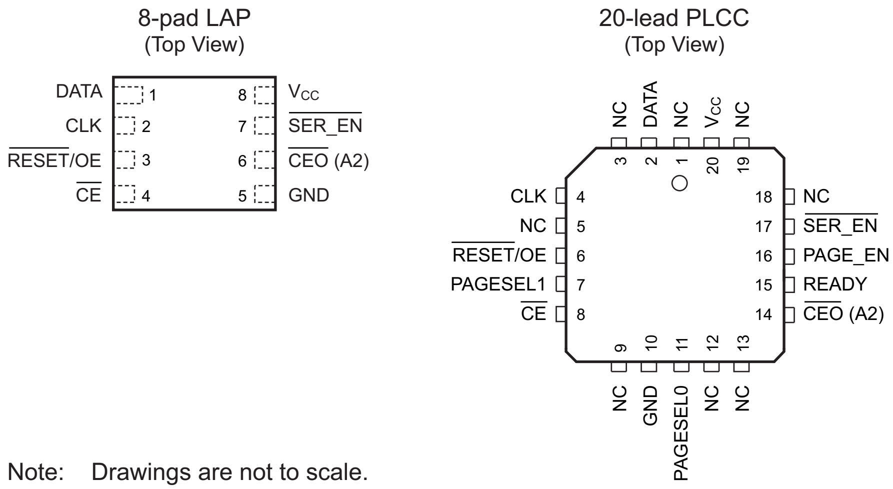
Table 1-2. Address Space PAGESEL[1:0]

Paging Decodes	AT17F16 (16Mb)
PAGESEL = 00, PAGE_EN = 1	00000 – 3FFFFh
PAGESEL = 01, PAGE_EN = 1	40000 – 7FFFFh
PAGESEL = 10, PAGE_EN = 1	80000 – BFFFFh
PAGESEL = 11, PAGE_EN = 1	C0000 – FFFFFh
PAGESEL = XX, PAGE_EN = 0	00000 – FFFFFh

Table 1-3. Pin Configurations

Name	I/O	8-pad LAP	20-lead PLCC
DATA	I/O	1	2
CLK	I	2	4
PAGE_EN	I	—	16
PAGESEL0	I	—	11
PAGESEL1	I	—	7
$\overline{\text{RESET}}$/OE	I	3	6
$\overline{\text{CE}}$	I	4	8
GND	—	5	10
$\overline{\text{CEO}}$	O	6	14
A2	I	6	14
READY	O	–	15
$\overline{\text{SER\_EN}}$	I	7	17
V_{CC}	—	8	20

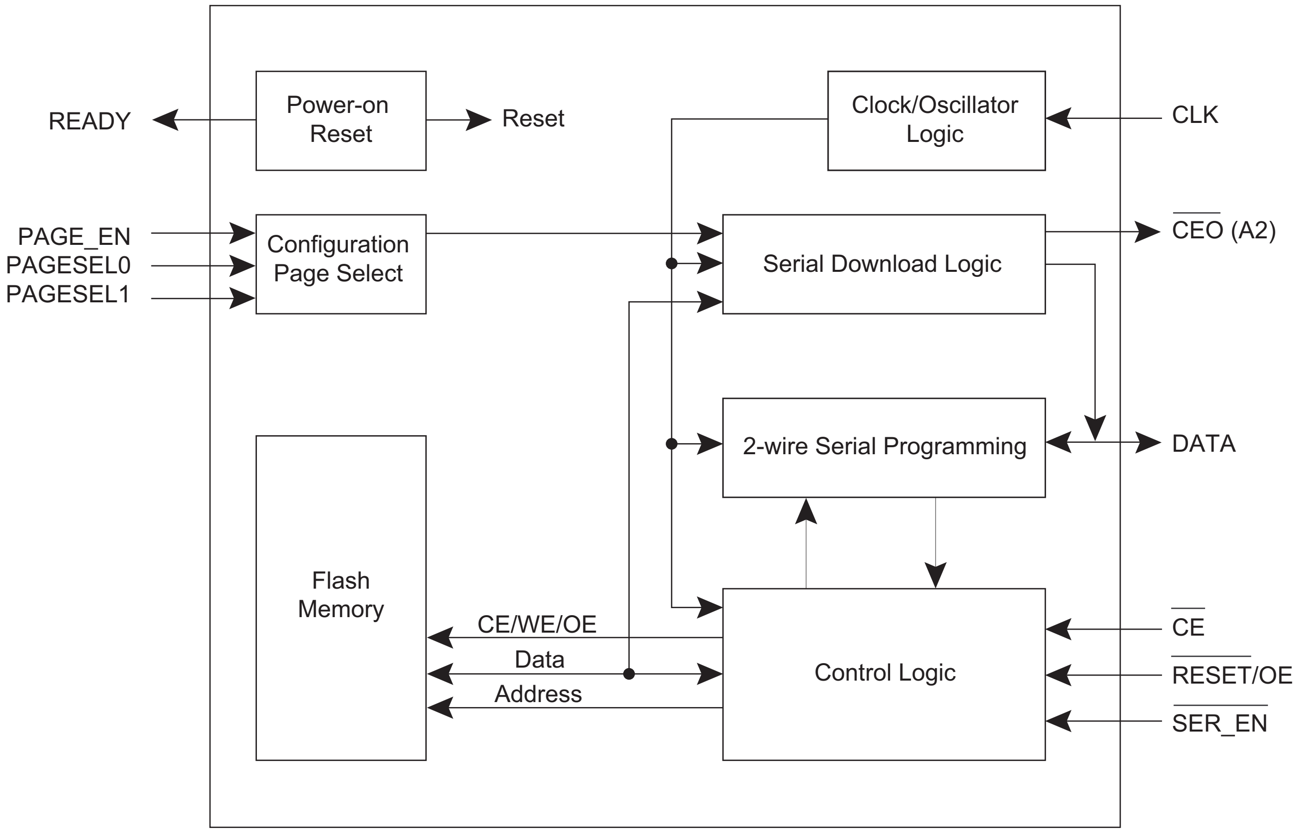
Figure 1-1. Pinouts



Note: Drawings are not to scale.

2. Block Diagram

Figure 2-1. Block Diagram



3. Device Description

The control signals for the configuration memory device ($\overline{\text{CE}}$, $\overline{\text{RESET}}$/OE and CLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration device without requiring an external intelligent controller.

The $\overline{\text{RESET}}$/OE and $\overline{\text{CE}}$ pins control the tri-state buffer on the DATA output pin and enable the address counter. When $\overline{\text{RESET}}$/OE is driven Low, the configuration device resets its address counter and tri-states its DATA pin. The $\overline{\text{CE}}$ pin also controls the output of the AT17F16. If $\overline{\text{CE}}$ is held High after the $\overline{\text{RESET}}$/OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When OE is subsequently driven High, the counter and the DATA output pin are enabled. When $\overline{\text{RESET}}$/OE is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of $\overline{\text{CE}}$.

When the configurator has driven out all of its data and $\overline{\text{CEO}}$ is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

4. FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17F16 Serial Configuration PROM has been designed for compatibility with the Master Serial mode.

This document discusses the Atmel AT40K, AT40KAL and AT94KAL applications as well as Xilinx applications.

5. Control of Configuration

Most connections between the FPGA device and the AT17F16 Serial Configurator PROM are simple and self-explanatory.

- The DATA output of the AT17F16 Configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17F16 Configurator.
- The $\overline{\text{CEO}}$ output of any AT17F16 Configurator drives the $\overline{\text{CE}}$ input of the next Configurator in a cascade chain of configurator devices.
- $\overline{\text{SER\_EN}}$ must be connected to V_{CC} or allowed to float to logic High via the internal pull-up resistor (except during ISP).
- The READY pin is available as an open-collector indicator of the device’s reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.
- PAGE_EN must be held Low if download paging is not desired. The PAGESEL[1:0] inputs must be tied off High or Low. If paging is desired, PAGE_EN must be High and the PAGESEL pins must be set to High or Low such that the desired page is selected, see Table 1-2.

6. Cascading Serial Configuration Devices

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the clock signal to the configurator asserts its $\overline{\text{CEO}}$ output Low and disables its DATA line driver. The second configurator recognizes the Low level on its $\overline{\text{CE}}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the $\overline{\text{RESET}}$/OE on each configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the $\overline{\text{RESET}}$/OE input can be tied to its inactive (High) level.

7. Programming Mode

The programming mode is entered by bringing $\overline{\text{SER\_EN}}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. The AT17F16 is read/write at 3.3V nominal. Refer to the AT17F16(A) Programming Specification available on www.atmel.com for more programming details. The AT17F16 is supported by the Atmel ATDH2200E programming system along with many third party programmers.

8. Standby Mode

The AT17F16 enters a low-power standby mode whenever $\overline{\text{SER\_EN}}$ is High and $\overline{\text{CE}}$ is asserted High. In this mode, the AT17F16 consumes less than 2mA of current at 3.6V. The output remains in a high-impedance state regardless of the state of the OE input.

9. Electrical Specifications

9.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +4.0V
Maximum Soldering Temp. (10 sec. @ 1/16in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100pF)	2000V

*Notice: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

9.2 Operating Conditions

Table 9-1. Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND -40°C to +85°C	2.97	3.63	V

9.3 DC Characteristics

Table 9-2. DC Characteristics

Symbol	Description	Min	Max	Units
V_{IH}	High-level Input Voltage	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5mA)	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3.0mA)		0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.0mA)	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3.0mA)		0.4	V
I_{CCA}	Supply Current, Active Mode (3.6V 33MHz)		40	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)	-10	10	µA
I_{CCS}	Supply Current, Standby Mode		2	mA

9.4 AC Characteristics

Table 9-3. AC Characteristics

Symbol	Description	Min	Typ	Max	Units
T_{OE}(1)	OE to Data Delay			55	ns
T_{CE}(1)	$\overline{\text{CE}}$ to Data Delay			60	ns
T_{CAC}(1)	CLK to Data Delay			30	ns
T_{OH}	Data Hold from $\overline{\text{CE}}$, OE, or CLK	0			ns
T_{DF}(2)	$\overline{\text{CE}}$ or OE to Data Float Delay			15	ns
T_{LC}	CLK Low Time	15			ns
T_{HC}	CLK High Time	15			ns
T_{SCE}	$\overline{\text{CE}}$ Setup Time to CLK (to guarantee proper counting)	25			ns
T_{HCE}	$\overline{\text{CE}}$ Hold Time from CLK (to guarantee proper counting)	0			ns
T_{HOE}	$\overline{\text{RESET}}$/OE Low Time (guarantees counter is reset)	20			ns
F_{MAX}	Maximum Input Clock Frequency $\overline{\text{SEREN}}$ = 0			10	MHz
F_{MAX}	Maximum Input Clock Frequency $\overline{\text{SEREN}}$ = 1			33	MHz
T_{WR}	Write Cycle Time(3)		12		µs
T_{EC}	Erase Cycle Time(3)		33		s

Notes:
1. AC test lead = 50pF.
2. Float delays are measured with 5pF AC loads. Transition is measured ±200mV from steady-state active levels.
3. See the AT17F(A) Programming Specification for procedural information.

Table 9-4. AC Characteristics When Cascading

Symbol	Description	Min	Max	Units
T_{CDF}(2)	CLK to Data Float Delay		50	ns
T_{OCK}(1)	CLK to $\overline{\text{CEO}}$ Delay		55	ns
T_{OCE}(1)	$\overline{\text{CE}}$ to $\overline{\text{CEO}}$ Delay		40	ns
T_{OOE}(1)	$\overline{\text{RESET}}$/OE to $\overline{\text{CEO}}$ Delay		35	ns
F_{MAX}	Maximum Input Clock Frequency		33	MHz

Notes:
1. AC test load = 50pF.
2. Float delays are measured with 5pF AC loads. Transition is measured ± 200mV from steady-state active levels.

Figure 9-1. AC Waveforms

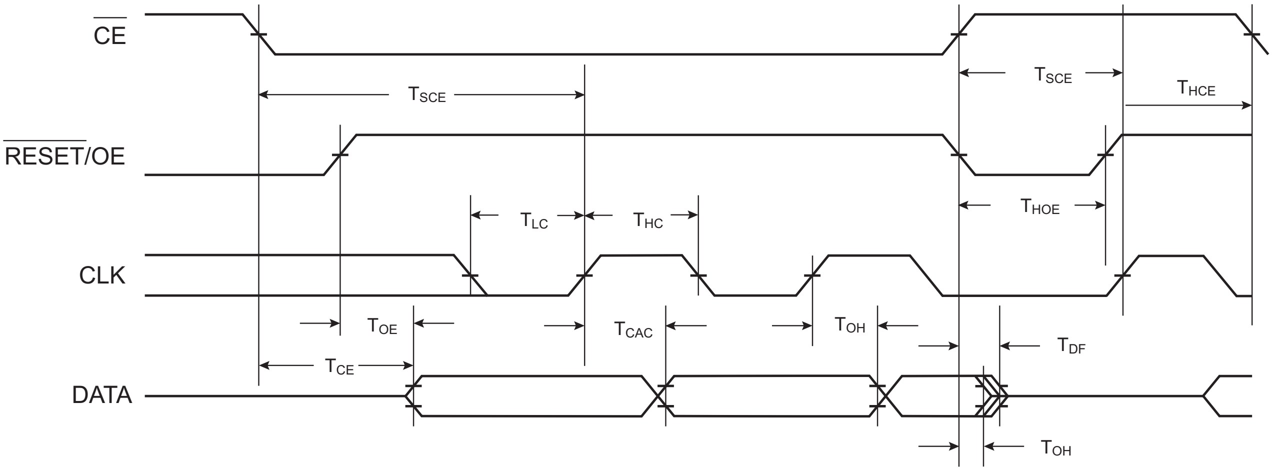
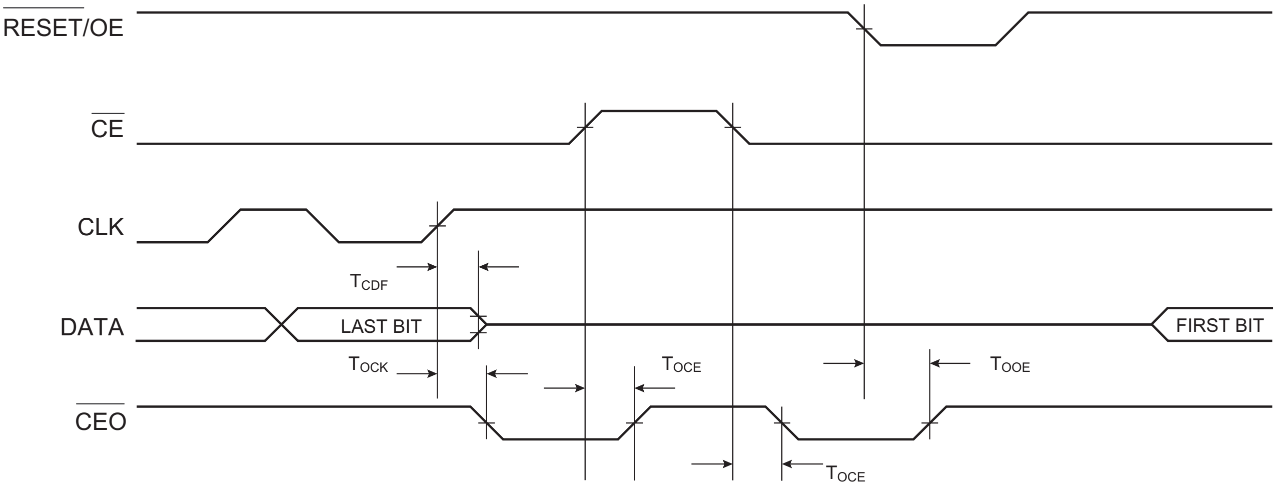
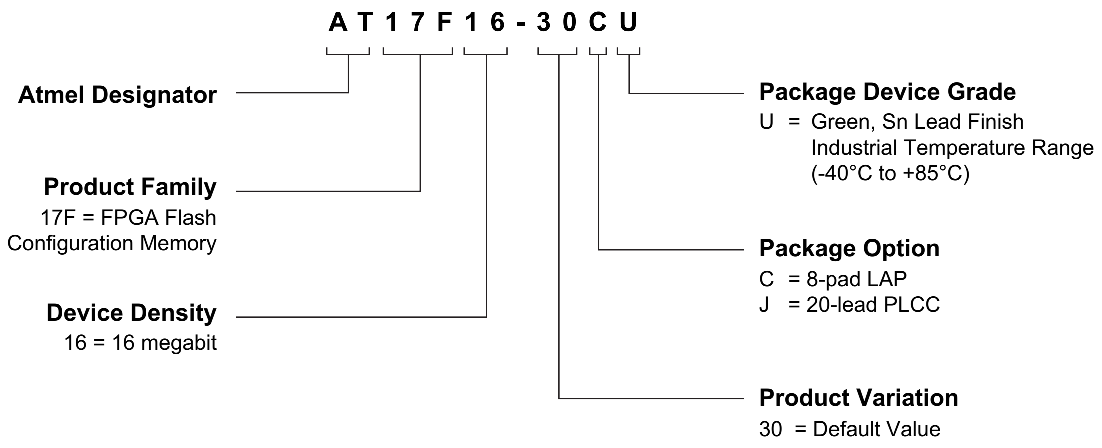


Figure 9-2. AC Waveforms when Cascading



10. Ordering Information

10.1 Ordering Code Detail



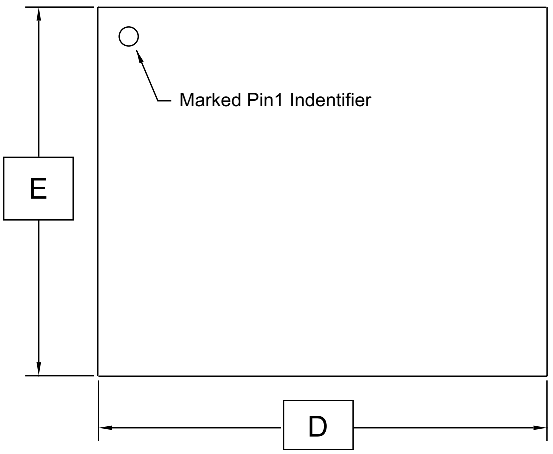
10.2 Ordering Codes

Memory Size	Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
16-Mbit	AT17F16-30CU	Sn (Lead-free/Halogen-free)	8CN4	3.3V	Industrial (-40°C to 85°C)
	AT17F16-30JU		20J		

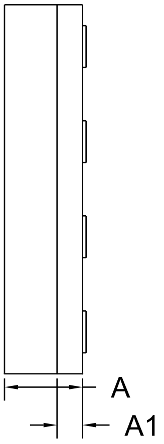
Package Type	
8CN4	8-pad, 6.00mm x 6.00mm x 1.04mm, Leadless Array Package (LAP) Pin-compatible with 8-lead SOIC/VOIC Packages
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)

11. Packaging Information

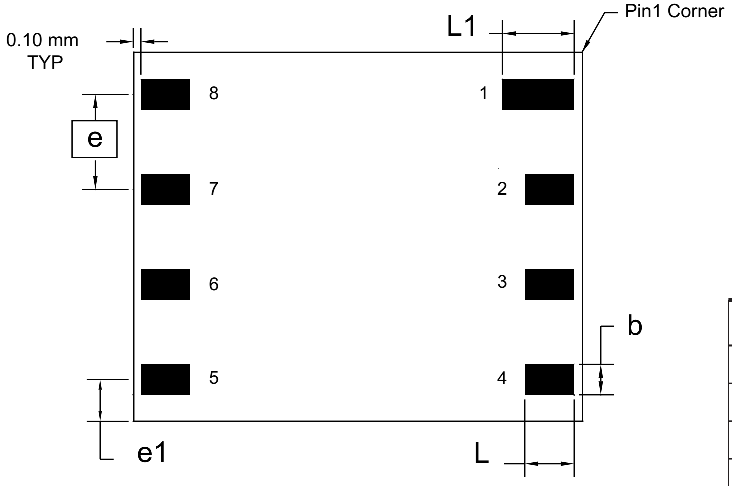
11.1 8CN4 — 8-pad LAP



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

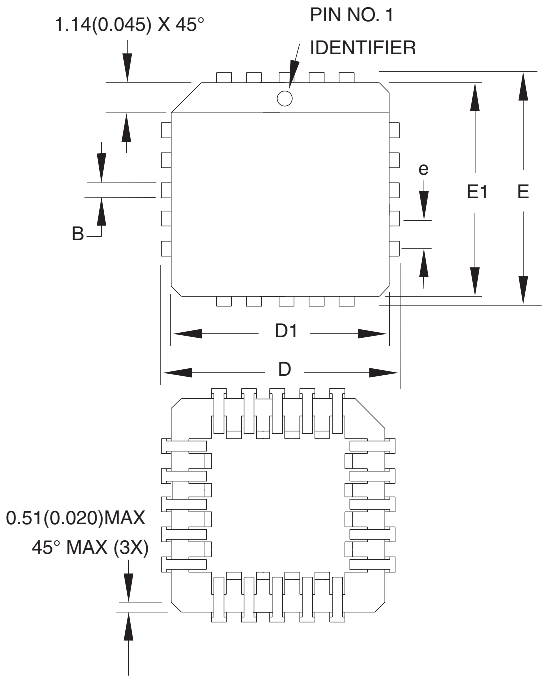
SYMBOL	MIN	TYP	MAX	NOTE
A	0.94	1.04	1.14	
A1	0.30	0.34	0.38	
D	5.89	5.99	6.09	
E	5.89	5.99	6.09	
e		1.27 BSC		
e1		1.10 REF		
L	0.95	1.00	1.05	1
L1	1.25	1.30	1.35	1
b	0.45	0.50	0.55	1

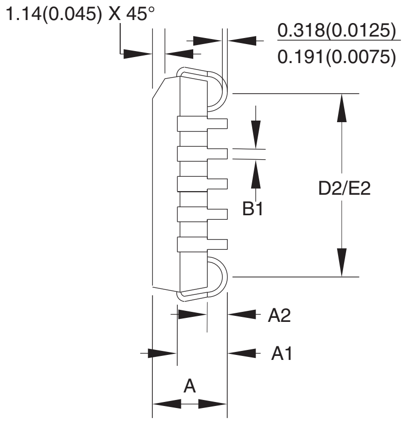
Note: 1. Metal Pad Dimensions.
2. All exposed metal area shall have the following finished platings.
Ni: 0.0005 to 0.015 mm
Au: 0.0005 to 0.001 mm

12/22/14

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8CN4, 8-pad 6x6x1.04mm Body, 1.27mm pitch Leadless Array Package (LAP)	DMH	8CN4	E

11.2 20J — 20-lead PLCC





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102mm) maximum

10/04/01

	TITLE	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

12. Revision History

Doc Rev	Date	Comments
3392G	01/2015	Removed commercial and 32-lead TQFP package options. Updated the 8CN4 package outline drawing, template, Atmel logos, and disclaimer page. Added an ordering code detail.
3392F	02/2008	Removed -30JC, -30JI, -30BJC and -30BJI devices from ordering information.
3392E	08/2007	Removed -30CC and -30CI devices from ordering information. Announced last-time buy for -30JC, -30BJC, -30JI, and -30BJI devices.
3392D	03/2006	Added last-time buy for AT17F16-30CC and AT17F16-30CI.

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