74LVC162245A-Q100

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

Rev. 2 — 11 February 2019 Product data sheet

1. General description

The 74LVC162245A-Q100 is a 16-bit transceivers with non-inverting 3-state bus compatible outputs in both send and receive directions. Two send/receive (nDIR) inputs control direction, and two output enable ($n\overline{OE}$) inputs make cascading easy. The $n\overline{OE}$ inputs control the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices as translators in mixed 3.3 V and 5 V applications.

Both HIGH and LOW output stages include 30 Ω series termination resistors to reduce line noise.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Integrated 30 Ω termination resistors
- High-impedance when V_{CC} = 0 V
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
  - CDM ANSI/ESDA/Jedec JS-002 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC162245ADGG-Q100	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVC162245ADGV-Q100	-40 °C to +125 °C	TSSOP48 [1]	plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm	SOT480-1

[1] Also known as TVSOP48.

4. Functional diagram

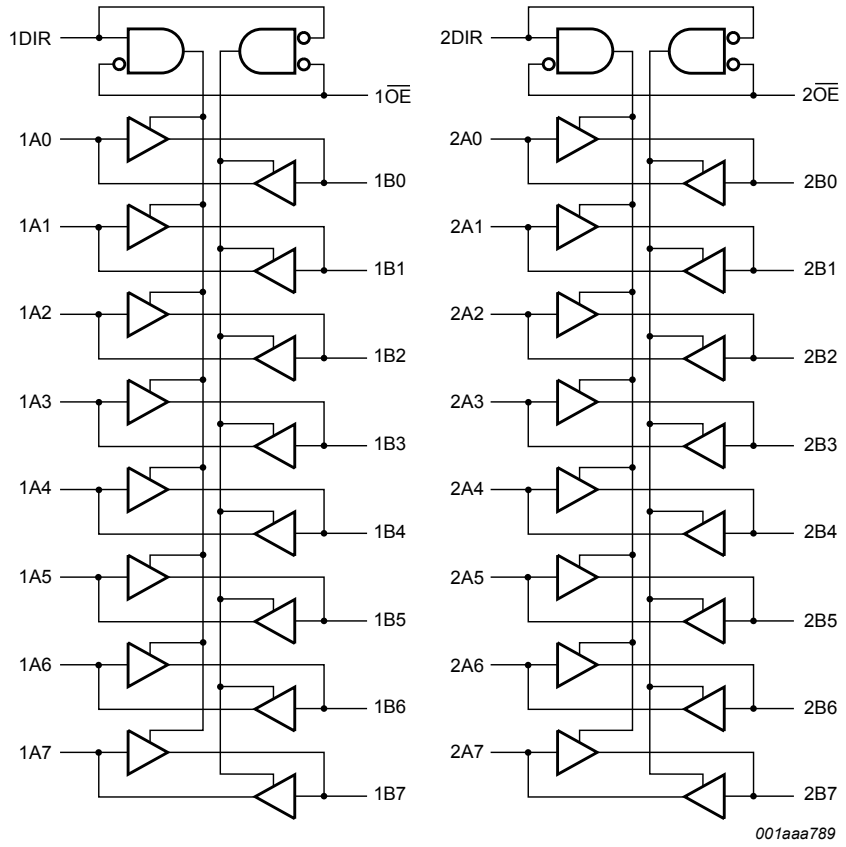


Fig. 1. Logic symbol

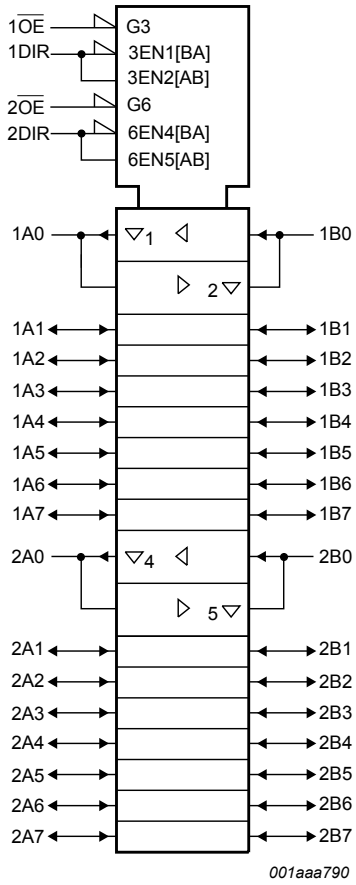


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning

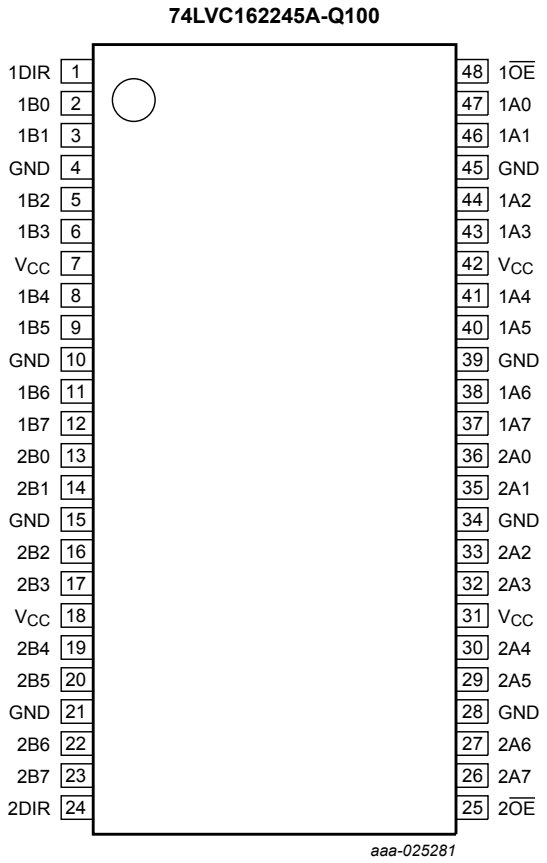


Fig. 3. Pin configuration SOT362-1 (TSSOP48) and SOT480-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage
$1\overline{OE}$, $2\overline{OE}$	48, 25	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output

6. Functional description

Table 3. Function table

Inputs[1]		Outputs	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW	[2]	-0.5	V_{CC} + 0.5	V
		output 3-state	[2]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65V_{CC}	-	-	0.65V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35V_{CC}	-	0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V_{CC} - 0.3	-	V
		I_O = -2 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = -4 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = -6 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 2 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 4 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 6 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 12 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V	-	±0.1	±5	-	±20	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; [2] V_O = 5.5 V or GND; V_{CC} = 3.6 V	-	±0.1	±5	-	±20	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0.0 V	-	±0.1	±10	-	±20	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 3.6 V	-	0.1	20	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF
$C_{I/O}$	input/output capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	10	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.
[2] For I/O ports the parameter I_{OZ} includes the input leakage current.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

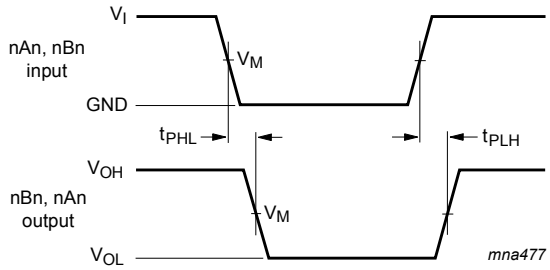
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nAn to nBn; nBn to nAn; see Fig. 4 [2]						
		V_{CC} = 1.2 V	-	12	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.5	6.6	16.0	1.5	18.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.5	7.8	1.0	9.1	ns
		V_{CC} = 2.7 V	1.0	3.5	6.7	1.0	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.9	5.7	1.0	8.5	ns
t_{en}	enable time	$n\overline{OE}$ to nAn, nBn; see Fig. 5 [2]						
		V_{CC} = 1.2 V	-	18	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	7.7	17.2	2.0	19.8	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	4.3	9.4	1.5	10.9	ns
		V_{CC} = 2.7 V	1.5	4.6	8.5	1.5	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.5	7.5	1.0	7.5	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn, nBn; see Fig. 5 [2]						
		V_{CC} = 1.2 V	-	10	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.8	4.6	11.0	2.8	12.7	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.6	6.3	1.0	7.3	ns
		V_{CC} = 2.7 V	1.5	3.4	7.5	1.5	11.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.2	6.5	1.5	8.5	ns
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC} [3]						
		V_{CC} = 1.65 V to 1.95 V	-	10.4	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	14.0	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	17.2	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

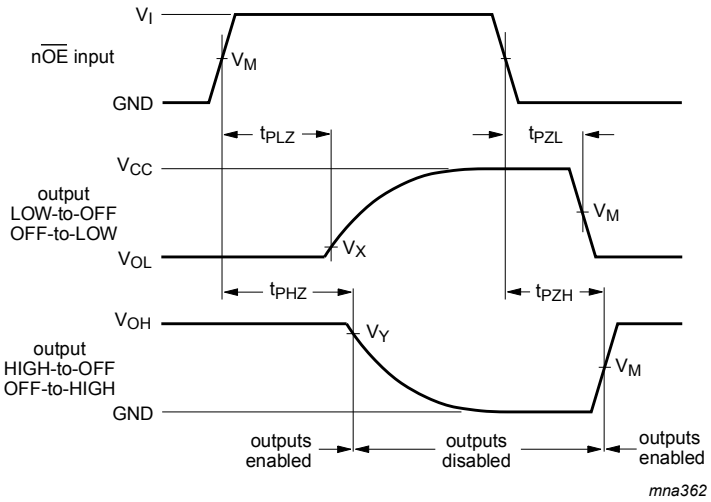
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The input (nAn, nBn) to output (nBn, nAn) propagation delays



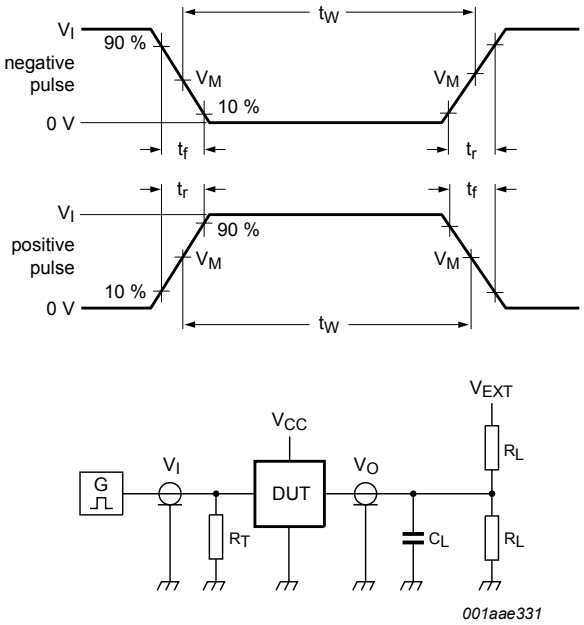
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_M	V_I	V_M	V_X	V_Y
1.2 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
1.65 V to 1.95 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	1.5 V	2.7 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

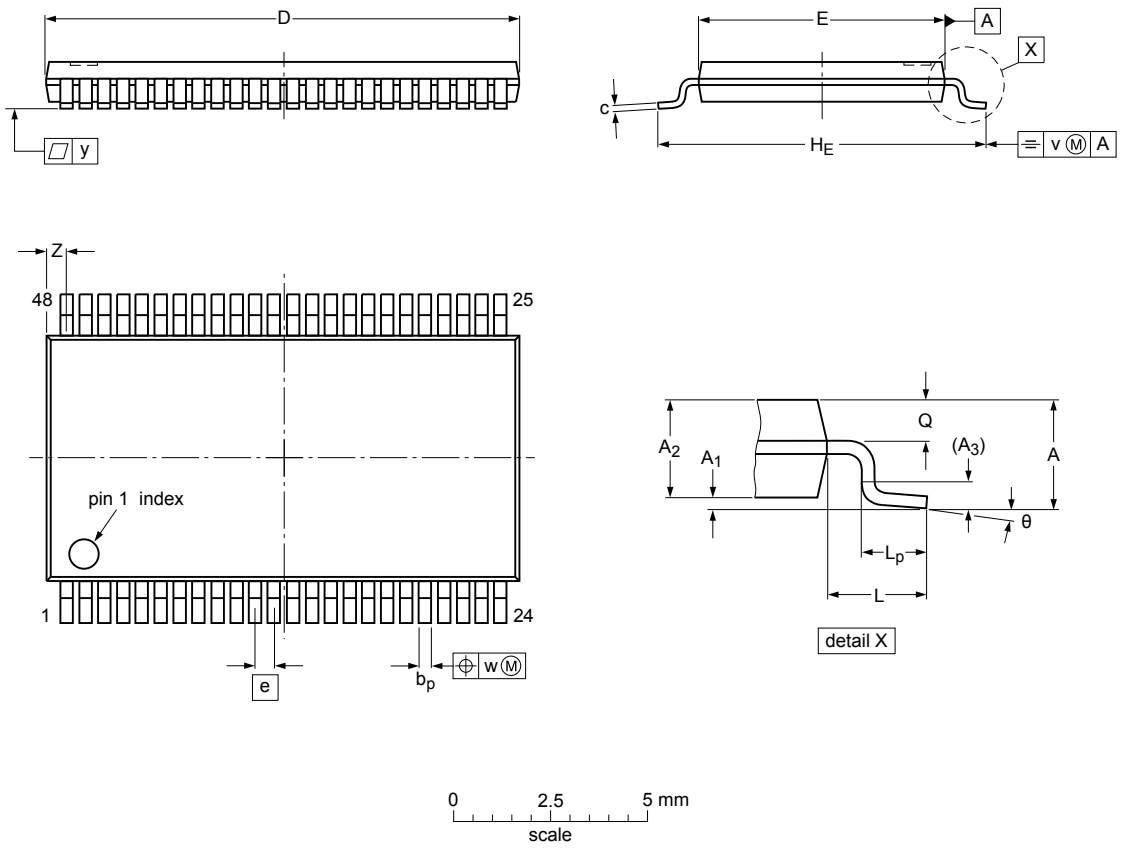
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

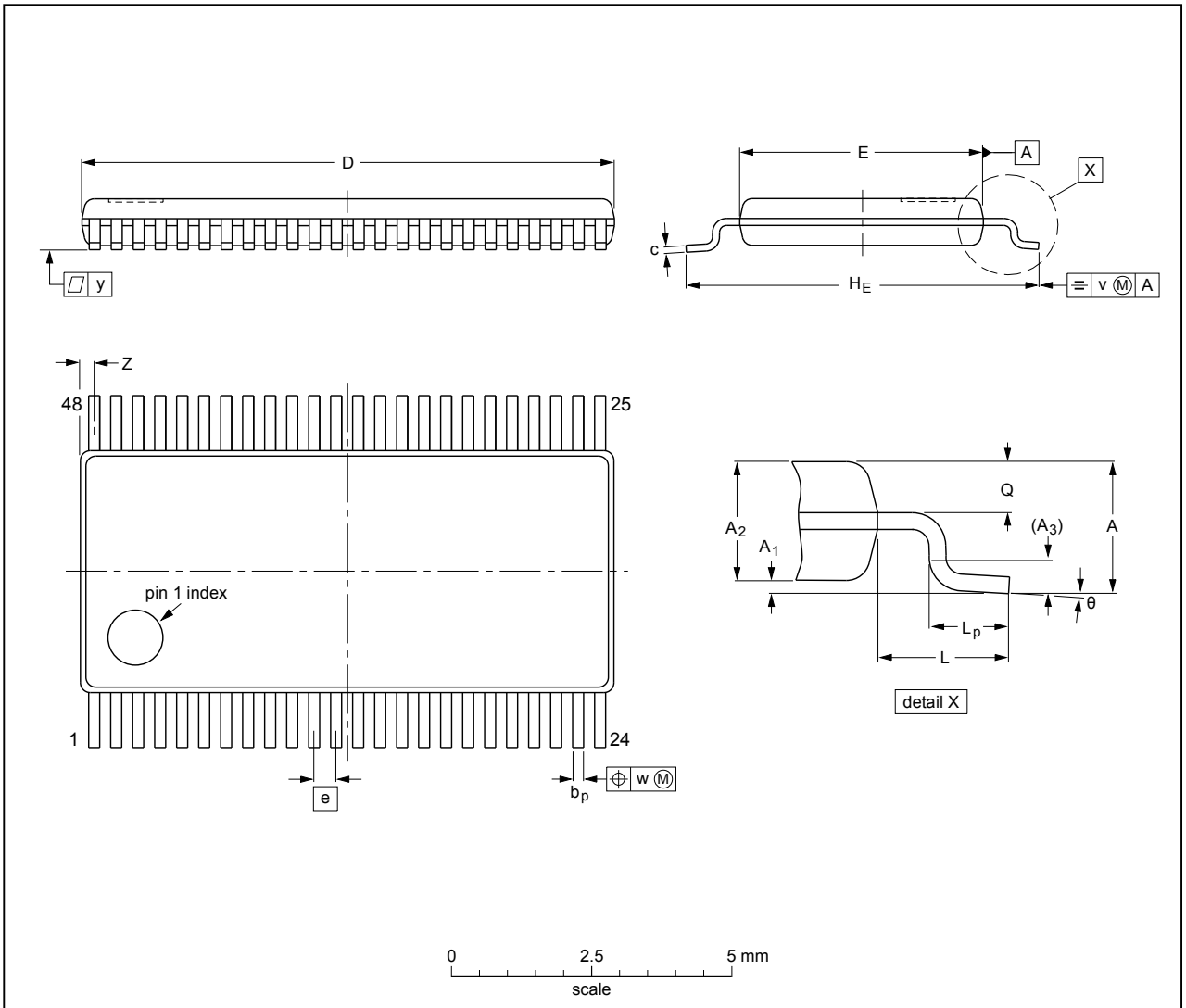
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~03-02-19~~ 13-08-05

Fig. 7. Package outline SOT362-1 (TSSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm **SOT480-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.8 9.6	4.5 4.3	0.4	6.6 6.2	1	0.7 0.5	0.4 0.3	0.2	0.07	0.08	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT480-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 8. Package outline SOT480-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC162245A_Q100 v.2	20190211	Product data sheet	-	74LVC162245A_Q100 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74LVC162245ADGV-Q100 (SOT480-1) added.			
74LVC162245A_Q100 v.1	20161118	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 11 February 2019

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