FEB388_002

FAN9611/FAN9612 400W Interleaved Dual BCM PFC Controller

Evaluation Board User Guide

Featured Fairchild Product: FAN9611, FAN9612

Please contact a local Fairchild Sales representative for an evaluation board.

Table of Contents

The following user guide supports the FAN9611/12 400W evaluation board for interleaved boundary-conduction-mode power-factor-corrected supply. It should be used in conjunction with the FAN9611/12 datasheet as well as the Fairchild application note *AN-6086 Design Considerations for Interleaved Boundary-Conduction Mode PFC using FAN9612*. Although marked FAN9612, the evaluation board can be interchangeably used to evaluate either the FAN9611 (10V turn-on threshold) or FAN9612 controller (12.5V turn-on threshold). Please visit Fairchild's website at www.fairchildsemi.com for additional information.

1. Overview of the Evaluation Board

The FAN9611/12 interleaved dual Boundary-Conduction-Mode (BCM) Power-Factor-Correction (PFC) controllers operate two parallel-connected boost power trains 180º out of phase. Interleaving extends the maximum practical power level of the control technique from about 300W to greater than 800W. Unlike the continuous conduction mode (CCM) technique often used at higher power levels, BCM offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less expensive diodes without sacrificing efficiency. Furthermore, the input and output filters can be smaller due to ripple current cancellation between the power trains and doubling of effective switching frequency.

The advanced line feedforward with peak detection circuit minimizes the output voltage variation during line transients. To guarantee stable operation with less switching loss at light load, the maximum switching frequency is clamped at 525kHz. Synchronization is maintained under all operating conditions.

Protection functions include output over-voltage, over-current, open-feedback, under-voltage lockout, brownout, and redundant latching over-voltage protection. The FAN9611/12 is available in a lead-free 16-lead SOIC package.

This FAN9611/12 evaluation board is a four-layer board designed for 400W (400V/1A) rated power. Thanks to the phase management, the efficiency is maintained above 96% at low-line and high-line, even down to 10% of the rated output power. Efficiency is 96.4% at line voltage 115V_{AC} and 98.2% at 230V_{AC} under full-load conditions.

2. Key Features

- Low Total Harmonic Distortion, High Power Factor
- 180° Out-of-Phase Synchronization
- Automatic Phase Disable at Light Load
- 1.8A Sink, 1.0A Source, High-Current Gate Drivers
- Transconductance (g_M) Error Amplifier for Reduced Overshoot
- Voltage-Mode Control with $(V_{IN})^2$ Feed-forward
- Closed-Loop Soft-Start with Programmable Soft-Start Time for Reduced Overshoot
- Minimum Restart Timer Frequency to Avoid Audible Noise
- Maximum Switching Frequency Clamp
- Brownout Protection with Soft Recovery
- Non-Latching OVP on FB Pin and Second-Level Latching Protection on OVP Pin
- Open-Feedback Protection
- Over-Current and Power-Limit Protection for Each Phase
- Low Startup Current: 80µA Typical
- Works with DC, 50Hz to 400Hz AC Inputs

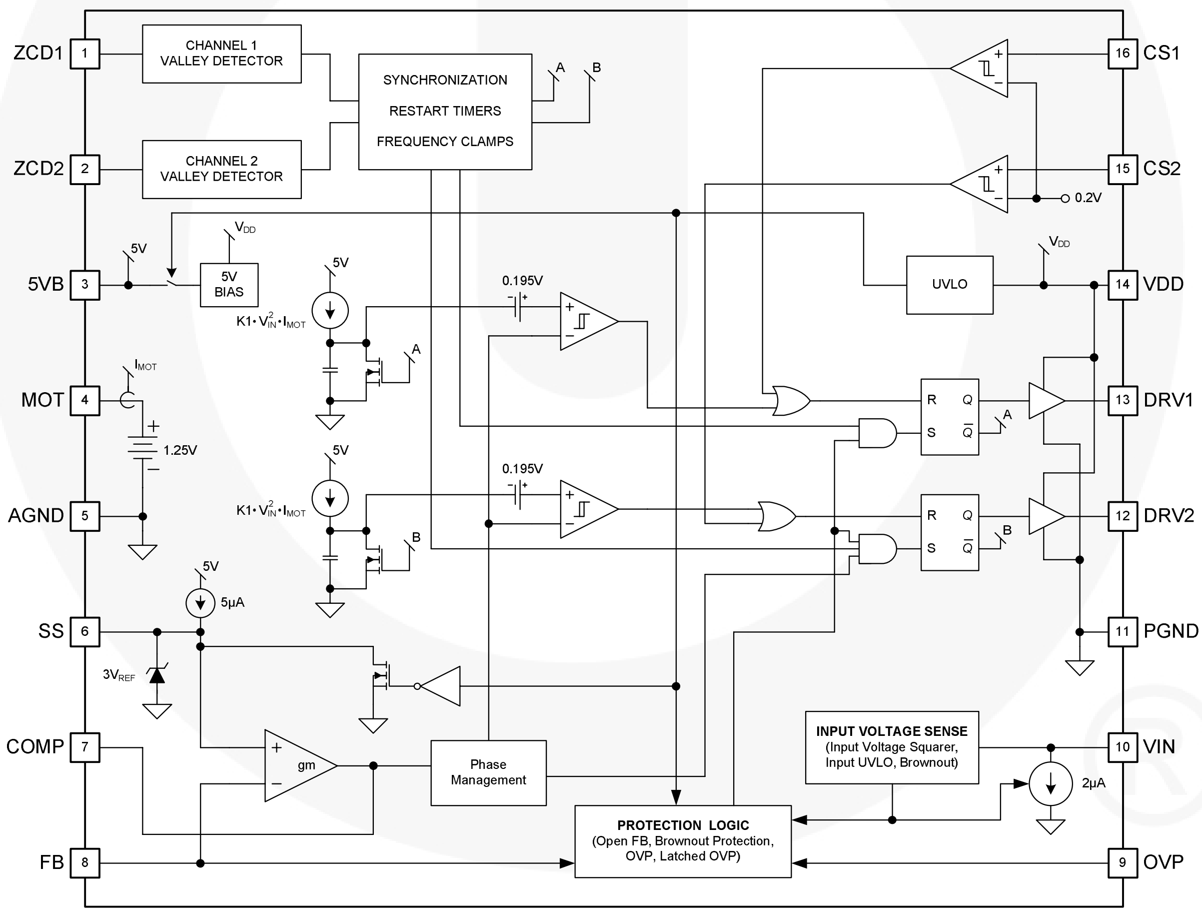


Figure 1. Block Diagram

3. Specifications

This board has been designed and optimized for the following conditions:

Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)
V_{IN} Nominal : 85~264V_{AC} V_{DD} Supply : 13V_{DC}~18V_{DC}	400W	400V-1A

Note:
1. Minimum output voltage during the 20ms hold-up time is 330V_{DC}.

- V_{LINE} = 85~264V_{AC}
- V_{OUT} = 400V
- f_{SW} > 50kHz
- Efficiency > 96% down to 20% load (115V_{AC})
- Efficiency > 97% down to 20% load (230V_{AC})
- PF > 0.99 at full load

The trip points for the built-in protections are set as below in the evaluation board.

- The non-latching output OVP trip point is set at 108% of the nominal output voltage.
- The latching output OVP trip point is set at 117% of the nominal output voltage.
- The line UVLO (brownout protection) trip point is set at 68V_{AC} (10V_{AC} hysteresis).
- The pulse-by-pulse current limit for each MOSFET is set at 9.1A.

The maximum power limit is set at ~120% of the rated output power. The phase management function permits phase shedding/adding ~15% of the nominal output power for high line (230V_{AC}). This level can be programmed by modifying MOT resistor (R6).

4. Test Procedure

Before testing the board; DC voltage supply for V_{DD}, AC voltage supply for line input, and DC electric load for output should be connected to the board properly.

1. Supply V_{DD} for the control chip first. It should be higher than 13V *(refer to the specification for V_{DD} turn-on threshold voltage in Table 1).*

Table 1. Specification Excerpt from FAN9611/12 Datasheet

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
$I_{STARTUP}$	Startup Supply Current	$V_{DD} = V_{ON} – 0.2V$		80	110	µA
I_{DD}	Operating Current	Output Not Switching		3.7	5.2	mA
I_{DD_DYM}	Dynamic Operating Current	f_{SW} = 50kHz; C_{LOAD} = 2nF		4	6	mA
V_{ON}	UVLO Start Threshold, FAN9611	V_{DD} Increasing	9.5	10.0	10.5	V
	UVLO Start Threshold, FAN9612		12.0	12.5	13.0	V
V_{OFF}	UVLO Stop Threshold Voltage	V_{DD} Decreasing	7.0	7.5	8.0	V
V_{HYS}	UVLO Hysteresis, FAN9611	$V_{ON} – V_{OFF}$		2.5		V
	UVLO Hysteresis, FAN9612			5.0		V

2. Connect the AC voltage (85~265V_{AC}) to start the FAN9611/12 evaluation board. Since FAN9611/12 has brownout protection, any input voltages lower than operation range triggers the protection.
3. Change load current (0~1A) and check the operation.

5. Schematic

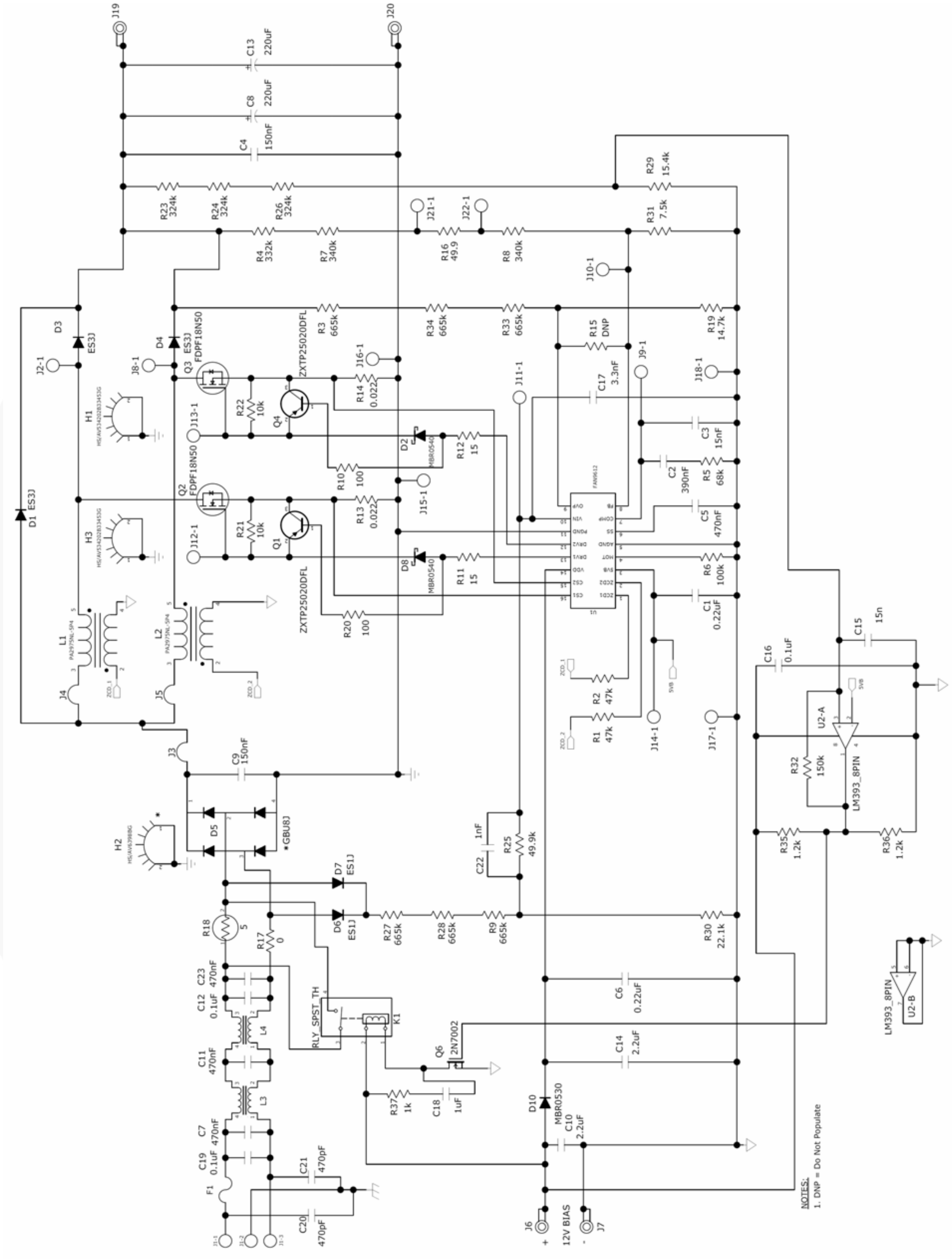


Figure 2. FAN9611/12 400W Evaluation Board Schematic

6. Boost Inductor Specification

PA2075NL from Pulse Engineering (www.pulseeng.com)

- Core: PQ3230 (Ae=161mm^2)
- Bobbin: PQ3230
- Inductance : 200µH

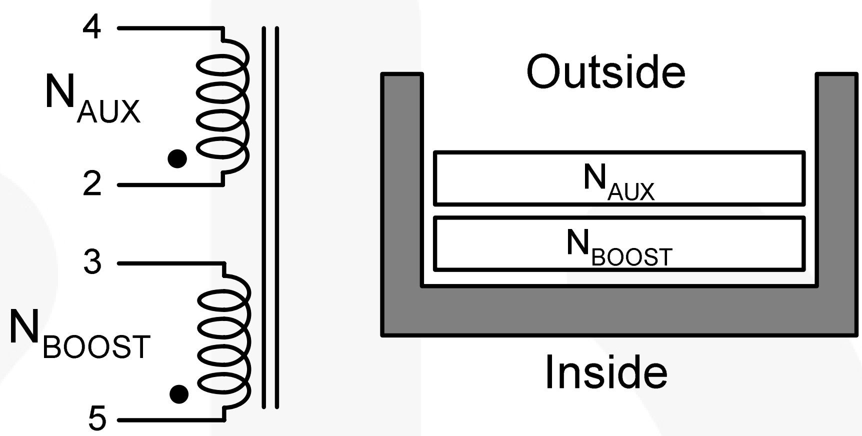
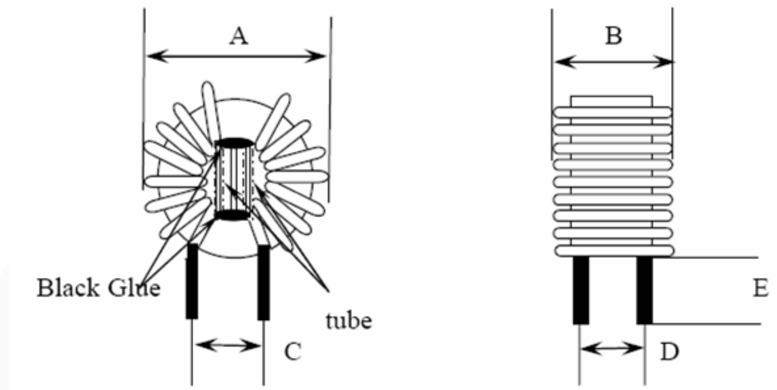


Figure 3. Boost Inductor used in this FAN9611/12 Evaluation Board

Table 2. Inductor Turns Specifications

	Pin	Turns
N1	5 → 3	30
Insulation Tape		
N2	2 → 4	3
Insulation Tape		

7. Line Filter Inductor Specifications



A : 30mm (max)
B: 15 mm (max)
C: 11 mm
D: 13 mm
E: 15±1 mm

Electrical Specifications (1kHz, 1V)

- Inductance: 9.0mH (min.) for each winding
- DC resistance: 0.05Ω (max.) for each winding
- Number of turns: 0.9mm×2/30.5 turns for each winding

Figure 4. Line Filter Inductor Specification

Table 3. Materials List

Component	Material	Manufacturer	UL File Number
Core	T22x14x08	Core T22x14x08, TOMITA	
Wire	THFN-216	Ta Ya Electric Wire Co,. Ltd.	E197768
	UEWN/U	PACIFIC Wire and cable Co., Ltd.	E201757
	UEWE	Tai-1 Electric Wire & Cable Co., Ltd.	E85640
	UWY	Jang Shing Wire Co., Ltd.	E174837
Solder	96.5%, Sn, 3%, Ag, 0.5% Cu	Xin Yuan Co., Ltd.	

8. PCB Layout

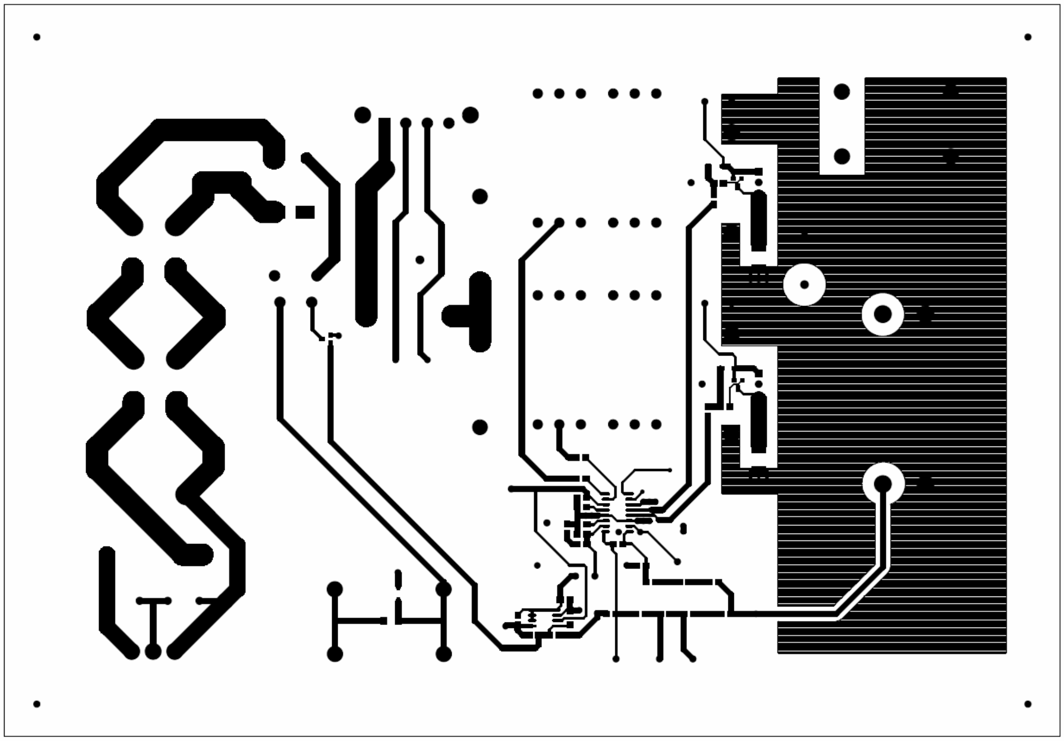


Figure 5. First Layer (Top Side)

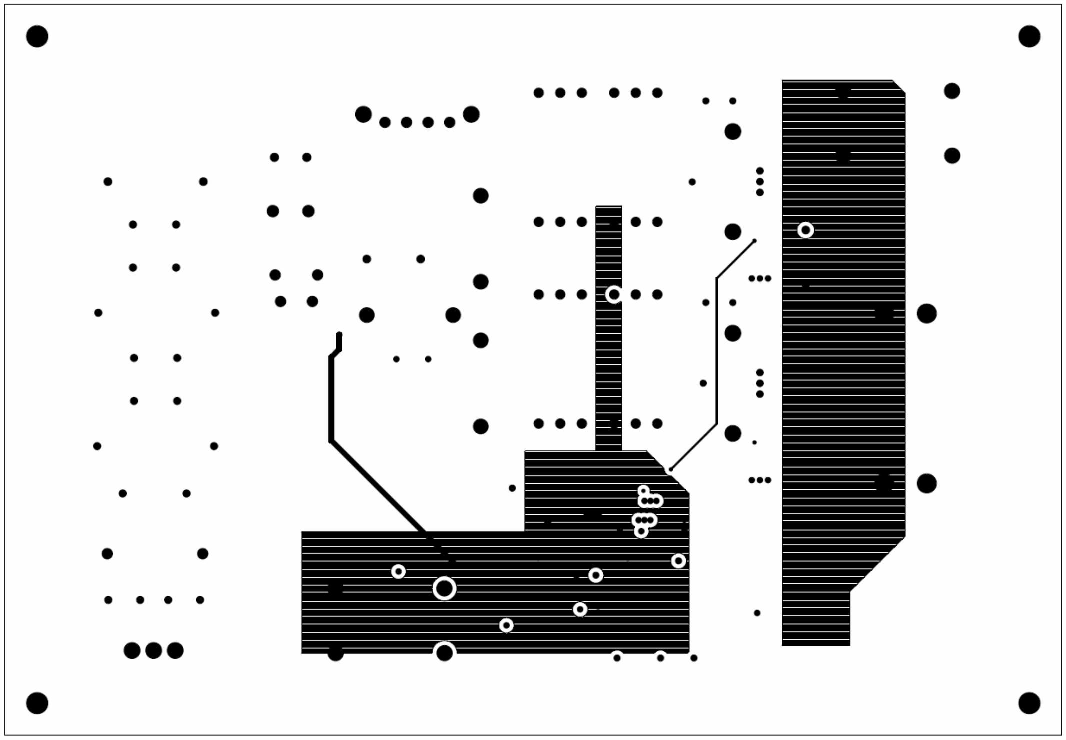


Figure 6. Second Layer (Plane Layer)

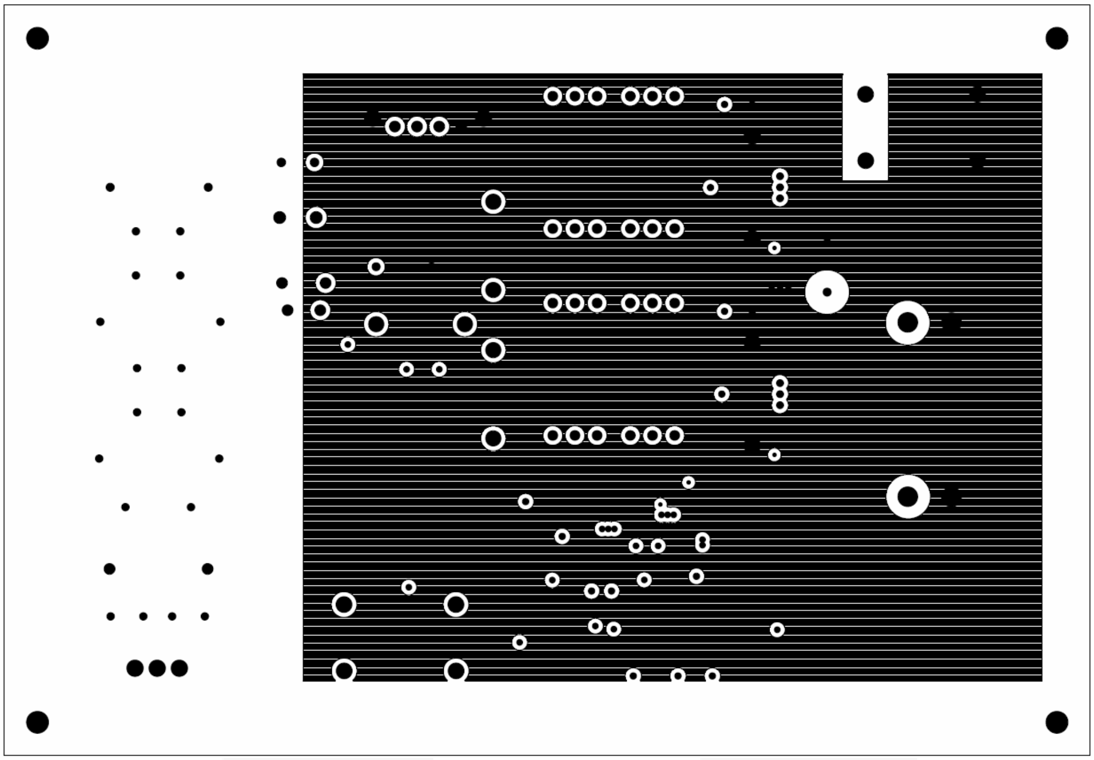


Figure 7. Third Layer (Ground layer)

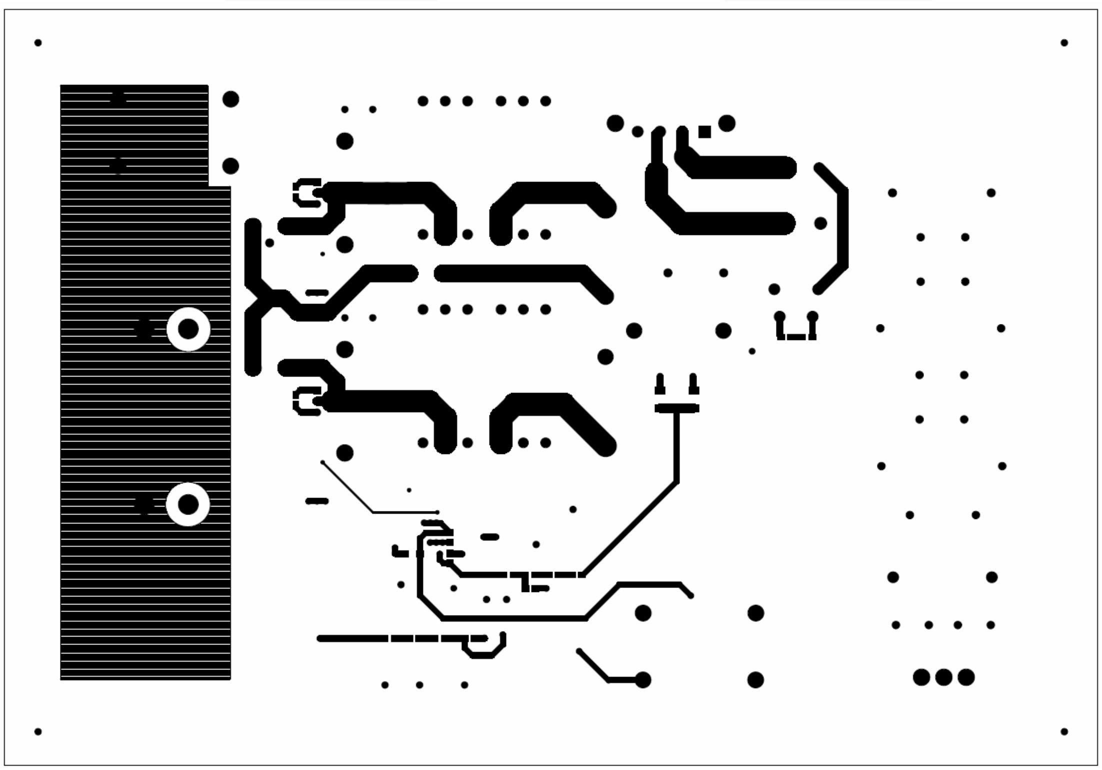


Figure 8. Fourth Layer (Bottom Side)

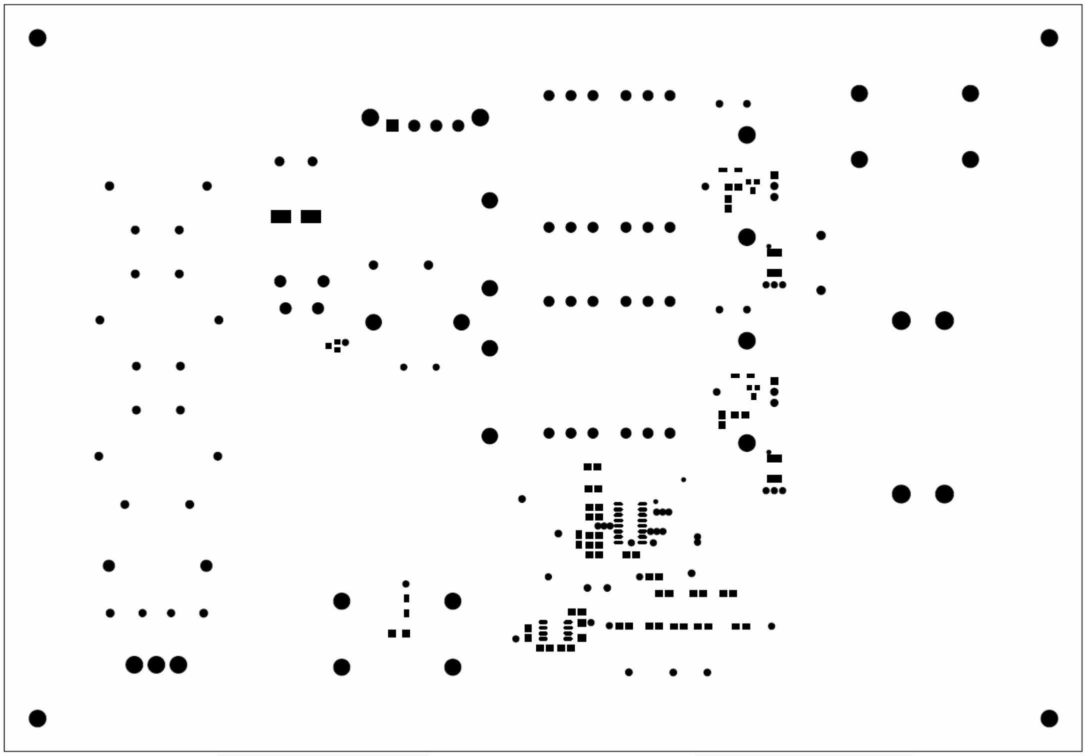


Figure 9. Top Solder Mask

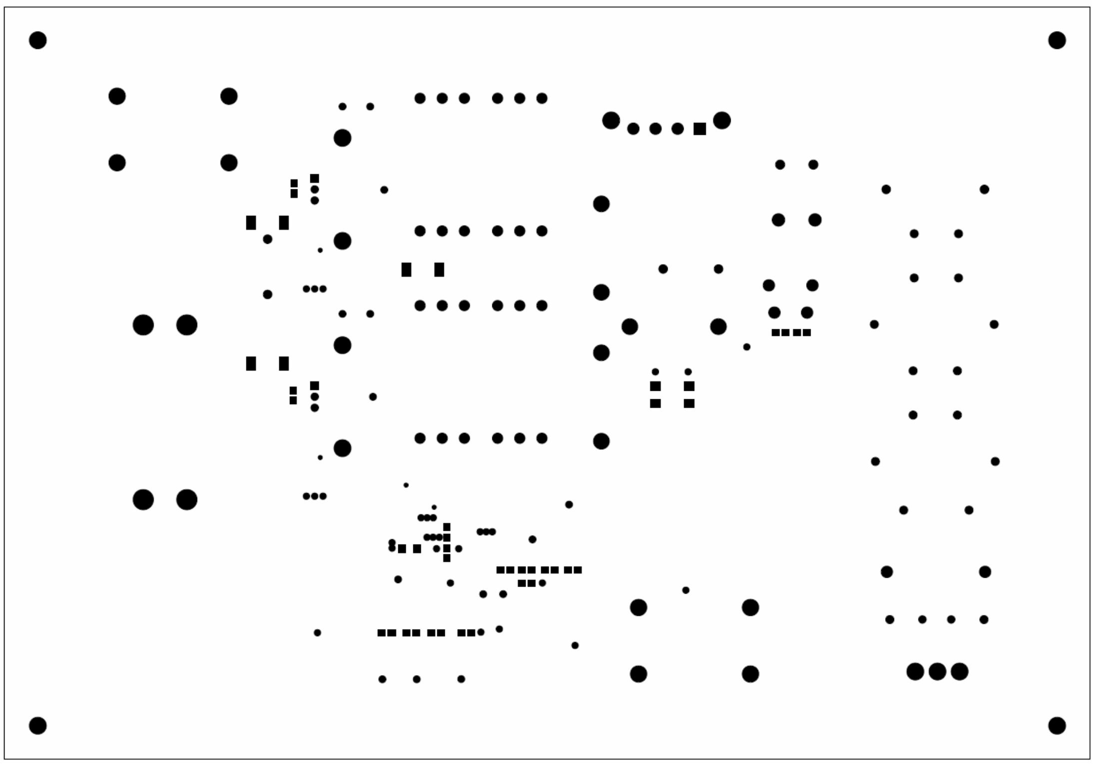


Figure 10. Bottom Solder Mask

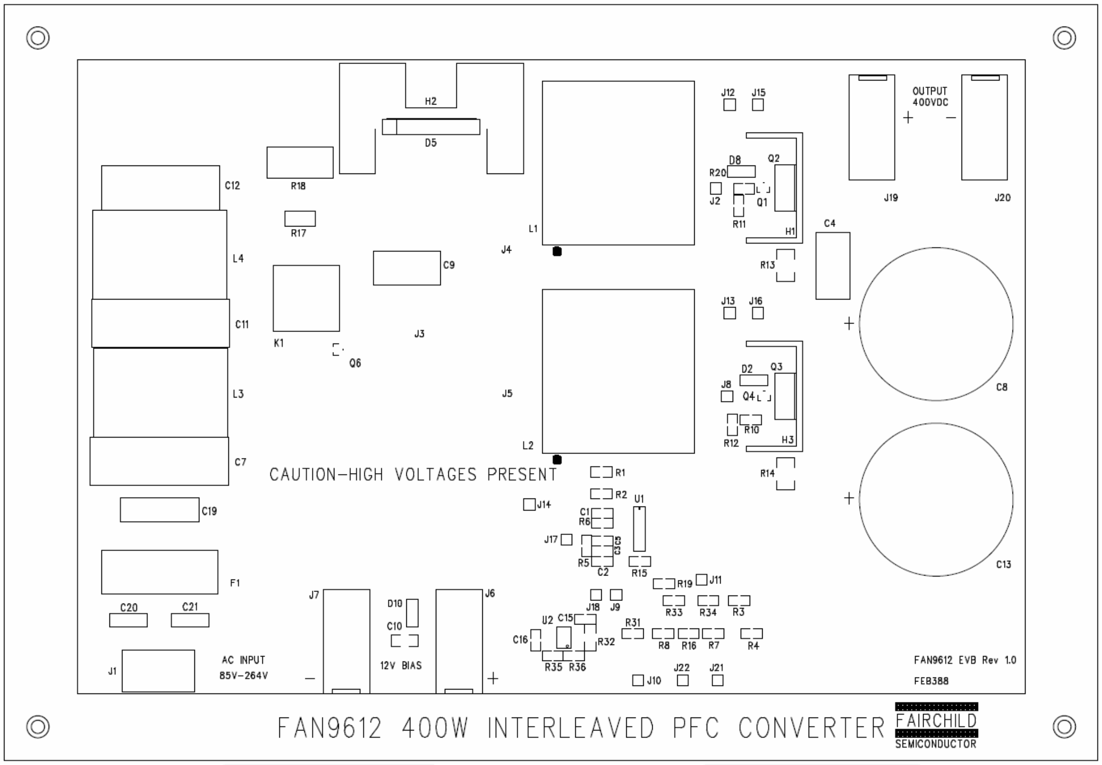


Figure 11. Top Silkscreen

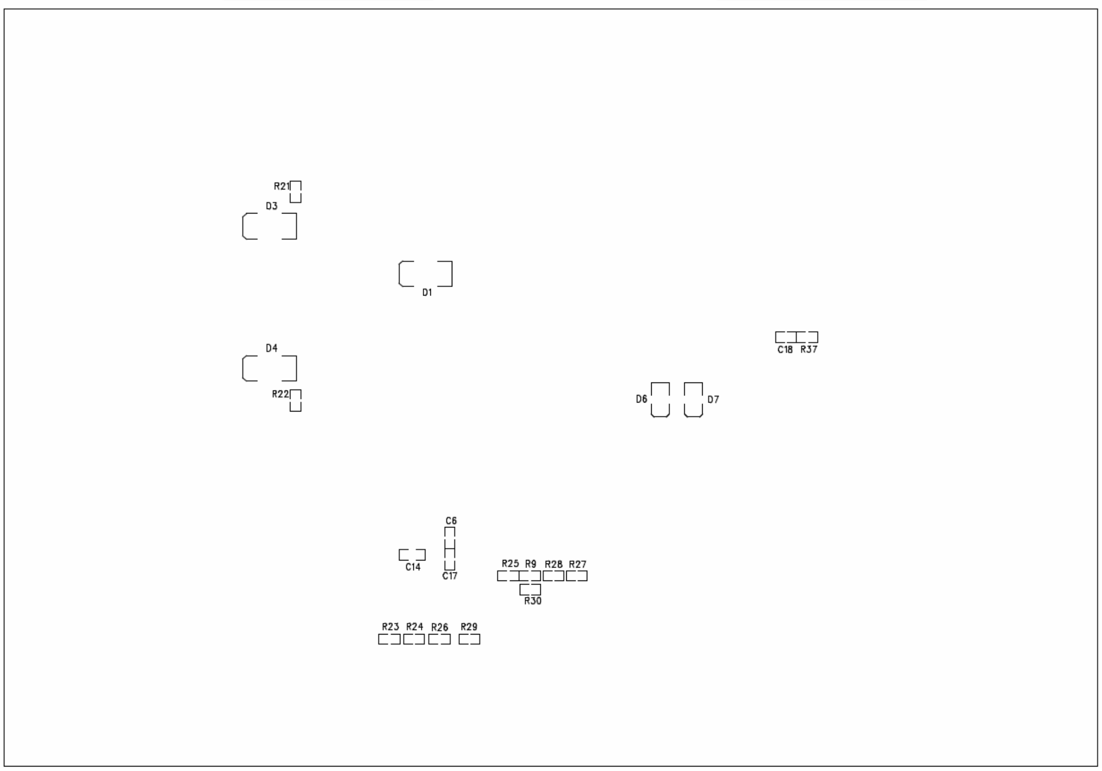


Figure 12. Bottom Silkscreen

9. Bill of Materials (BOM)

Qty	Reference	Part Number	Value	Description	Package Type	Manufacturer
2	C1 C6		0.22µF	CAP, SMD, CERAMIC, 25V, X7R	805	STD
1	C2		390nF	CAP, SMD, CERAMIC, 25V, X7R	805	STD
2	C4 C9	ECWF2W154JAQ	150nF	Cap, 400V, 5%, Polypropylene	Radial, Thru-Hole	Panasonic-ECG
1	C5		470nF	CAP, SMD, CERAMIC,25V, X7R	805	STD
2	C7 C11 C23	B32914A3474	470nF,330V	Cap, 330VAC, 10%, Polypropylene	Box, Thru-Hole	EPCOS
2	C8 C13	EETUQ2W221E	220µF	Cap, Alum, Elect.	Radial, Thru-Hole	Panasonic
2	C10 C14		2.2µF	CAP, SMD, CERAMIC, 25V, X7R	1206	STD
1	C12	HQX104K275R2	0.1µF, 275V	Cap, X series 250VAC, 5%, Polypropylene	Box, Thru-Hole	Fuhjyyu Electronic Industrial Co.
1	C15		15n	CAP, SMD, CERAMIC,25V, X7R	805	STD
1	C16		0.1µF	CAP, SMD, CERAMIC, 25V, X7R	805	STD
1	C18		1µF	CAP, SMD, CERAMIC,50V, X5R	805	STD
1	C19	PHE840MB 6100MB05R17	0.1µF	Cap, X Type, 275VAC, 10%, Polypropylene	Box, Axial	KEMET
2	C20-21	CS85-B2GA471KYNS	470pF	Cap, Ceramic, 250VAC, 10%, Y5P,	Disc, Thru-hole	TDK Corporation
1	C22		1nF	CAP, SMD, CERAMIC, 25V, X7R	805	STD
3	D1 D3-4	S3J		Diode, 600V, 3A, Std recovery	SMC	Fairchild Semiconductor
2	D2 D8	MBR0540		Diode, Schottky,40V, 500mA	SOD-123	Fairchild Semiconductor
1	D5	GBU8J		Bridge Rectifier, 600V, 8A	Thru-Hole	Fairchild Semiconductor
2	D6-7	ES1J		DIODE FAST REC 1A 600V	SMA	Fairchild Semiconductor
1	D10	MBR0530		DIODE SCHOTTKY 30V 500MA SOD-123	SOD-123	Fairchild Semiconductor
1	F1	31.8201		Fuseholder, 5x20mm, 250VAC, 10A	PCB mount, Thru-hole	Schurter Inc
2	H1 H3	534202B33453G		Heatsink, 13.4degC/W, TO-220 with Tab-Koolclip for Q2-3	1"x0.475"x1.18"	Aavid Thermalloy
1	H2	639BG		TO-220 Heat sink for D5, Bridge Rectifier	1.65"x1.5"	Aavid Thermalloy
1	J1	ED100/3DS		Terminal Block, 5MM Vert., 3 Pos.	Thru-hole	On Shore Technology, Inc.
14	J2 J8-18 J21-22	3103-1-00-15-00-00-08-0		Probe-pin, Gold, 0.3" x 40mil dia., 31mil mounting length	Thru-Hole	Mill-Max
3	J3-5			Jumper wire, #16, Insulated, for current probe measurement	Thru-Hole	Custom
2	J6 J19	571-0500		Banana Jack, .175, Horizontal, Insulated_RED	Thru-hole	Deltron
2	J7 J20	571-0100		Banana Jack, .175, Horizontal, Insulated_BLK	Thru-hole	Deltron
2	L3-4	TRN-0197		Common Mode Choke	Thru-Hole	SEN HUEI INDUSTRIAL CO.,LTD
2	Q1 Q4	ZXTP25020DFL		Transistor, PNP, 20V, 1.5A	SOT-23	Zetex
2	Q2-3	FDPF18N50		MOSFET, NCH, 500V, 18A, 0.265 Ohm	TO-220	Fairchild Semiconductor

Continued on following page…

BOM (Continued)

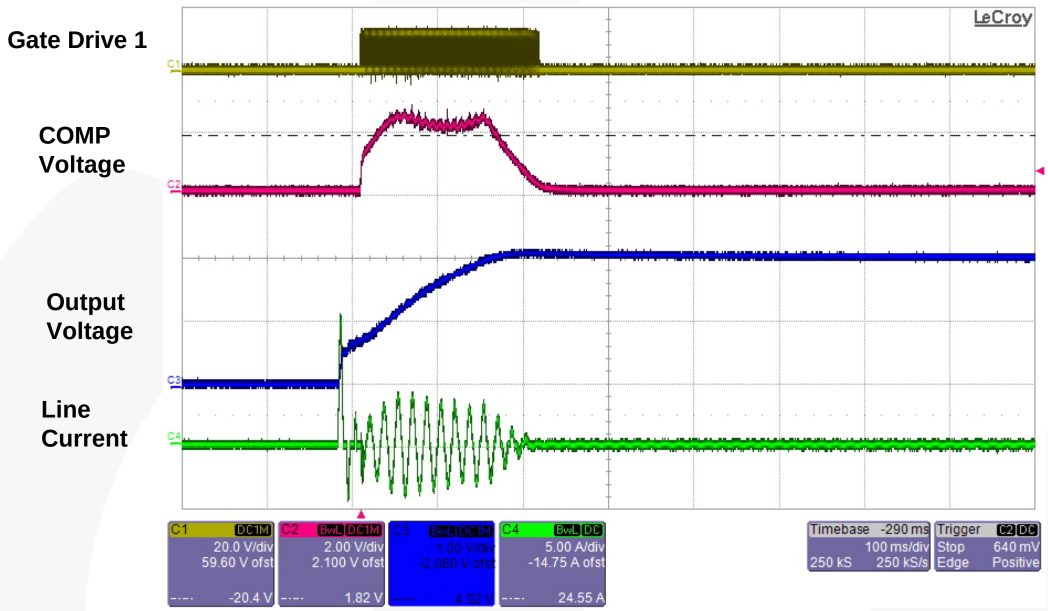
Qty	Reference	Part Number	Value	Description	Package Type	Manufacturer
2	R1-2		47kΩ	RES, SMD, 1/8W	805	STD
6	R3 R9 R27-28 R33-34		665kΩ	RES, SMD, 1/8W	805	STD
1	R4		332kΩ	RES, SMD, 1/8W	805	STD
1	R5		68kΩ	RES, SMD, 1/8W	805	STD
1	R6		100kΩ	RES, SMD, 1/8W	805	STD
2	R7-8		340kΩ	RES, SMD, 1/8W	805	STD
2	R10 R20		100Ω	RES, SMD, 1/8W	805	STD
2	R11-12		15Ω	RES, SMD, 1/8W	805	STD
1	R15		DNP	RES, SMD, 1/8W	805	STD
1	R16		49.9Ω	RES, SMD, 1/8W	805	STD
1	R17		0	RES, SMD, 1/2W	2010	STD
1	R18	B57237S0509M000	5Ω	Thermister, 5Ω	Thru-Hole	EPCOS
1	R19		14.7kΩ	RES, SMD, 1/8W	805	STD
4	1 inserted into each corner of PCB	LCBS-12-01		LOCKING BOARD SUPPORT 3/4", 1 for each PCB corner	Standoff	Richco Plastic Company
1	1 at D5, H2	3103		Nylon Shoulder Washer #4x0.187", Black	Washer	Keystone Electronics
1	1 at D5, H2	MLWZ 003		Split Lock Washer, Metric M 3 Zinc	Washer	B&F Fastener
1	1 at D5, H2	HNZ440		Nut Hex, #4-40 Zinc	Nut	B&F Fastener
1	1 at D5, H2	PMS 440 0050 PH		Screw Machine Phillips, 4-40x1/2" Zinc	Screw	B&F Fastener
1	PWB	FAN9611/12 FEB388 Rev. 0.0.1	FEB388	PWB, 9.8" x 6.8"	PWB	Fairchild Semiconductor
2	R1-2		47kΩ	RES, SMD, 1/8W	805	STD
6	R3 R9 R27-28 R33-34		665kΩ	RES, SMD, 1/8W	805	STD
1	R4		332kΩ	RES, SMD, 1/8W	805	STD
1	R5		68kΩ	RES, SMD, 1/8W	805	STD
1	R6		100kΩ	RES, SMD, 1/8W	805	STD
2	R7-8		340kΩ	RES, SMD, 1/8W	805	STD
2	R10 R20		100Ω	RES, SMD, 1/8W	805	STD
2	R11-12		15Ω	RES, SMD, 1/8W	805	STD
2	R13-14		0.022Ω	RES, SMD, 1/2W	1812	STD
1	R15		DNP	RES, SMD, 1/8W	805	STD
1	R16		49.9Ω	RES, SMD, 1/8W	805	STD

Note:
2. DNP = Do not populate. STD = standard components

10. Test Results

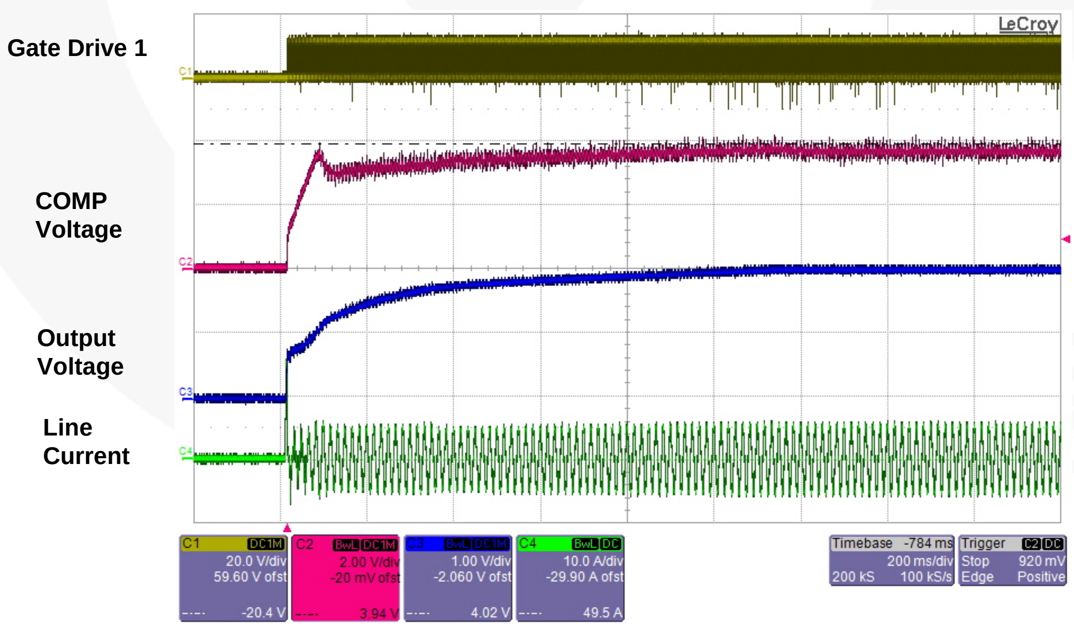
10.1. Startup

Figure 13 and Figure 14 show the startup operation at 115V_{AC} line voltage for no-load and full-load condition, respectively. Due to the closed-loop soft-start, almost no overshoot is observed for no-load startup and full-load startup.



CH1: Gate Drive 1 Voltage (20V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (200V/div), CH4: Line Current (5A/div), Time (100ms/div)

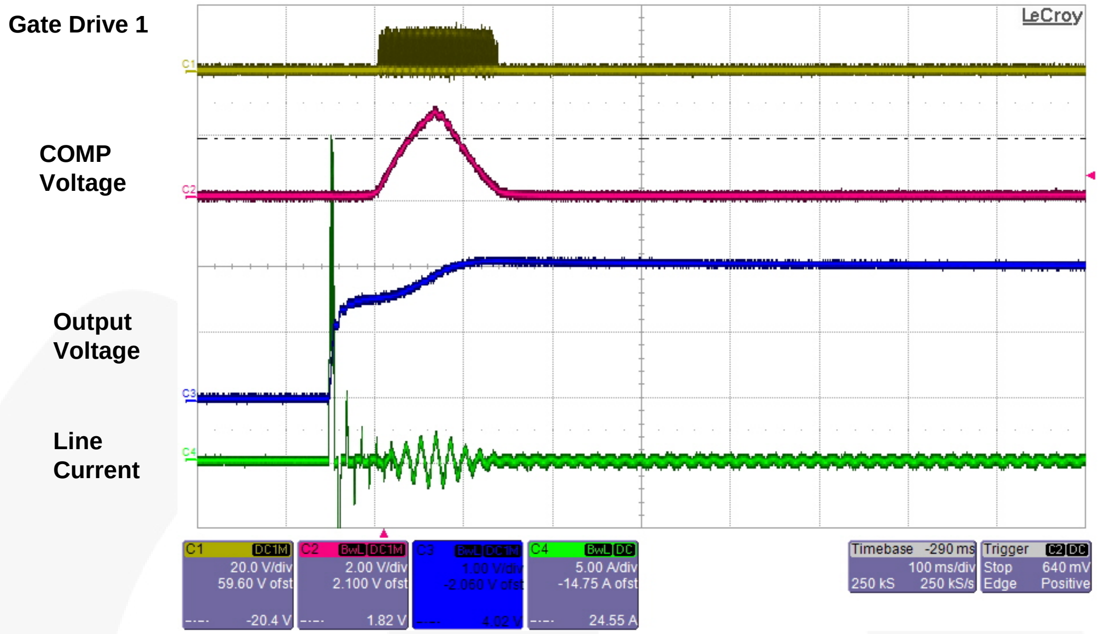
Figure 13. No-Load Startup at 115V_{AC}



CH1: Gate Drive 1 Voltage (20V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (200V/div), CH4: Line Current (10A/div), Time (200ms/div)

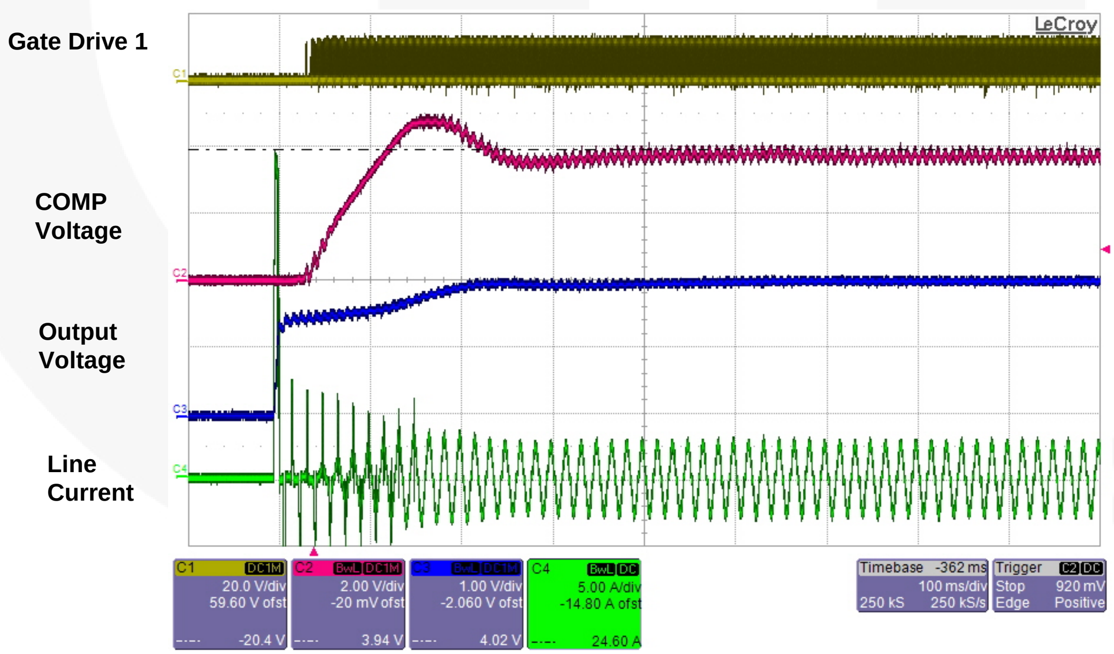
Figure 14. Full-Load Startup at 115V_{AC}

Figure 15 and Figure 16 show the startup operation at 230V_{AC} line voltage for no-load and full-load conditions, respectively. Due to the closed-loop soft-start, almost no overshoot is observed for no-load startup and full-load startup.



CH1: Gate Drive 1 Voltage (20V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (200V/div), CH4: Line Current (5A/div), Time (100ms/div)

Figure 15. No-Load Startup at 230V_{AC}

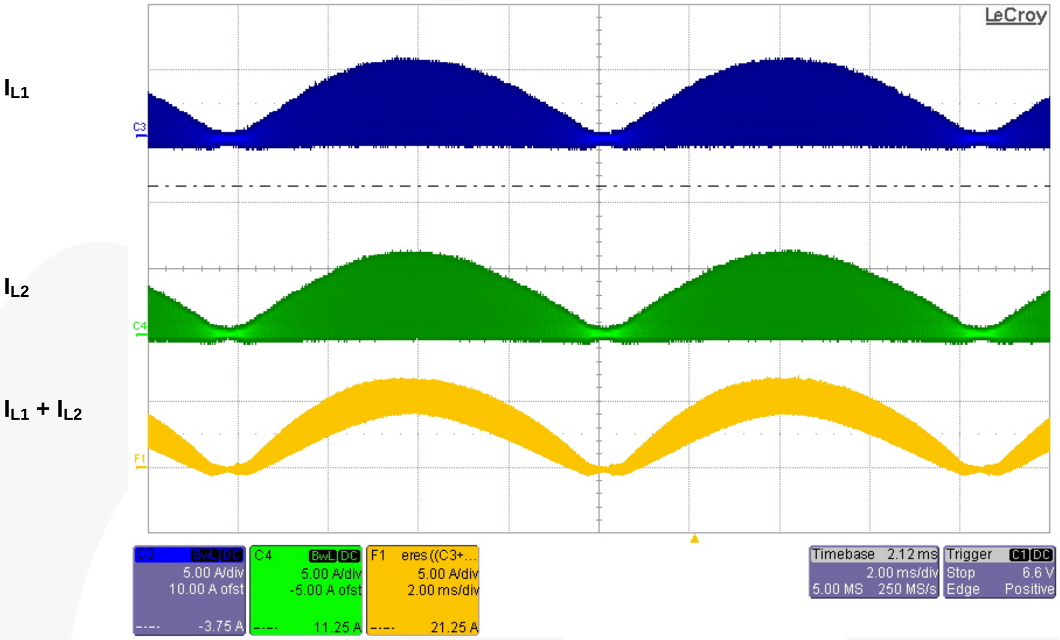


CH1: Gate Drive 1 Voltage (20V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (200V/div), CH4: Line Current (5A/div), Time (100ms/div)

Figure 16. Full-Load Startup at 230V_{AC}

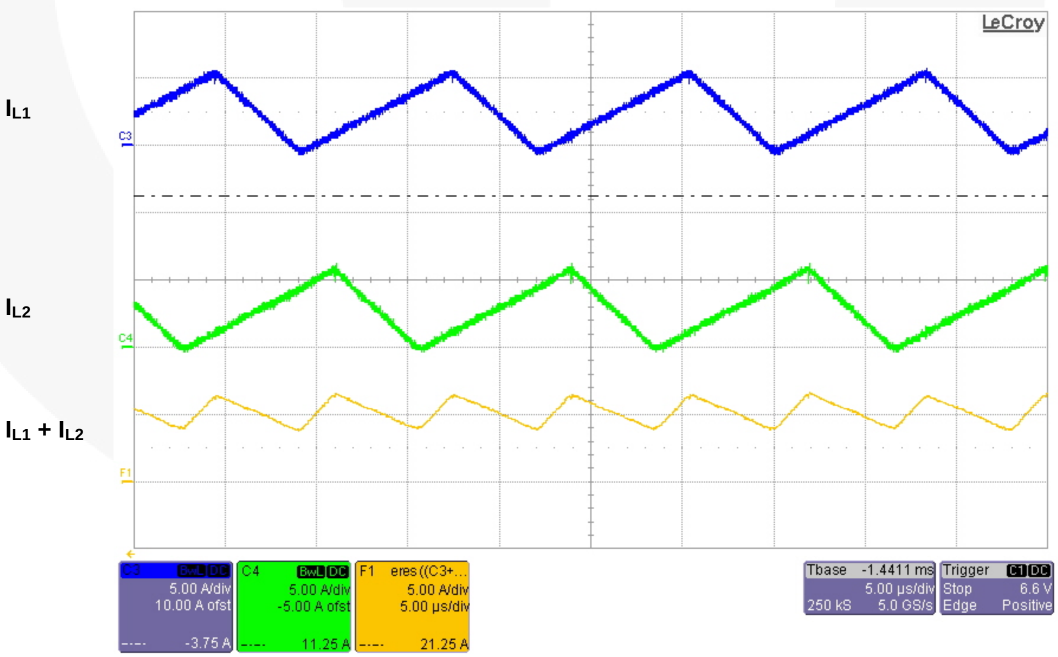
10.2. Normal Operation

Figure 17 and Figure 18 show the two inductor currents and sum of two inductor currents at 115V_{AC} line voltage and full-load conditions. The sum of the inductor currents has relatively small ripple due to the ripple cancellation of interleaving operation.



CH3: Inductor L1 Current (5A/div), CH4: Inductor L2 Current (5A/div),
F1: Sum of Two Inductor Current (5A/div), Time (2ms/div)

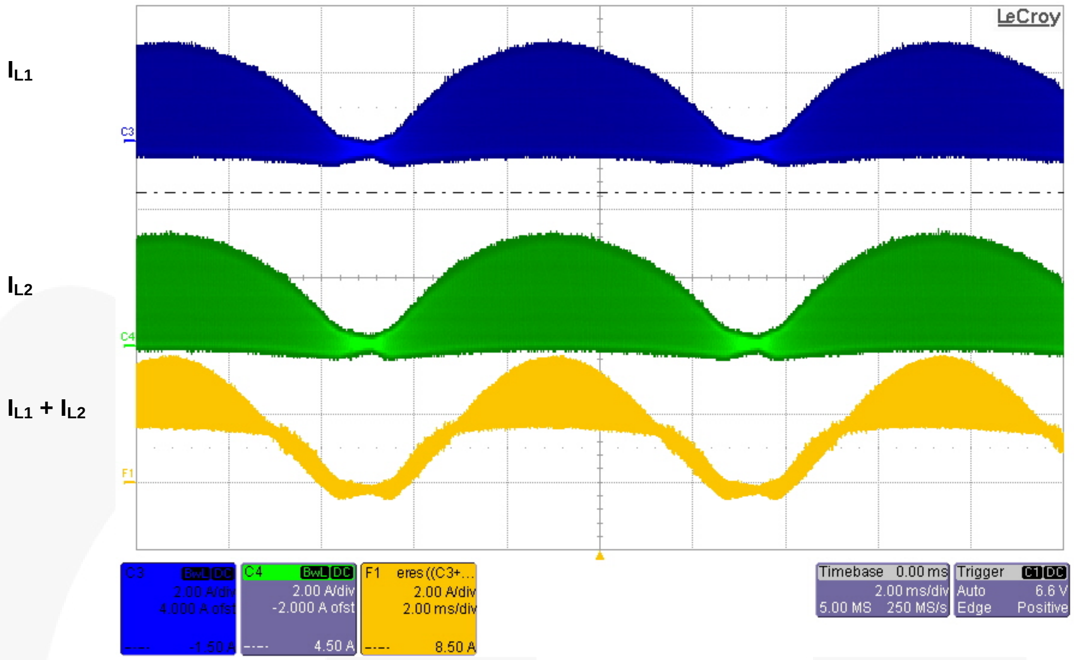
Figure 17. Inductor Current Waveforms at Full-Load and 115V_{AC}



CH3: Inductor L1 Current (5A/div), CH4: Inductor L2 Current (5A/div),
F1: Sum of Two Inductor Current (5A/div), Time (5µs/div)

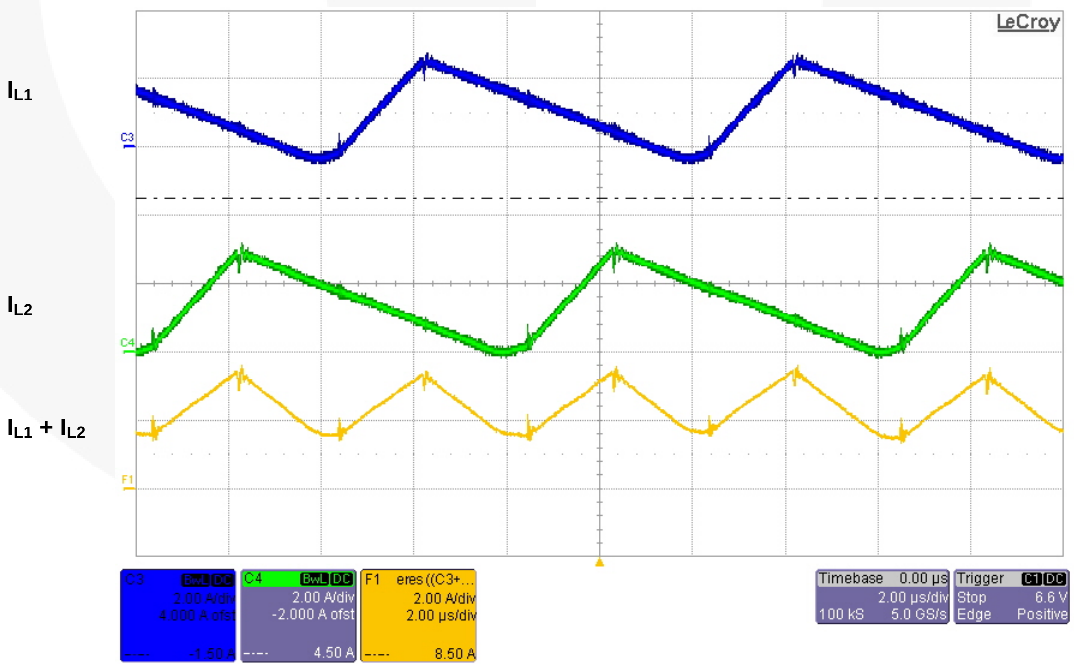
Figure 18. Zoom of Inductor Current Waveforms of Figure 17 at Peak of Line Voltage

Figure 19 and Figure 20 show the two inductor currents and sum of two inductor currents at 230V_{AC} line voltage and full-load conditions. The sum of the inductor currents has relatively small ripple due to the ripple cancellation of interleaving operation.



CH3: Inductor L1 Current (2A/div), CH4: Inductor L2 Current (2A/div),
F1: Sum of Two Inductor Current (2A/div), Time (2ms/div)

Figure 19. Inductor Current Waveforms at Full-Load and 230V_{AC}

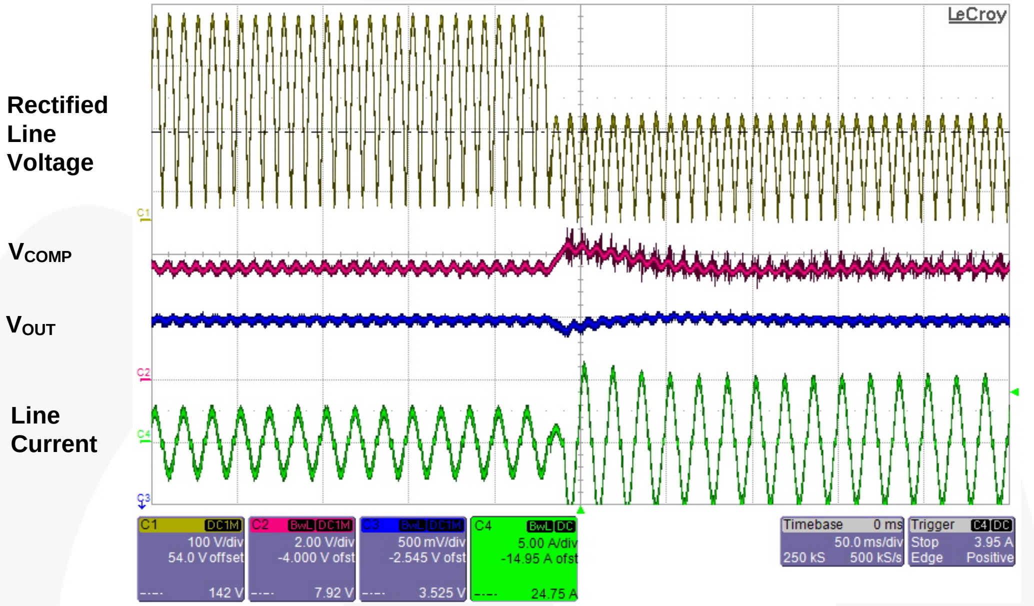


CH3: Inductor L1 Current (2A/div), CH4: Inductor L2 Current (2A/div),
F1: Sum of Two Inductor Current (2A/div), Time (2µs/div)

Figure 20. Zoom of Inductor Current Waveforms of Figure 19 at Peak of Line Voltage

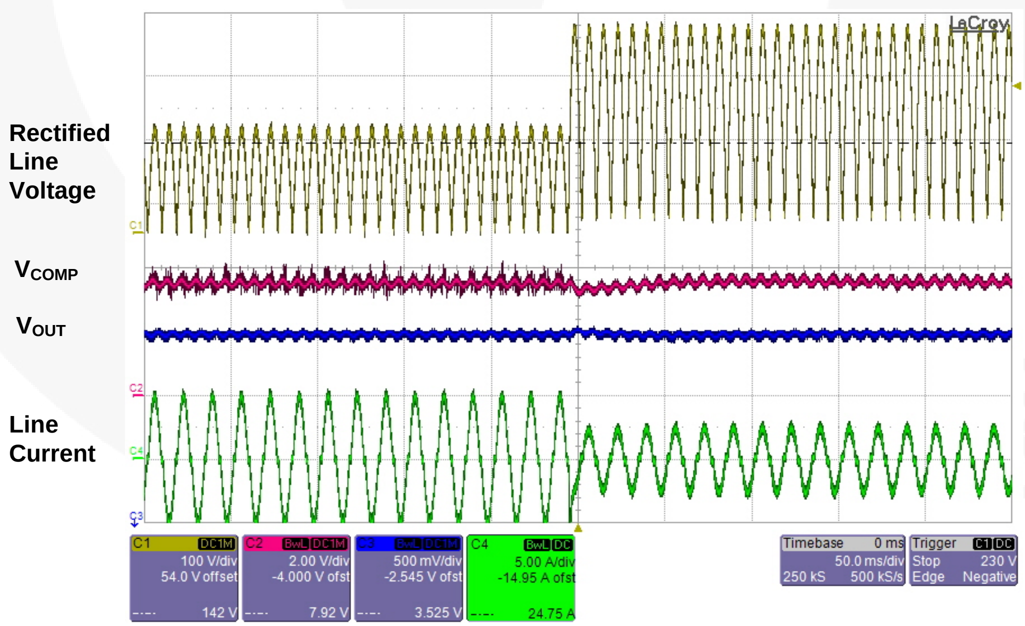
10.3. Line Transient

Figure 21 and Figure 22 show the line transient operation and minimal effect on output voltage due to the line feed-forward function. When the line voltage changes from 230V_{AC} to 115V_{AC}, about 20V (5% of nominal output voltage) voltage undershoot is observed. When the line voltage changes from 115V_{AC} to 230V_{AC}, almost no voltage undershoot is observed.



CH1: Rectified Line Voltage (100V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (100V/div), CH4: Line Current (5A/div), Time (50ms/div)

Figure 21. Line Transient Response at Full-Load Condition (230V_{AC} →115V_{AC})

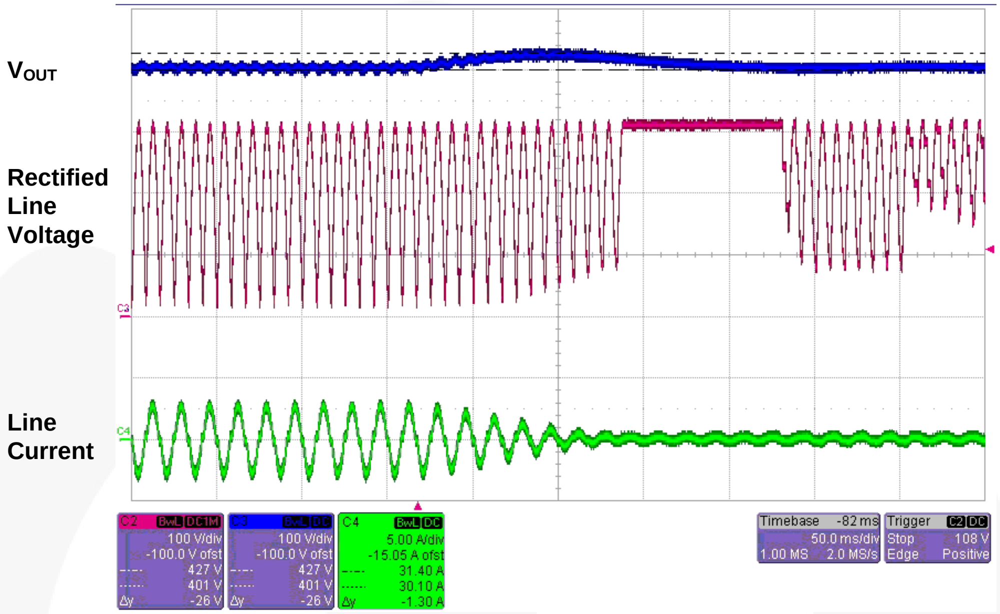


CH1: Rectified Line Voltage (100V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (100V/div), CH4: Line Current (5A/div), Time (50ms/div)

Figure 22. Line Transient Response at Full-Load Condition (115V_{AC} →230V_{AC})

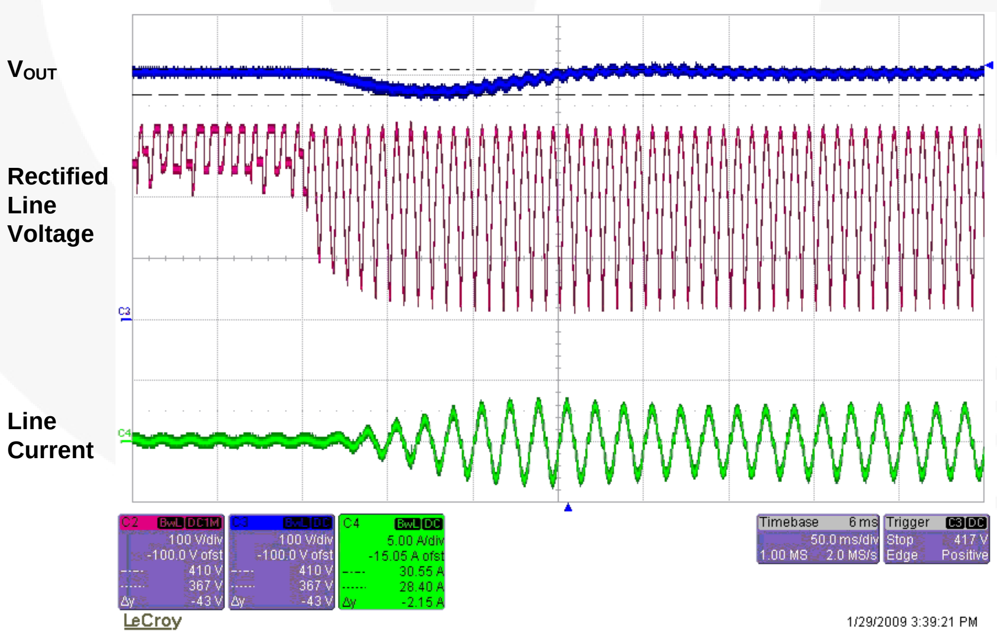
10.4. Load Transient

Figure 23 and Figure 24 show the load-transient operation. When the output load changes from 100% to 0%, 26V (6.5% of nominal output voltage) voltage overshoot is observed. When the output load changes from 0% to 100%, 43V (11% of nominal output voltage) voltage undershoot is observed.



CH2: Rectified line voltage (100V/div), CH3: Output voltage (100V/div),
CH4: Line current (5A/div), Time (50ms/div)

Figure 23. Load Transient Response at 230V$_{AC}$ (Full Load → No Load)

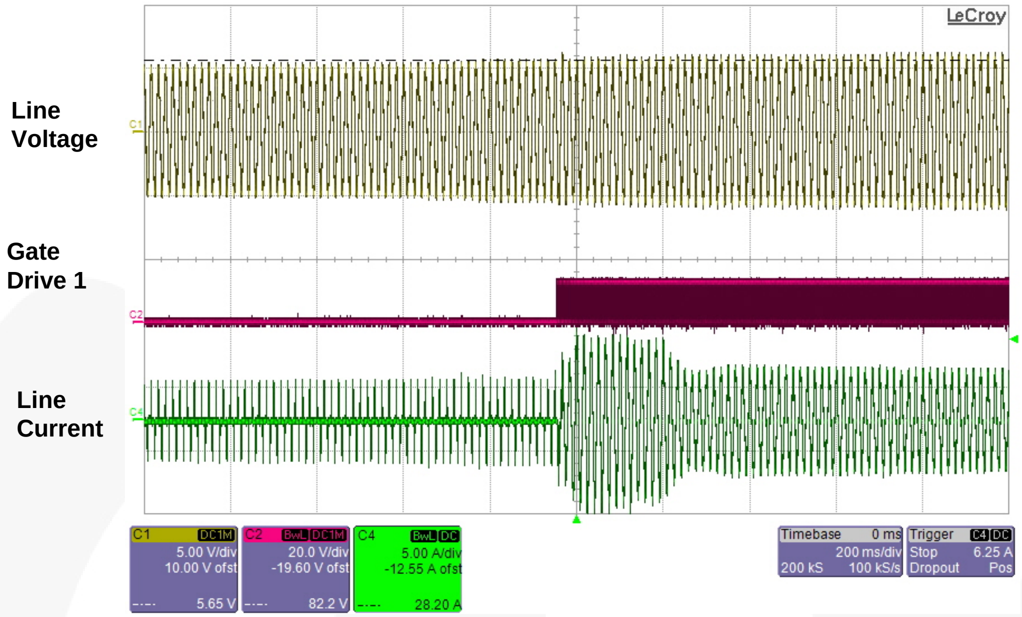


CH2: Rectified Line Voltage (100V/div), CH3: Output Voltage (100V/div),
CH4: Line Current (5A/div), Time (50ms/div)

Figure 24. Load Transient Response at 230V$_{AC}$ (No Load → Full Load)

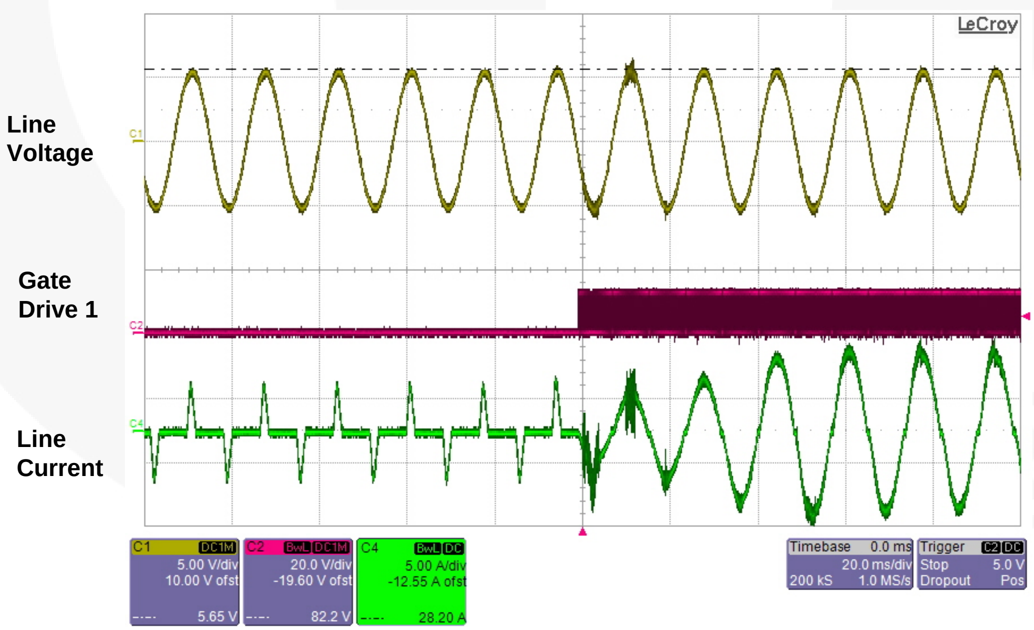
10.5. Brownout Protection

Figure 25 and Figure 26 show the startup operation at slowly increasing line voltage. The power supply starts up when the line voltage reaches around $78V_{AC}$.



CH1: Line Voltage (100V/div), CH2: Gate Drive 1 Voltage (20V/div),
CH4: Line Current (5A/div), Time (200ms/div)

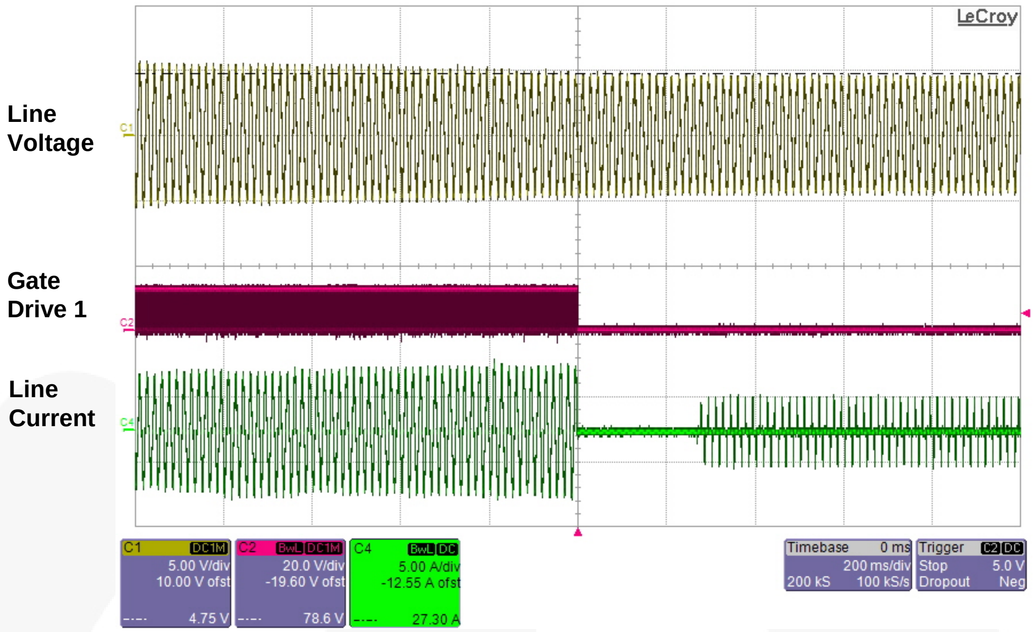
Figure 25. Startup Slowly Increasing the Line Voltage



CH1: Line Voltage (100V/div), CH2: Gate Drive 1 Voltage (20V/div),
CH4: Line Current (5A/div), Time (20ms/div)

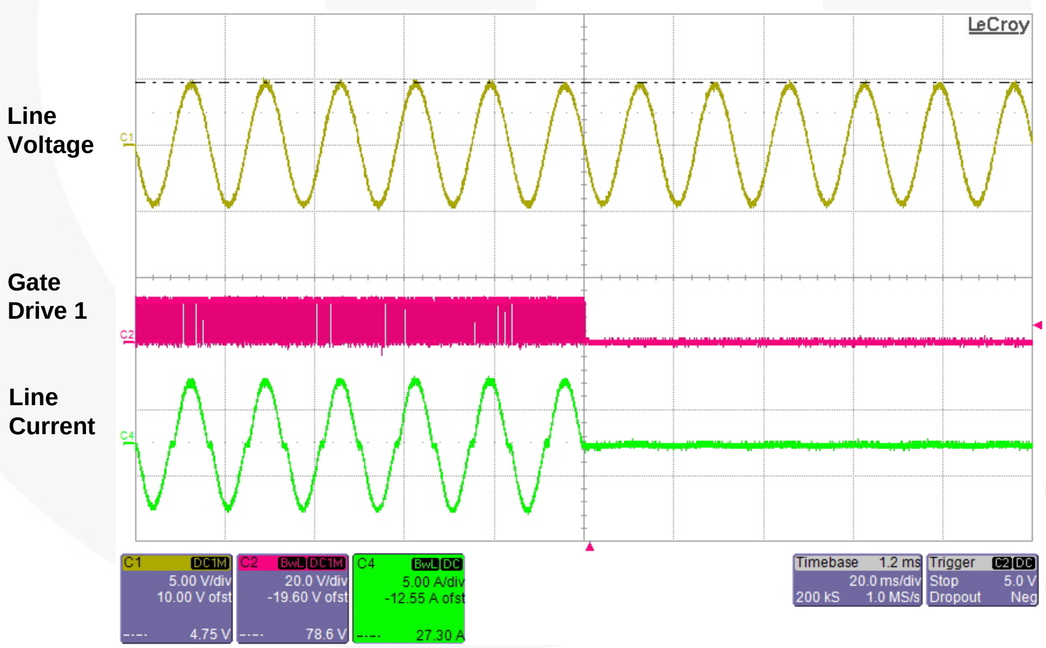
Figure 26. Shutdown Slowly Decreasing the Line Voltage

Figure 27 and Figure 28 show the shutdown operation at slowly decreasing line voltage. The power shuts down when line voltage drops below 68V_{AC}.



CH1: Line Voltage (100V/div), CH2: Gate Drive 1 Voltage (20V/div), CH4: Line Current (5A/div), Time (200ms/div)

Figure 27. Startup Slowly Increasing the Line Voltage

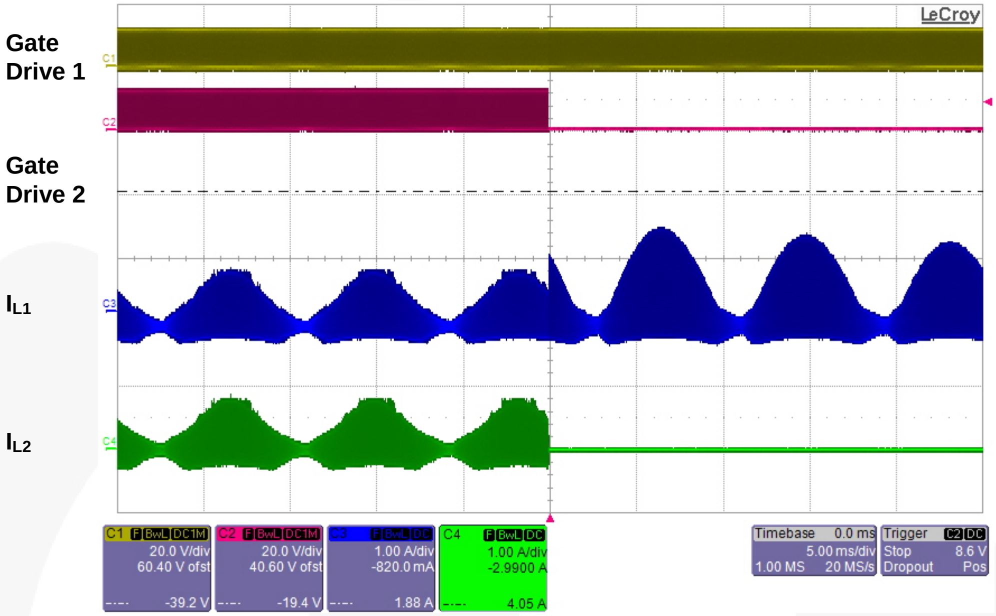


CH1: Line Voltage (100V/div), CH2: Gate Drive 1 Voltage (20V/div), CH4: Line Current (5A/div), Time (20ms/div)

Figure 28. Shutdown Slowly Decreasing the Line Voltage

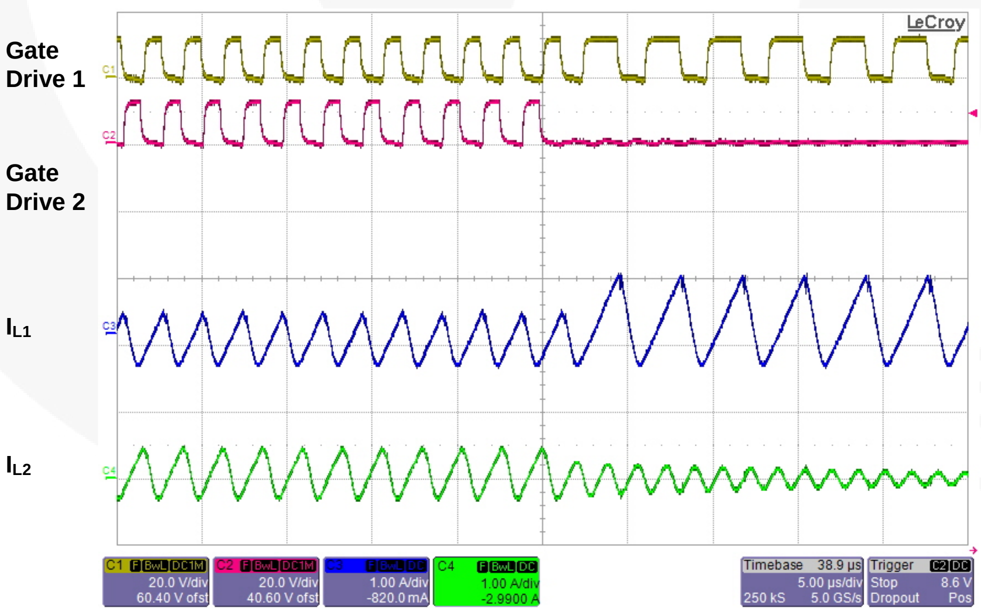
10.6. Phase Management

Figure 29 and Figure 30 show the phase-shedding waveforms. As observed, when the gate drive signal of Channel 2 is disabled, the duty cycle of Channel 1 gate drive signal is doubled to minimize the line current glitch and guarantee smooth transient.



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Inductor L1 Current (1A/div), CH4: Inductor L2 Current (1A/div), Time (5ms/div)

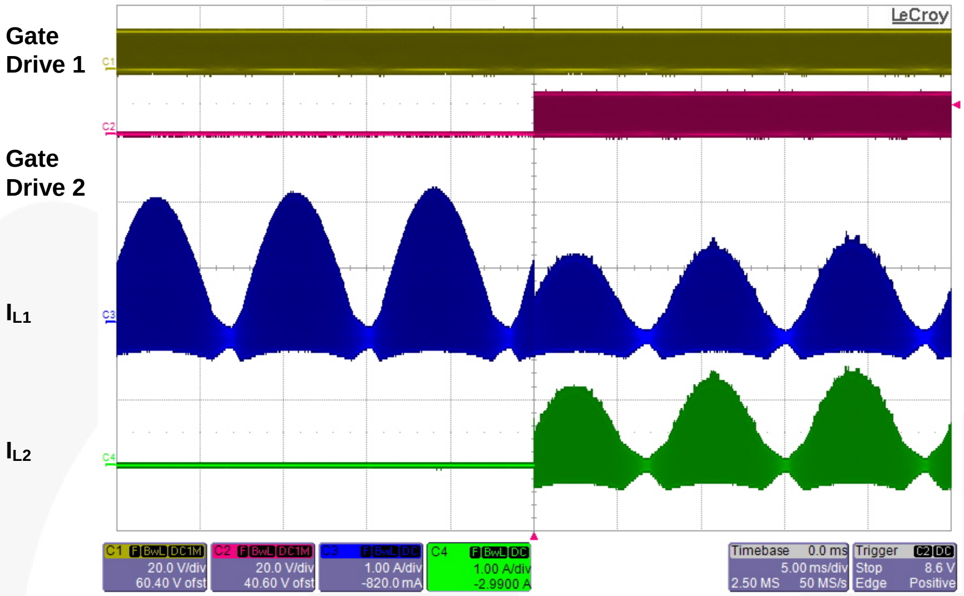
Figure 29. Phase-Shedding Operation



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Inductor L1 Current (1A/div), CH4: Inductor L2 Current (1A/div), Time (5µs/div)

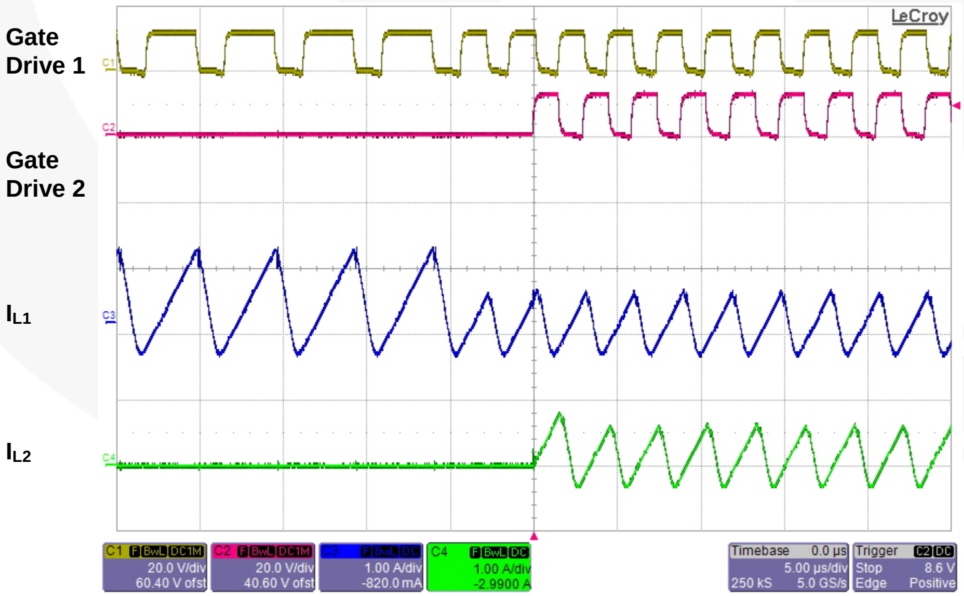
Figure 30. Phase-Shedding Operation (Zoomed-in Timescale)

Figure 31 and Figure 32 show the phase-adding waveforms. As observed, just before the channel 2 gate drive signal is enabled, the duty cycle of Channel 1 gate drive signal is halved to minimize the line current glitch and guarantee smooth transient. In Figure 32, the first pulse of gate drive 2 during the phase-adding operation is skipped to ensure 180 degree out-of-phase interleaving operation during transient.



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Inductor L1 Current (1A/div), CH4: Inductor L2 Current (1A/div), Time (5ms/div)

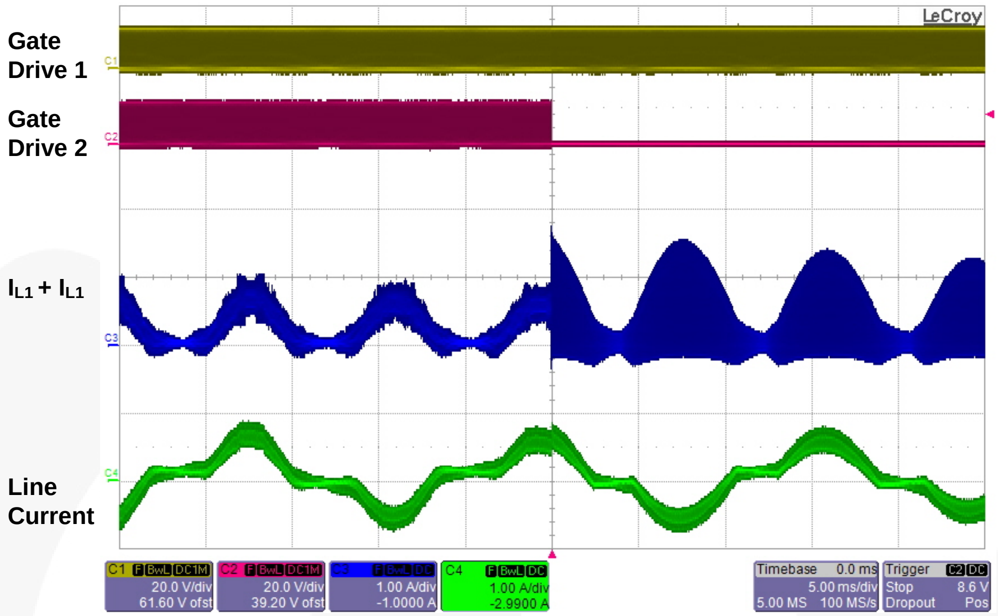
Figure 31. Phase-Adding Operation



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Inductor L1 Current (1A/div), CH4: Inductor L2 Current (1A/div), Time (5µs/div)

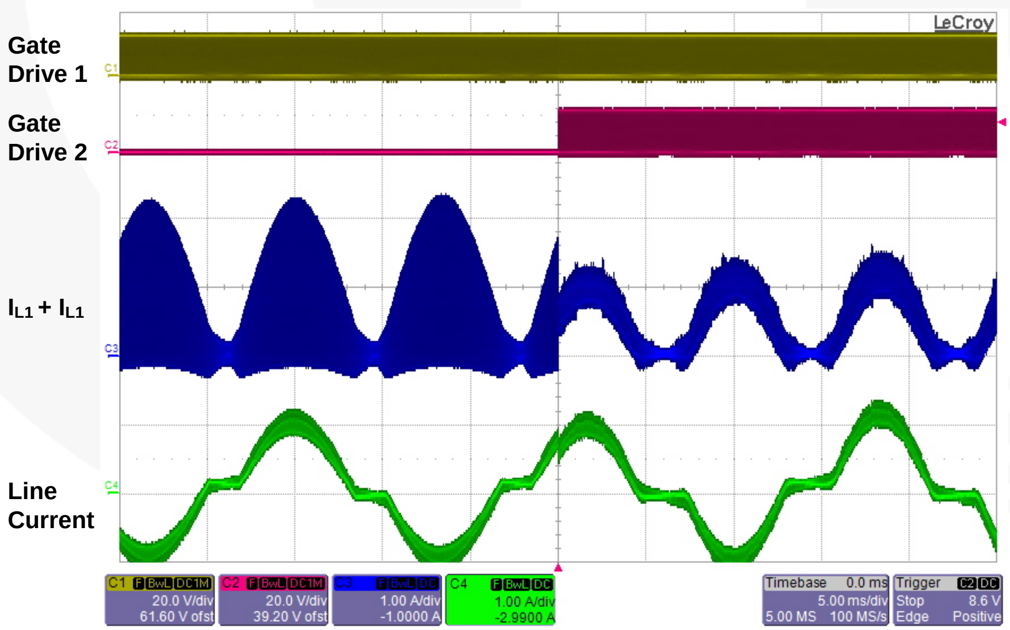
Figure 32. Phase-Adding Operation (Zoomed-in Timescale)

Figure 33 and Figure 34 show the sum of two-inductor current and line current for phase shedding and adding, respectively. The small line-current glitch during phase management exists because the actual average value of inductor current is less than half of the peak value due to the negative portion of inductor current, as shown in Figure 30 and Figure 32. However, the phase management takes place at relatively light-load condition and the effect of this phenomenon is negligible.



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Sum of Two Inductor Currents (1A/div), CH4: Line Current (1A/div), Time (5ms/div)

Figure 33. Phase Shedding and Line Current



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Sum of Two Inductor Currents (1A/div), CH4: Line Current (1A/div), Time (5ms/div)

Figure 34. Phase Adding Operation and Line Current

10.7. Efficiency

Figure 35 through Figure 38 show the measured efficiency of the 400W evaluation board with and without phase management at input voltages of $115V_{AC}$ and $230V_{AC}$. Phase management improves the efficiency at light load by up to 7%, depending on the line voltage and load condition. The phase management thresholds on the test evaluation board are around 15% of the nominal output power (Figure 35 and Figure 36). They can be adjusted upwards to achieve a more desirable efficiency profile (Figure 37 and Figure 38) by increasing the MOT resistor.

Since phase shedding reduces the switching loss by effectively decreasing the switching frequency at light load, a greater efficiency improvement is achieved at $230V_{AC}$, where switching losses dominate. Relatively less improvement is obtained at $115V_{AC}$ since the MOSFET is turned on with zero voltage and switching losses are negligible.

The efficiency measurements include the losses in the EMI filter as well as cable loss; however, the power consumption of the control IC (<< 1W) is not included since an external power supply is used for V_{DD}.

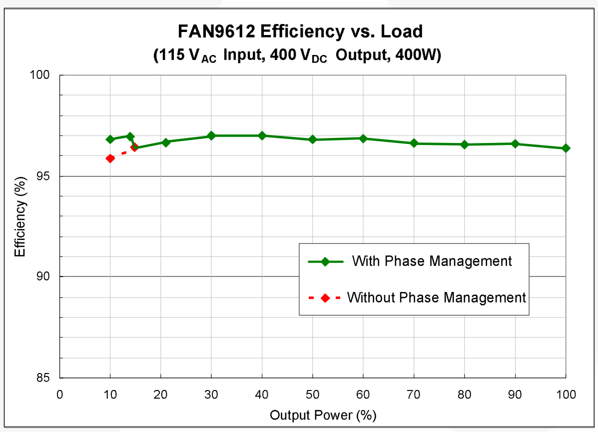


Figure 35. Measured Efficiency at $115V_{AC}$ (Default Thresholds)

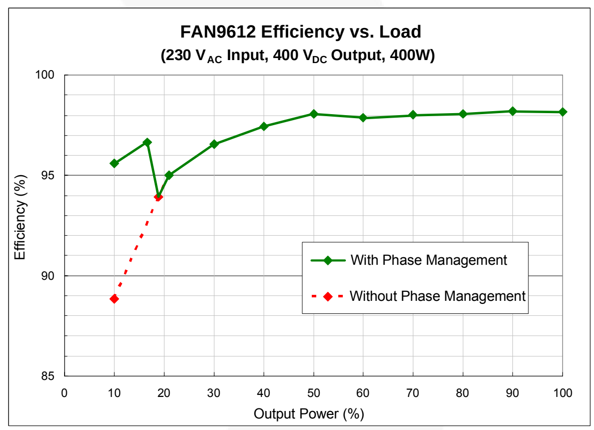


Figure 36. Measured Efficiency at $230V_{AC}$ (Default Thresholds)

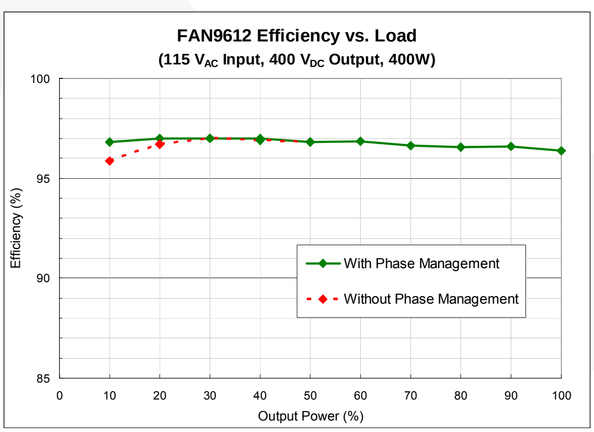


Figure 37. Measured Efficiency at $115V_{AC}$ (Adjusted Thresholds)

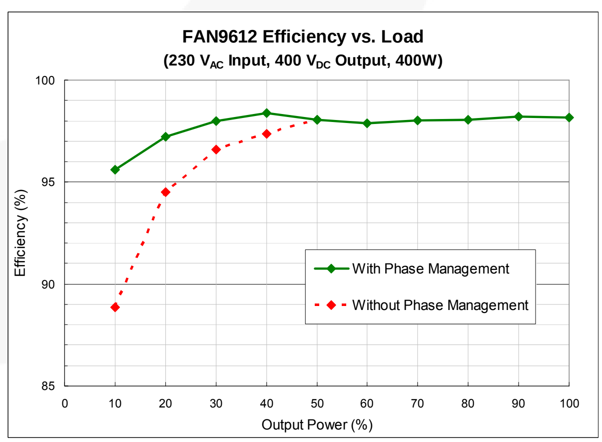


Figure 38. Measured Efficiency at $230V_{AC}$ (Adjusted Thresholds)

10.8. Harmonic Distortion and Power Factor

Figure 39 and Figure 40 compare the measured harmonic current with EN61000 class D and C, respectively, at input voltages of 115V_{AC} and 230V_{AC}. Class D is applied to TV and PC power, while Class C is applied to lighting applications. As can be observed, both regulations are met with sufficient margin.

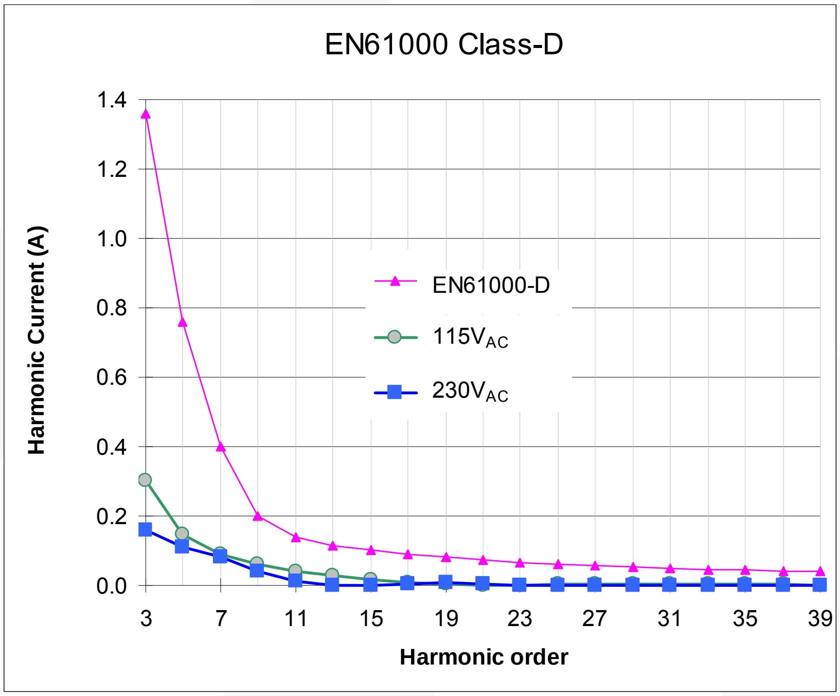


Figure 39. Measured Harmonic Current and EN61000 Class-D Regulation

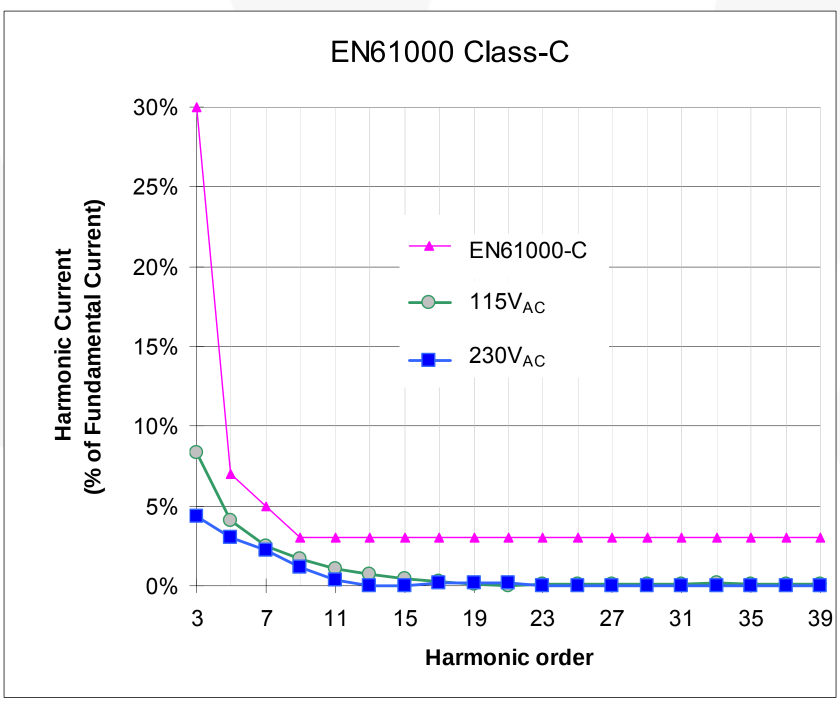


Figure 40. Measured Harmonic Current and EN61000 Class-C Regulation

Figure 41 shows the measured power factors at input voltage of $115V_{AC}$ and $230V_{AC}$. As observed, high power factor above 0.98 is obtained from 100% to 50% load. Table 4 shows the total harmonic distortion at input voltages of $115V_{AC}$ and $230V_{AC}$.

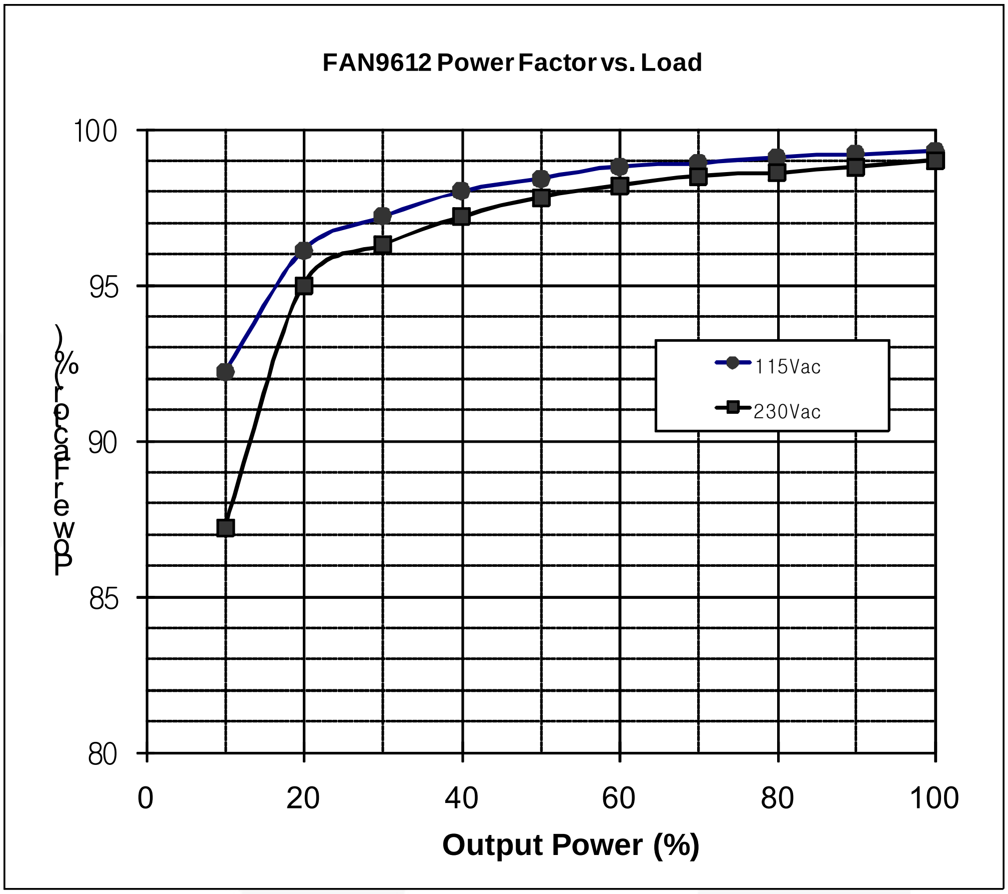


Figure 41. Measured Power Factor

Table 4. Total Harmonic Distortion (THD)

Line Voltage	100 % Load	75 % Load	50 % Load	25 % Load
$115V_{AC}$	9.68%	11.82%	15.87%	24.08%
$230V_{AC}$	11.36%	12.95%	15.30%	16.81%

11. References

Datasheet: FAN9611 / FAN9612 – Interleaved Dual BCM PFC Controllers

AN-6086 – "Design Consideration for interleaved Boundary Conduction Mode (BCM) PFC using FAN9612"

12. Ordering Information

Orderable Part Number	Description
FEB388	FAN9611/FAN9612 400W Evaluation Board

13. Revision History

Date	Rev. #	Description
August 2010	0.0.1	Initial release
August 2010	0.0.2	Added PCB layout figures

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9