

The S-8249 Series is a voltage monitoring IC with a cell balancing function and includes a high-accuracy voltage detection circuit and a delay circuit.

The S-8249 Series is suitable for cell balancing and overcharge protection of batteries and capacitors.

## ■ Features

- High-accuracy voltage detection circuit
    - Cell balancing detection voltage: 2.0 V to 4.6 V (5 mV step) Accuracy  $\pm 12$  mV ( $2.0 \text{ V} \leq V_{\text{BU}} < 2.4 \text{ V}$ )  
Accuracy  $\pm 0.5\%$  ( $2.4 \text{ V} \leq V_{\text{BU}} \leq 4.6 \text{ V}$ )
    - Cell balancing release voltage: 2.0 V to 4.6 V<sup>\*1</sup> Accuracy  $\pm 24$  mV ( $2.0 \text{ V} \leq V_{\text{BL}} < 2.4 \text{ V}$ )  
Accuracy  $\pm 1.0\%$  ( $2.4 \text{ V} \leq V_{\text{BL}} \leq 4.6 \text{ V}$ )
    - Overcharge detection voltage: 2.0 V to 4.6 V (5 mV step) Accuracy  $\pm 12$  mV ( $2.0 \text{ V} \leq V_{\text{CU}} < 2.4 \text{ V}$ )  
Accuracy  $\pm 0.5\%$  ( $2.4 \text{ V} \leq V_{\text{CU}} \leq 4.6 \text{ V}$ )
    - Overcharge release voltage: 2.0 V to 4.6 V<sup>\*2</sup> Accuracy  $\pm 24$  mV ( $2.0 \text{ V} \leq V_{\text{CL}} < 2.4 \text{ V}$ )  
Accuracy  $\pm 1.0\%$  ( $2.4 \text{ V} \leq V_{\text{CL}} \leq 4.6 \text{ V}$ )
  - Built-in Nch transistor with ON resistance of 5  $\Omega$  typ. between the CB pin and the VSS pin
  - Current consumption: 2.0  $\mu\text{A}$  max. ( $T_a = +25^\circ\text{C}$ )
  - Delay times are generated only by an internal circuit (External capacitors are unnecessary).
  - CO pin output form and output logic are selectable: CMOS output Active "H", active "L"  
Nch open-drain output Active "H", active "L"
  - Switchable to power-saving mode by using the  $\overline{\text{CE}}$  pin
  - Operation temperature range:  $T_a = -40^\circ\text{C}$  to  $+85^\circ\text{C}$
  - Lead-free (Sn 100%), halogen-free
- \*1. Cell balancing release voltage = Cell balancing detection voltage – Cell balancing hysteresis voltage  
(Cell balancing hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 50 mV step.)
- \*2. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage  
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 50 mV step.)

## ■ Applications

- Rechargeable battery module
- Capacitor module

## ■ Package

- SOT-23-6

■ Block Diagram



\*1. All diodes shown in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name



\*1. Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

| Package Name | Dimension    | Tape         | Reel         |
|--------------|--------------|--------------|--------------|
| SOT-23-6     | MP006-A-P-SD | MP006-A-C-SD | MP006-A-R-SD |

3. Product name list

Table 2 (2 / 1)

| Product Name    | Cell Balancing Detection Voltage [V <sub>BU</sub> ] | Cell Balancing Release Voltage [V <sub>BL</sub> ] | Overcharge Detection Voltage [V <sub>CU</sub> ] | Overcharge Release Voltage [V <sub>CL</sub> ] | CO Pin Output Form    | CO Pin Output Logic | Combination of Delay Time |
|-----------------|---|---|---|---|-----------------------|---------------------|---------------------------|
| S-8249AAA-M6T1U | 2.600 V   | 2.600 V   | 2.750 V   | 2.750 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAB-M6T1U | 3.000 V   | 3.000 V   | 3.150 V   | 3.150 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAC-M6T1U | 3.000 V   | 3.000 V   | 3.200 V   | 3.200 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAD-M6T1U | 3.100 V   | 3.100 V   | 3.250 V   | 3.250 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAE-M6T1U | 3.100 V   | 3.100 V   | 3.300 V   | 3.300 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAF-M6T1U | 2.600 V   | 2.600 V   | 2.800 V   | 2.800 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAG-M6T1U | 2.400 V   | 2.400 V   | 2.900 V   | 2.900 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAH-M6T1U | 2.400 V   | 2.400 V   | 3.000 V   | 3.000 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAI-M6T1U | 2.100 V   | 2.100 V   | 3.000 V   | 3.000 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAK-M6T1U | 2.400 V   | 2.400 V   | 3.200 V   | 3.200 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAL-M6T1U | 2.100 V   | 2.000 V   | 3.200 V   | 3.200 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAM-M6T1U | 2.620 V   | 2.520 V   | 2.800 V   | 2.700 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAN-M6T1U | 3.300 V   | 3.300 V   | 4.080 V   | 3.930 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAO-M6T1U | 2.000 V   | 2.000 V   | 3.000 V   | 3.000 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAP-M6T1U | 3.700 V   | 3.700 V   | 4.500 V   | 4.500 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAQ-M6T1U | 3.800 V   | 3.800 V   | 4.080 V   | 3.930 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAR-M6T1U | 2.800 V   | 2.800 V   | 3.150 V   | 3.150 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAS-M6T1U | 2.800 V   | 2.800 V   | 3.200 V   | 3.200 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAT-M6T1U | 2.800 V   | 2.800 V   | 3.100 V   | 3.100 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAU-M6T1U | 2.500 V   | 2.400 V   | 3.800 V   | 3.700 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAV-M6T1U | 2.300 V   | 2.200 V   | 3.800 V   | 3.700 V                                       | CMOS output           | Active "H"          | (1)                       |
| S-8249AAW-M6T1U | 2.650 V   | 2.600 V   | 2.750 V   | 2.650 V                                       | Nch open-drain output | Active "L"          | (1)                       |
| S-8249AAZ-M6T1U | 4.150 V   | 4.150 V   | 4.275 V   | 4.275 V                                       | CMOS output           | Active "H"          | (2)                       |

**Table 2 (2 / 2)**

| Product Name    | Cell Balancing Detection Voltage [V <sub>BU</sub> ] | Cell Balancing Release Voltage [V <sub>BL</sub> ] | Overcharge Detection Voltage [V <sub>CU</sub> ] | Overcharge Release Voltage [V <sub>CL</sub> ] | CO Pin Output Form | CO Pin Output Logic | Combination of Delay Time |
|-----------------|---|---|---|---|--------------------|---------------------|---------------------------|
| S-8249ABA-M6T1U | 3.650 V   | 3.550 V   | 3.800 V   | 3.500 V                                       | CMOS output        | Active "L"          | (3)                       |
| S-8249ABB-M6T1U | 4.350 V   | 4.350 V   | 4.425 V   | 4.325 V                                       | CMOS output        | Active "L"          | (3)                       |
| S-8249ABC-M6T1U | 4.200 V   | 4.200 V   | 4.300 V   | 4.200 V                                       | CMOS output        | Active "L"          | (4)                       |

- Remark 1.** Contact our sales office for the products with detection voltage values other than those specified above.
2. Set  $V_{CU} > V_{BU}$ .
  3. Refer to **Table 3** for details about combinations of delay times.

**Table 3**

| Combination of Delay Time | Cell Balancing Detection Delay Time [t <sub>BU</sub> ] | Cell Balancing Release Delay Time [t <sub>BL</sub> ] | Overcharge Detection Delay Time [t <sub>CU</sub> ] | Overcharge Release Delay Time [t <sub>CL</sub> ] |
|---------------------------|--|--|--|--|
| (1)                       | 128 ms   | 1.0 ms   | 128 ms   | 1.0 ms   |
| (2)                       | 128 ms   | 1.0 ms   | 1024 ms  | 1.0 ms   |
| (3)                       | 64 ms  | 2.0 ms   | 256 ms   | 2.0 ms   |
| (4)                       | 64 ms  | 2.0 ms   | 256 ms   | 1.0 ms   |

**Remark** The delay times can be changed within the ranges listed above. For details, please contact our sales office.

**Table 4**

| Delay Time  | Symbol          | Selection Range |                      |                      |        |         | Remark                        |
|---|-----------------|-----------------|----------------------|----------------------|--------|---------|-------------------------------|
| Cell balancing detection delay time <sup>*1</sup> | t <sub>BU</sub> | 64 ms           | 128 ms <sup>*2</sup> | 256 ms               | 512 ms | 1024 ms | Select a value from the left. |
| Cell balancing release delay time                 | t <sub>BL</sub> | 0.5 ms          |                      | 1.0 ms <sup>*2</sup> |        | 2.0 ms  | Select a value from the left. |
| Overcharge detection delay time <sup>*1</sup>     | t <sub>CU</sub> | 64 ms           | 128 ms <sup>*2</sup> | 256 ms               | 512 ms | 1024 ms | Select a value from the left. |
| Overcharge release delay time                     | t <sub>CL</sub> | 0.5 ms          |                      | 1.0 ms <sup>*2</sup> |        | 2.0 ms  | Select a value from the left. |

\*1. Set  $t_{CU} \geq t_{BU}$ .

\*2. The value is the delay time of the standard products.

■ **Pin Configuration**

1. **SOT-23-6**



**Figure 2**

**Table 5**

| Pin No. | Symbol          | Description  |
|---------|-----------------|--|
| 1       | CO              | Output pin for overcharge signal   |
| 2       | VSS             | Input pin for negative power supply  |
| 3       | DP              | Test mode switching pin<br>"H": Test mode (used to shorten the delay time)<br>"L": Normal operation mode |
| 4       | $\overline{CE}$ | Power-saving mode switching pin<br>"H": Power-saving mode<br>"L": Normal operation mode                  |
| 5       | VDD             | Input pin for positive power supply  |
| 6       | CB              | Output pin for cell balancing signal<br>(Nch open-drain output)  |

■ **Absolute Maximum Ratings**

**Table 6**

(Ta = +25°C unless otherwise specified)

| Item                                      | Symbol           | Applied Pin | Absolute Maximum Rating  | Unit |
|---|------------------|-------------|--|------|
| Input voltage between VDD pin and VSS pin | V <sub>DS</sub>  | VDD         | V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 6.0                         | V    |
| Input pin voltage                         | V <sub>IN</sub>  | CE, DP      | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 6.0 | V    |
| Output pin voltage                        | V <sub>OUT</sub> | CO, CB      | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 6.0 | V    |
| Output pin current                        | I <sub>CB</sub>  | CB          | 100 (–40°C to +85°C)   | mA   |
| Operation ambient temperature             | T <sub>opr</sub> | –           | –40 to +85   | °C   |
| Storage temperature                       | T <sub>stg</sub> | –           | –55 to +125  | °C   |

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ **Thermal Resistance Value**

**Table 7**

| Item                                     | Symbol          | Condition | Min.    | Typ. | Max. | Unit |      |
|--|-----------------|-----------|---------|------|------|------|------|
| Junction-to-ambient thermal resistance*1 | θ <sub>JA</sub> | SOT-23-6  | Board A | –    | 159  | –    | °C/W |
|  |                 |           | Board B | –    | 124  | –    | °C/W |
|  |                 |           | Board C | –    | –    | –    | °C/W |
|  |                 |           | Board D | –    | –    | –    | °C/W |
|  |                 |           | Board E | –    | –    | –    | °C/W |

\*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Power Dissipation" and "Test Board" for details.

**■ Electrical Characteristics**

For details about the test circuits and testing method, refer to "■ Test Circuit".

**Caution** Unless otherwise specified in Table 8, set V2 = V3 = 0 V, and SWn (n = 1 to 4) = OFF.

Table 8 (1 / 2)

(Ta = +25°C unless otherwise specified)

| Item  | Symbol   | Condition   | Min.                            | Typ.                    | Max.            | Unit                    |        |
|---|--|---|---------------------------------|-------------------------|-----------------|-------------------------|--------|
| <b>Detection voltage</b>                      |  |   |                                 |                         |                 |                         |        |
| Cell balancing detection voltage              | V <sub>BU</sub>                                | SW1 = ON  | 2.0 V ≤ V <sub>BU</sub> < 2.4 V | V <sub>BU</sub> - 0.012 | V <sub>BU</sub> | V <sub>BU</sub> + 0.012 | V      |
|   |  |   | 2.4 V ≤ V <sub>BU</sub> ≤ 4.6 V | V <sub>BU</sub> × 0.995 | V <sub>BU</sub> | V <sub>BU</sub> × 1.005 | V      |
| Cell balancing release voltage                | V <sub>BL</sub>                                | SW1 = ON  | 2.0 V ≤ V <sub>BL</sub> < 2.4 V | V <sub>BL</sub> - 0.024 | V <sub>BL</sub> | V <sub>BL</sub> + 0.024 | V      |
|   |  |   | 2.4 V ≤ V <sub>BL</sub> ≤ 4.6 V | V <sub>BL</sub> × 0.99  | V <sub>BL</sub> | V <sub>BL</sub> × 1.01  | V      |
| Overcharge detection voltage                  | V <sub>CU</sub>                                | 2.0 V ≤ V <sub>CU</sub> < 2.4 V                         |                                 | V <sub>CU</sub> - 0.012 | V <sub>CU</sub> | V <sub>CU</sub> + 0.012 | V      |
|   |  | 2.4 V ≤ V <sub>CU</sub> ≤ 4.6 V                         |                                 | V <sub>CU</sub> × 0.995 | V <sub>CU</sub> | V <sub>CU</sub> × 1.005 | V      |
| Overcharge release voltage                    | V <sub>CL</sub>                                | 2.0 V ≤ V <sub>CL</sub> < 2.4 V                         |                                 | V <sub>CL</sub> - 0.024 | V <sub>CL</sub> | V <sub>CL</sub> + 0.024 | V      |
|   |  | 2.4 V ≤ V <sub>CL</sub> ≤ 4.6 V                         |                                 | V <sub>CL</sub> × 0.99  | V <sub>CL</sub> | V <sub>CL</sub> × 1.01  | V      |
| <b>Temperature coefficient</b>                |  |   |                                 |                         |                 |                         |        |
| Detection voltage temperature coefficient 1*1 | $\frac{\Delta V_{BU}}{\Delta Ta \cdot V_{BU}}$ | Ta = -40°C to +85°C*3                                   |                                 | -                       | 100             | 350                     | ppm/°C |
| Detection voltage temperature coefficient 2*2 | $\frac{\Delta V_{CU}}{\Delta Ta \cdot V_{CU}}$ | Ta = -40°C to +85°C*3                                   |                                 | -                       | 100             | 350                     | ppm/°C |
| <b>Input voltage</b>                          |  |   |                                 |                         |                 |                         |        |
| Operation voltage between VDD pin and VSS pin | V <sub>DS</sub>                                | Voltages output from CO pin and CB pin are fixed        |                                 | 1.5                     | -               | 5.0                     | V      |
| CE pin voltage "H"                            | V <sub>CEH</sub>                               | -   |                                 | -                       | -               | V <sub>DD</sub> × 0.9   | V      |
| CE pin voltage "L"                            | V <sub>CEL</sub>                               | -   |                                 | V <sub>DD</sub> × 0.1   | -               | -                       | V      |
| DP pin voltage "H"                            | V <sub>DPH</sub>                               | -   |                                 | -                       | -               | V <sub>DD</sub> × 0.9   | V      |
| DP pin voltage "L"                            | V <sub>DPL</sub>                               | -   |                                 | V <sub>DD</sub> × 0.1   | -               | -                       | V      |
| <b>Input current</b>                          |  |   |                                 |                         |                 |                         |        |
| Current consumption during operation          | I <sub>OPE</sub>                               | I <sub>VDD</sub> when V1 = V <sub>BL</sub> - 0.1 V      |                                 | -                       | 1.2             | 2.0                     | μA     |
| Current consumption during power-saving       | I <sub>PSV</sub>                               | I <sub>VDD</sub> when V1 = V2 = V <sub>BL</sub> - 0.1 V |                                 | -                       | -               | 0.1                     | μA     |

\*1. A change in the temperature of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta V_{BU}}{\Delta Ta} [\text{mV}/^\circ\text{C}] = V_{BU} [\text{V}] \times \frac{\Delta V_{BU}}{\Delta Ta \cdot V_{BU}} [\text{ppm}/^\circ\text{C}] \div 1000$$

\*2. A change in the temperature of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta V_{CU}}{\Delta Ta} [\text{mV}/^\circ\text{C}] = V_{CU} [\text{V}] \times \frac{\Delta V_{CU}}{\Delta Ta \cdot V_{CU}} [\text{ppm}/^\circ\text{C}] \div 1000$$

\*3. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

**Remark 1.**  $\frac{\Delta V_{BU}}{\Delta Ta}, \frac{\Delta V_{CU}}{\Delta Ta}$ : Change in temperature of detection voltage

2. V<sub>BU</sub>, V<sub>CU</sub>: Set detection voltage

3.  $\frac{\Delta V_{BU}}{\Delta Ta \cdot V_{BU}}, \frac{\Delta V_{CU}}{\Delta Ta \cdot V_{CU}}$ : Detection voltage temperature coefficient

**Table 8 (2 / 2)**

(Ta = +25°C unless otherwise specified)

| Item  | Symbol            | Condition   | Min.                  | Typ.            | Max.                  | Unit |
|---|-------------------|---|-----------------------|-----------------|-----------------------|------|
| <b>Delay time</b>   |                   |   |                       |                 |                       |      |
| Cell balancing detection delay time   | t <sub>BU</sub>   | –   | t <sub>BU</sub> × 0.8 | t <sub>BU</sub> | t <sub>BU</sub> × 1.2 | ms   |
| Cell balancing release delay time   | t <sub>BL</sub>   | –   | t <sub>BL</sub> × 0.8 | t <sub>BL</sub> | t <sub>BL</sub> × 1.2 | ms   |
| Overcharge detection delay time   | t <sub>CU</sub>   | –   | t <sub>CU</sub> × 0.8 | t <sub>CU</sub> | t <sub>CU</sub> × 1.2 | ms   |
| Overcharge release delay time   | t <sub>CL</sub>   | –   | t <sub>CL</sub> × 0.8 | t <sub>CL</sub> | t <sub>CL</sub> × 1.2 | ms   |
| <b>Output current</b>   |                   |   |                       |                 |                       |      |
| <b>CB pin output current</b>  |                   |   |                       |                 |                       |      |
| CB pin sink current   | I <sub>CBS</sub>  | V1 = V <sub>BU</sub> + 0.1 V, SW2 = ON, V4 = 0.5 V      | 30                    | –               | –                     | mA   |
| CB pin leakage current  | I <sub>CBL</sub>  | V1 = V <sub>BL</sub> – 0.1 V, SW2 = ON, V4 = 6.0 V      | –                     | –               | 0.1                   | μA   |
| <b>CO pin output current (output form: CMOS output, output logic: active "H")</b>           |                   |   |                       |                 |                       |      |
| CO pin sink current   | I <sub>COL</sub>  | V1 = V <sub>CL</sub> – 0.1 V, SW4 = ON, V5 = 0.5 V      | 5.0                   | –               | –                     | mA   |
| CO pin source current   | I <sub>COH</sub>  | V1 = V <sub>CU</sub> + 0.1 V, SW4 = ON, V5 = V1 – 0.5 V | 1.0                   | –               | –                     | mA   |
| <b>CO pin output current (output form: CMOS output, output logic: active "L")</b>           |                   |   |                       |                 |                       |      |
| CO pin sink current   | I <sub>COL</sub>  | V1 = V <sub>CU</sub> + 0.1 V, SW4 = ON, V5 = 0.5 V      | 5.0                   | –               | –                     | mA   |
| CO pin source current   | I <sub>COH</sub>  | V1 = V <sub>CL</sub> – 0.1 V, SW4 = ON, V5 = V1 – 0.5 V | 1.0                   | –               | –                     | mA   |
| <b>CO pin output current (output form: Nch open-drain output, output logic: active "H")</b> |                   |   |                       |                 |                       |      |
| CO pin sink current   | I <sub>COL</sub>  | V1 = V <sub>CL</sub> – 0.1 V, SW4 = ON, V5 = 0.5 V      | 5.0                   | –               | –                     | mA   |
| CO pin leakage current  | I <sub>COHL</sub> | V1 = V <sub>CU</sub> + 0.1 V, SW4 = ON, V5 = 6.0 V      | –                     | –               | 0.1                   | μA   |
| <b>CO pin output current (output form: Nch open-drain output, output logic: active "L")</b> |                   |   |                       |                 |                       |      |
| CO pin sink current   | I <sub>COL</sub>  | V1 = V <sub>CU</sub> + 0.1 V, SW4 = ON, V5 = 0.5 V      | 5.0                   | –               | –                     | mA   |
| CO pin leakage current  | I <sub>COHL</sub> | V1 = V <sub>CL</sub> – 0.1 V, SW4 = ON, V5 = 6.0 V      | –                     | –               | 0.1                   | μA   |



■ Test Circuit

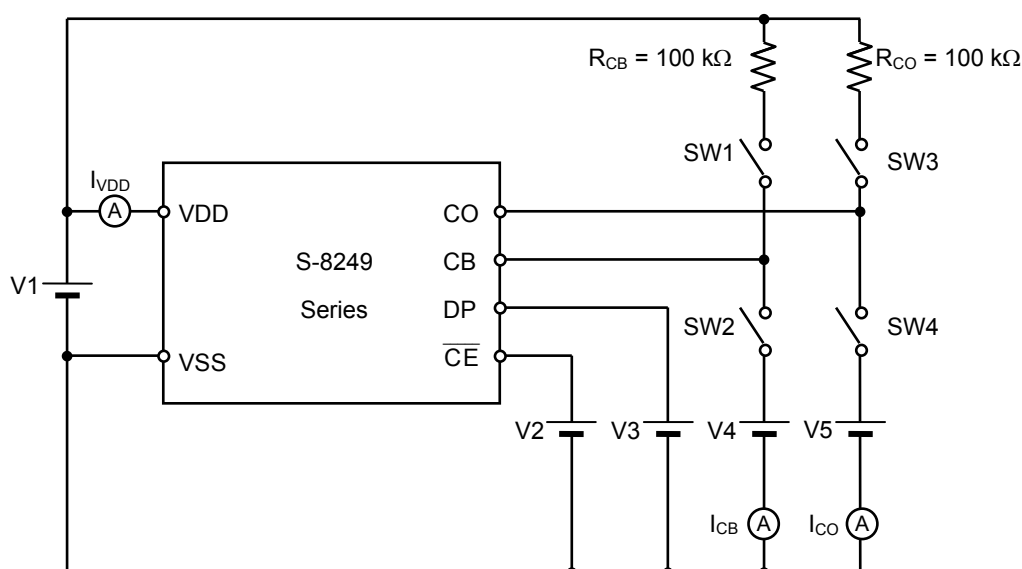


Figure 3

**Caution** Unless otherwise specified in Table 8, set  $V2 = V3 = 0\text{ V}$ , and  $SWn$  ( $n = 1$  to  $4$ ) = OFF.

**1.  $\overline{CE}$  pin voltage "H"**

$\overline{CE}$  pin voltage "H" ( $V_{\overline{CE}H}$ ) is defined as the voltage at which  $I_{VDD}$  is changed from  $I_{OPE}$  to  $I_{PSV}$  when  $V2$  is increased from  $0\text{ V}$  after setting  $V1 = V_{BL} - 0.1\text{ V}$ .

**2.  $\overline{CE}$  pin voltage "L"**

$\overline{CE}$  pin voltage "L" ( $V_{\overline{CE}L}$ ) is defined as the voltage at which  $I_{VDD}$  is changed from  $I_{PSV}$  to  $I_{OPE}$  when  $V2$  is decreased from  $V_{BL} - 0.1\text{ V}$  after setting  $V1 = V2 = V_{BL} - 0.1\text{ V}$ .

**3. DP pin voltage "H"\*1**

DP pin voltage "H" ( $V_{DPH}$ ) is defined as the voltage at which the test mode is switched when  $V3$  is increased from  $0\text{ V}$  after setting  $V1 = V_{BL} - 0.1\text{ V}$ .

**4. DP pin voltage "L"\*1**

DP pin voltage "L" ( $V_{DPL}$ ) is defined as the voltage at which the normal operation mode is switched when  $V3$  is decreased from  $V_{BL} - 0.1\text{ V}$  after setting  $V1 = V3 = V_{BL} - 0.1\text{ V}$ .

**5. Cell balancing detection delay time**

Cell balancing detection delay time ( $t_{BU}$ ) is defined as the time from when  $SW1$  is set to ON and  $V1$  is set to  $V_{BU} - 0.1\text{ V}$  to when the CB pin output is inverted after setting  $V1$  to  $V_{BU} + 0.1\text{ V}$ .

**6. Cell balancing release delay time**

Cell balancing release delay time ( $t_{BL}$ ) is defined as the time from when  $SW1$  is set to ON and  $V1$  is set to  $V_{BL} + 0.1\text{ V}$  to when the CB pin output is inverted after setting  $V1$  to  $V_{BL} - 0.1\text{ V}$ .

**7. Overcharge detection delay time**

Overcharge detection delay time ( $t_{CU}$ ) is defined as the time from when  $SW1$  is set to ON and  $V1$  is set to  $V_{CU} - 0.1\text{ V}$  to when the CO pin output is inverted after setting  $V1$  to  $V_{CU} + 0.1\text{ V}$ .

**8. Overcharge release delay time**

Overcharge release delay time ( $t_{CL}$ ) is defined as the time from when  $SW1$  is set to ON and  $V1$  is set to  $V_{CL} + 0.1\text{ V}$  to when the CO pin output is inverted after setting  $V1$  to  $V_{CL} - 0.1\text{ V}$ .

\*1. For details about switching to the test mode by using the DP pin, refer to "5. DP pin" in "■ Operation".

■ Standard Circuit



Figure 4

Table 9 Constants for External Components

| Symbol    | Part      | Purpose                                       | Min.          | Typ.         | Max.           | Remark   |
|-----------|-----------|---|---------------|--------------|----------------|--|
| $R_{VDD}$ | Resistor  | ESD protection, for power fluctuation control | 150 $\Omega$  | 330 $\Omega$ | 1.0 k $\Omega$ | Resistance should be as small as possible to avoid worsening the overcharge detection accuracy due to current consumption.*1 |
| $C_{VDD}$ | Capacitor | For power fluctuation control                 | 0.068 $\mu$ F | 0.1 $\mu$ F  | 1.0 $\mu$ F    | Connect a capacitor of 0.068 $\mu$ F or more between VDD pin and VSS pin.*1  |
| $R_{CB}$  | Resistor  | For setting the cell balancing current value  | —             | —            | —              | Set the required cell balancing current value depending on "2. Cell balancing status" in "■ Operation".*2                    |

\*1. When connecting a resistor less than 150  $\Omega$  to  $R_{VDD}$  or a capacitor less than 0.068  $\mu$ F to  $C_{VDD}$ , the S-8249 Series may malfunction when power is largely fluctuated.

\*2. Set the cell balancing current value so that  $R_{CB}$  does not exceed the power dissipation.

**Cautions 1. The above constants may be changed without notice.**

**2. The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.**

■ Operation

**Remark** Refer to "■ Standard Circuit".

1. Normal status

In the S-8249 Series, if the voltage between the VDD pin and the VSS pin ( $V_{DS}$ ) has not reached the cell balancing detection voltage ( $V_{BU}$ ), the CB pin output is in the high-impedance status. The CO pin output status varies according to the output form and output logic selected, as shown in **Table 10**. This is the normal status.

Table 10

| CO Pin Output Form and Output Logic | CB Pin Output | CO Pin Output |
|-------------------------------------|---------------|---------------|
| CMOS output, active "H"             | "H"           | "L"           |
| CMOS output, active "L"             | "H"           | "H"           |
| Nch open-drain output, active "H"   | "H"           | "L"           |
| Nch open-drain output, active "L"   | "H"           | "H"           |

2. Cell balancing status

In the S-8249 Series, if  $V_{DS}$  is  $V_{BU}$  or higher and this status continues for the cell balancing detection delay time ( $t_{BU}$ ) or longer, the CB pin output becomes "L". This is the cell balancing status.

The cell balancing status is released when  $V_{DS}$  drops to the cell balancing release voltage ( $V_{BL}$ ) or lower and this status continues for the cell balancing release delay time ( $t_{BL}$ ) or longer.

The S-8249 Series includes an Nch transistor with ON resistance of  $5\ \Omega$  typ. ( $R_{CBON}$ ) between the CB pin and the VSS pin, thus causing the cell balancing current ( $I_{CB}$ ) to flow in cell balancing status, and the cell balancing operation to start.

By connecting a resistor ( $R_{CB}$ ) to the CB pin,  $I_{CB}$  in cell balancing status can be calculated by using the following equation.

$$I_{CB} = V_{BU} / (R_{CBON} + R_{CB})$$

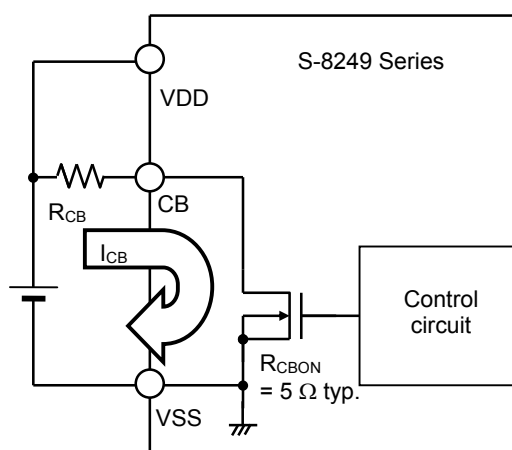


Figure 5

**3. Overcharge status**

In the S-8249 Series, if  $V_{DS}$  is the overcharge detection voltage ( $V_{CU}$ ) or higher and this status continues for the overcharge detection delay time ( $t_{CU}$ ) or longer, the CO pin output is inverted. The CO pin output status varies according to the output form and output logic selected, as shown in **Table 11**. This is the overcharge status. In the overcharge status, the CB pin output becomes "L".

**Table 11**

| CO Pin Output Form and Output Logic | CB Pin Output | CO Pin Output |
|-------------------------------------|---------------|---------------|
| CMOS output, active "H"             | "L"           | "H"           |
| CMOS output, active "L"             | "L"           | "L"           |
| Nch open-drain output, active "H"   | "L"           | "H"           |
| Nch open-drain output, active "L"   | "L"           | "L"           |

The overcharge status is released when  $V_{DS}$  drops to the overcharge release voltage ( $V_{CL}$ ) or lower and this status continues for the overcharge release delay time ( $t_{CL}$ ) or longer.

**4.  $\overline{CE}$  pin**

The S-8249 Series has the  $\overline{CE}$  pin (Power-saving mode switching pin). The S-8249 Series is set to power-saving mode by inputting a voltage of  $V_{\overline{CEH}}$  or higher to the  $\overline{CE}$  pin.

**Table 12**

| $\overline{CE}$ Pin                                 | Status                |
|---|-----------------------|
| Open ( $V_{\overline{CE}} = V_{SS}$ )               | Normal operation mode |
| "H" ( $V_{\overline{CE}} \geq V_{\overline{CEH}}$ ) | Power-saving mode     |
| "L" ( $V_{\overline{CE}} \leq V_{\overline{CEL}}$ ) | Normal operation mode |

In power-saving mode, the current consumption is decreased to current consumption during power-saving ( $I_{PSV}$ ). The CB pin or the CO pin output in power-saving mode is the same as that in the normal status.

The  $\overline{CE}$  pin is pulled down to  $V_{SS}$  by the internal resistor. When in a mode other than power-saving mode, leave the  $\overline{CE}$  pin open or short it with  $V_{SS}$ .

### 5. DP pin

The S-8249 Series has the DP pin (Test mode switching pin). The S-8249 Series is set to test mode (used to shorten the delay time) by inputting a voltage of  $V_{DPH}$  or higher to the DP pin.

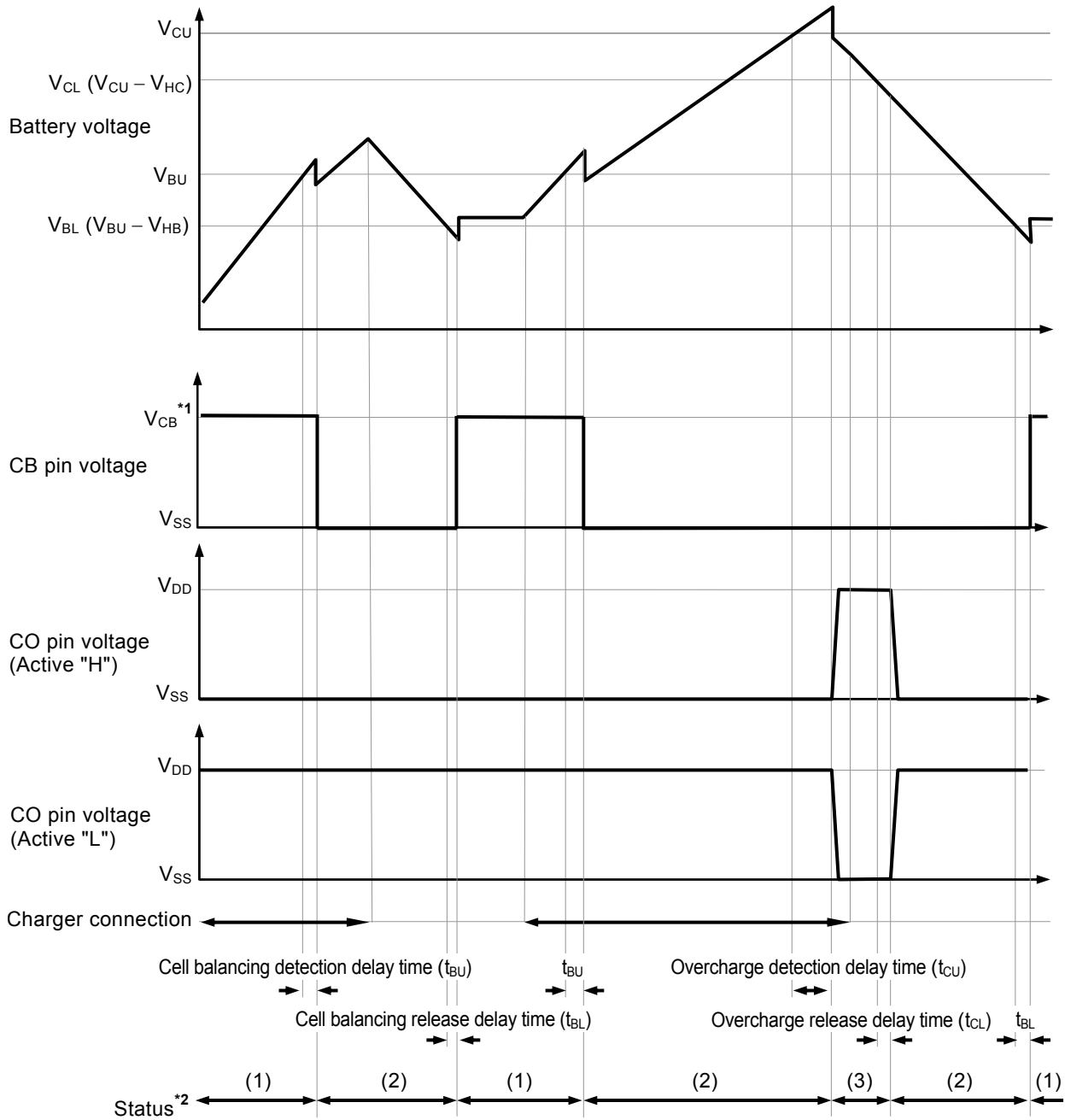
**Table 13**

| DP Pin                        | Status                |
|-------------------------------|-----------------------|
| Open ( $V_{DP} = V_{SS}$ )    | Normal operation mode |
| "H" ( $V_{DP} \geq V_{DPH}$ ) | Test mode             |
| "L" ( $V_{DP} \leq V_{DPL}$ ) | Normal operation mode |

In test mode, the cell balancing detection delay time ( $t_{BU}$ ) and overcharge detection delay time ( $t_{CU}$ ) are shortened to 1/64 of the delay time in the normal operation mode.

The DP pin is pulled down to  $V_{SS}$  by the internal resistor. When in a mode other than test mode, leave the DP pin open or short it with  $V_{SS}$ .

■ Timing Chart



\*1. The CB pin is pulled up by the external resistor.

\*2. (1): Normal status  
(2): Cell balancing status  
(3): Overcharge status

**Remark** The charger is assumed to charge with a constant current.

Figure 6

## ■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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■ **Characteristics (Typical Data)**

**1. Current consumption**

**1.1  $I_{OPE}$  vs.  $T_a$**



**1.2  $I_{PSV}$  vs.  $T_a$**



**1.3  $I_{OPE}$  vs.  $V_{DD}$**



**2. Cell balancing detection / release voltage, overcharge detection / release voltage and delay times**

**2.1  $V_{BU}$  vs.  $T_a$**



**2.2  $V_{BL}$  vs.  $T_a$**



**2.3  $V_{CU}$  vs.  $T_a$**

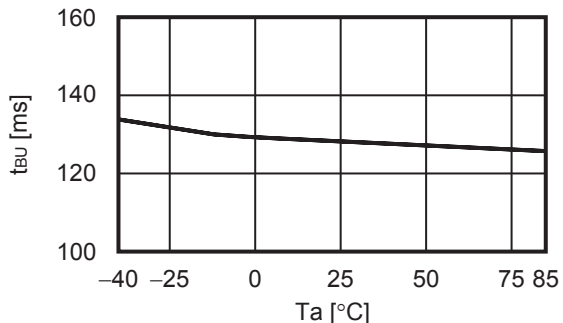


**2.4  $V_{CL}$  vs.  $T_a$**

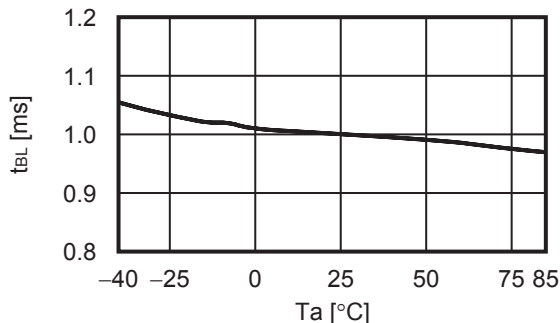




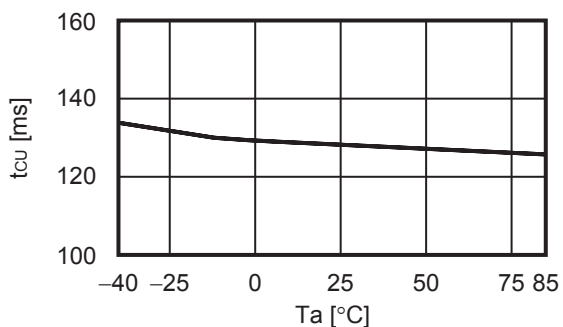
2.5  $t_{BU}$  vs.  $T_a$



2.6  $t_{BL}$  vs.  $T_a$



2.7  $t_{CU}$  vs.  $T_a$

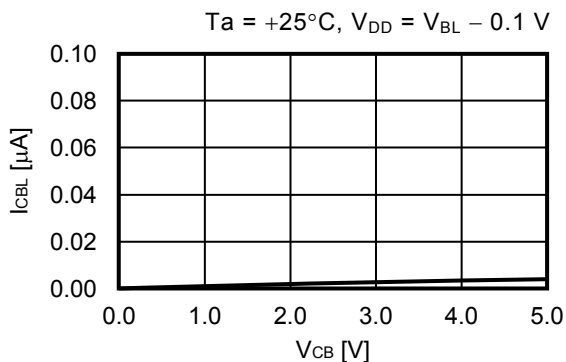


2.8  $t_{CL}$  vs.  $T_a$



3. Output current

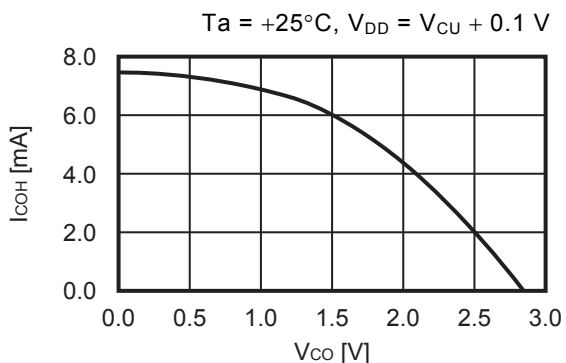
3.1  $I_{CBL}$  vs.  $V_{CB}$



3.2  $I_{CBS}$  vs.  $V_{CB}$



3.3  $I_{COH}$  vs.  $V_{CO}$



3.4  $I_{COL}$  vs.  $V_{CO}$



■ **Power Dissipation**

SOT-23-6



| Board | Power Dissipation ( $P_D$ ) |
|-------|-----------------------------|
| A     | 0.63 W                      |
| B     | 0.81 W                      |
| C     | —                           |
| D     | —                           |
| E     | —                           |

# SOT-23-3/3S/5/6 Test Board

 IC Mount Area

(1) Board A



| Item                        | Specification       |   |
|-----------------------------|---------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |   |
| Material                    | FR-4                |   |
| Number of copper foil layer | 2                   |   |
| Copper foil layer [mm]      | 1                   | Land pattern and wiring for testing: t0.070 |
|                             | 2                   | -   |
|                             | 3                   | -   |
|                             | 4                   | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | -                   |   |

(2) Board B



| Item                        | Specification       |   |
|-----------------------------|---------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |   |
| Material                    | FR-4                |   |
| Number of copper foil layer | 4                   |   |
| Copper foil layer [mm]      | 1                   | Land pattern and wiring for testing: t0.070 |
|                             | 2                   | 74.2 x 74.2 x t0.035                        |
|                             | 3                   | 74.2 x 74.2 x t0.035                        |
|                             | 4                   | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | -                   |   |

No. SOT23x-A-Board-SD-2.0



No. MP006-A-P-SD-2.1

|                   |                         |
|-------------------|-------------------------|
| TITLE             | SOT236-A-PKG Dimensions |
| No.               | MP006-A-P-SD-2.1        |
| ANGLE             |                         |
| UNIT              | mm                      |
|                   |                         |
| <b>ABLIC Inc.</b> |                         |



No. MP006-A-C-SD-3.1

|                   |                       |
|-------------------|-----------------------|
| TITLE             | SOT236-A-Carrier Tape |
| No.               | MP006-A-C-SD-3.1      |
| ANGLE             |                       |
| UNIT              | mm                    |
| <b>ABLIC Inc.</b> |                       |



Enlarged drawing in the central part



No. MP006-A-R-SD-2.1

|                   |                  |     |       |
|-------------------|------------------|-----|-------|
| TITLE             | SOT236-A-Reel    |     |       |
| No.               | MP006-A-R-SD-2.1 |     |       |
| ANGLE             |                  | QTY | 3,000 |
| UNIT              | mm               |     |       |
|                   |                  |     |       |
| <b>ABLIC Inc.</b> |                  |     |       |

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