



N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$ (Max.)	I _D (A) ^{a, g}	Q _g (Typ.)		
30	0.0043 at V _{GS} = 10 V	25	13.6 nC		
	0.0060 at V _{GS} = 4.5 V	25	13.0110		

PowerPAK® SO-8 6.15 mm **Bottom View**

Ordering Information: SiRA12DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

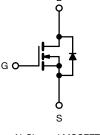
FEATURES

- Halogen-free According to IEC 61249-2-21 **Definition**
- TrenchFET® Gen IV Power MOSFET
- 100 % R_{α} and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

COMPLIANT HALOGEN FREE

APPLICATIONS

- High Power Density DC/DC
- Synchronous Rectification
- VRMs and Embedded DC/DC



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	S (T _A = 25 °C, unle	ess otherwise no	oted)		
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V_{DS}	30	V		
Gate-Source Voltage	V_{GS}	+ 20, - 16	v		
	T _C = 25 °C		25 ^g		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C	I_	25 ^g		
Continuous Brain Guirent (1) = 130 °C)	T _A = 25 °C	I _D	25 ^{b, c, g}		
	T _A = 70 °C		20 ^{b, c}	Α	
Pulsed Drain Current (t = 300 μs)	I _{DM}	80	7		
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	25 ^g		
Continuous Source-Drain Diode Guirent	T _A = 25 °C	'S	3.8 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	15		
Single Pulse Avalanche Energy	L = 0.1 IIII1	E _{AS}	11	mJ	
	T _C = 25 °C		31		
Maximum Power Dissipation	T _C = 70 °C	P _D	20	w	
Maximum Fower Dissipation	T _A = 25 °C	' D	4.5 ^{b, c}		
	T _A = 70 °C		2.9 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature		260	\exists		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	25	28	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	3.2	4	O/ VV	

Notes:

- a. Based on $T_C = 25$ °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 70 °C/W.
- g. Package limited.



SPECIFICATIONS ($T_J = 25 ^{\circ}\text{C}$,		· · · · · · · · · · · · · · · · · · ·	. ne:	T =			
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			1	1		I	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		16		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	5 .		- 5		,	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1.1		2.2	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20, -16 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1 μΔ		
Zero date voltage Drain Gurrent	טאטי	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	- μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	25			Α	
Durin Course On Olate Basistana 3	D	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		0.0032	0.0043	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$		0.0044	0.0060		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 10 A		51		S	
Dynamic ^b			<u>'</u>	_	•	L	
Input Capacitance	C _{iss}			2070		pF	
Output Capacitance	C _{oss}	V 45.V.V 6.V.C 4.M.V		600			
Reverse Transfer Capacitance	C _{rss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		51			
C _{rss} /C _{iss} Ratio				0.025	0.050		
	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A		29.5	45		
Total Gate Charge				13.6	21		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		5.2		nC	
Gate-Drain Charge	Q _{gd}	20 40 2		2.6			
Output Charge	Q _{oss}	V _{DS} = 15 V, V _{GS} = 0 V		16			
Gate Resistance	R _g	f = 1 MHz	0.3	1.7	3.4	Ω	
Turn-On Delay Time	t _{d(on)}			10	20		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_1 = 1.5 \Omega$		10	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		25	50		
Fall Time	t _f	· ·		10	20		
Turn-On Delay Time	t _{d(on)}			20	40	ns	
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$		15	30		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		22	45		
Fall Time	t _f	_		10	20		
Drain-Source Body Diode Characteristic						I	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			25		
Pulse Diode Forward Current ^a	I _{SM}	.0 _0 0			80	Α	
Body Diode Voltage	V _{SD}	I _S = 10 A		0.86	1.2	V	
Body Diode Reverse Recovery Time	1	19 - 1071		27	55	-	
<u> </u>	t _{rr}	I_ = 10 A dl/dt = 100 A/us		-		ns nC	
Body Diode Reverse Recovery Charge Reverse Recovery Fall Time	+	$I_F = 10 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s,}$ $T_J = 25 ^{\circ}\text{C}$		15	30	nC ns	
	t _a	., - 20 0		13	-		
Reverse Recovery Rise Time	t _b			14			

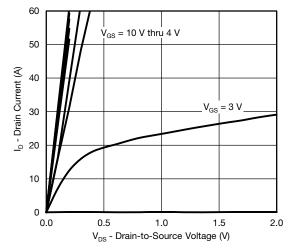
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

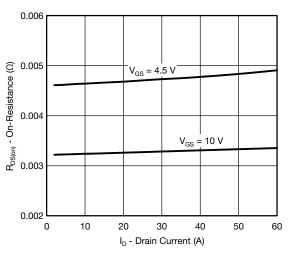
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



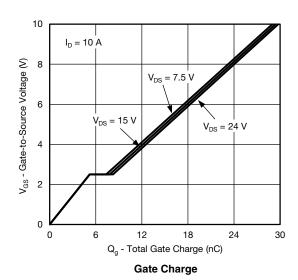
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

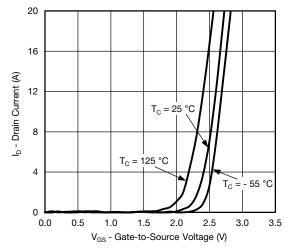


Output Characteristics

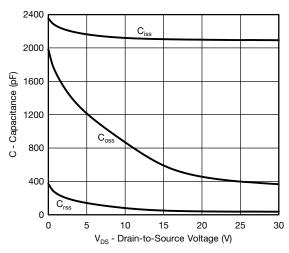


On-Resistance vs. Drain Current

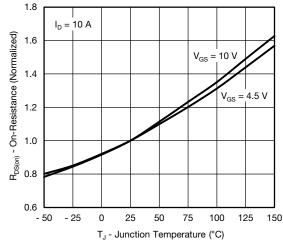




Transfer Characteristics



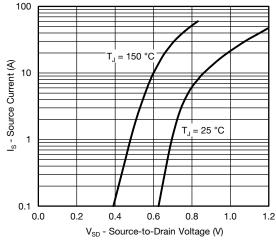
Capacitance

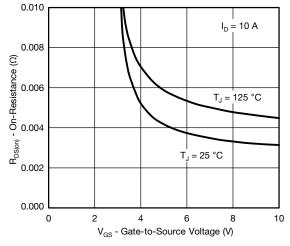


On-Resistance vs. Junction Temperature

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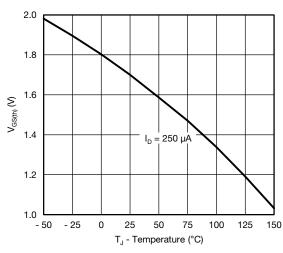
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

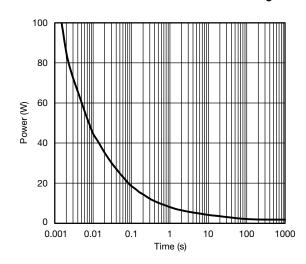




Source-Drain Diode Forward Voltage

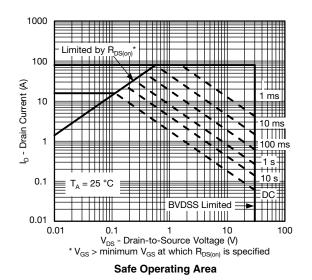
On-Resistance vs. Gate-to-Source Voltage





Threshold Voltage

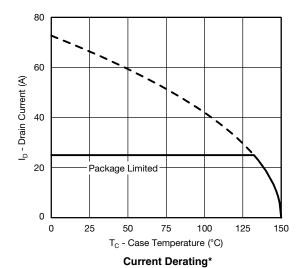
Single Pulse Power, Junction-to-Ambient

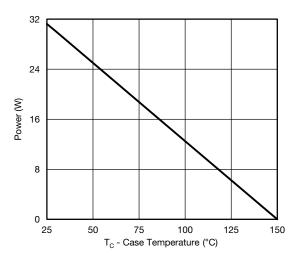






TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



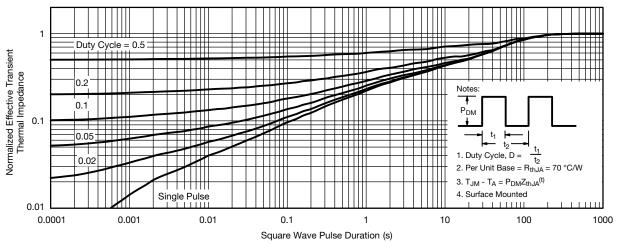


Power, Junction-to-Case

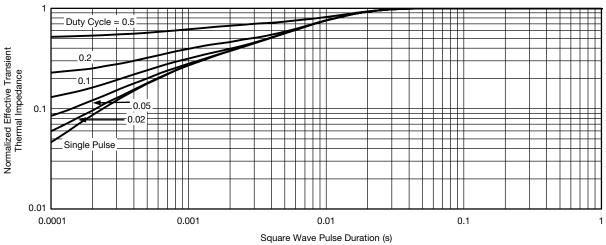
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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