6A Austin MicroLynx II™: SIP Non-Isolated DC-DC Power Module

2.4Vdc –5.5Vdc input; 0.75Vdc to 3.63Vdc output; 6A Output Current

D O S A
Distributed-power
Open Standards Alliance

RoHS Compliant

EZ-SEQUENCE™

Applications

- Distributed power architectures
- Intermediate bus voltage applications
- Telecommunications equipment
- Servers and storage applications
- Networking equipment
- Enterprise Networks
- Latest generation IC's (DSP, FPGA, ASIC) and Microprocessor powered applications

Features

- Compliant to RoHS EU Directive 2011/65/EU (-Z versions)
- Compliant to RoHS EU Directive 2011/65/EU under exemption 7b (Lead solder exemption). Exemption 7b will expire after June 1, 2016 at which time this product will no longer be RoHS compliant (non-Z versions)
- Flexible output voltage sequencing EZ-SEQUENCE™
- Delivers up to 6A output current
- High efficiency – 96% at 3.3V full load (V_{IN} = 5.0V)
- Small size and low profile:

  25.4 mm × 12.7mm × 6.68 mm

  (1.00 in × 0. 5 in × 0.263 in)
- Low output ripple and noise
- High Reliability:

  Calculated MTBF = 12.8M hours at 25°C Full-load
- Programmable Output voltage
- Line Regulation: 0.3% (typical)
- Load Regulation: 0.4% (typical)
- Temperature Regulation: 0.4 % (typical)
- Remote On/Off
- Output overcurrent protection (non-latching)
- Wide operating temperature range (-40°C to 85°C)
- *UL** 60950-1Recognized, *CSA*† C22.2 No. 60950-1-03 Certified, and *VDE*‡ 0805:2001-12 (EN60950-1) Licensed
- ISO** 9001 and ISO 14001 certified manufacturing facilities

Description

Austin MicroLynx™ II SIP power modules are non-isolated dc-dc converters that can deliver up to 6A of output current with full load efficiency of 96.0% at 3.3V output. These modules provide a precisely regulated output voltage programmable via an external resistor from 0.75Vdc to 3.63Vdc over a wide range of input voltage (V_{IN} = 2.4 – 5.5Vdc). Austin MicroLynx™ II has a sequencing feature, EZ-SEQUENCE™ that enable designers to implement various types of output voltage sequencing when powering multiple modules on board. Their open-frame construction and small footprint enable designers to develop cost- and space-efficient solutions. In addition to sequencing, standard features include remote On/Off, programmable output voltage and over current protection.

* *UL* is a registered trademark of Underwriters Laboratories, Inc.

† *CSA* is a registered trademark of Canadian Standards Association.

‡ *VDE* is a trademark of Verband Deutscher Elektrotechniker e.V.

** ISO is a registered trademark of the International Organization of Standards

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Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Device	Symbol	Min	Max	Unit
Input Voltage Continuous	All	V_{IN}	-0.3	5.8	Vdc
Sequencing voltage	All	Vseq	-0.3	$V_{IN,max}$	Vdc
Operating Ambient Temperature (see Thermal Considerations section)	All	T_A	-40	85	°C
Storage Temperature	All	T_{stg}	-55	125	°C

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions.

Parameter	Device	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$V_{O,set} \leq 3.63$	V_{IN}	2.4	—	5.5	Vdc
Maximum Input Current ($V_{IN}= V_{IN, min}$ to $V_{IN, max}$, $I_O=I_{O, max}$)	All	$I_{IN,max}$			6.0	Adc
Input No Load Current	$V_{O,set} = 0.75$ Vdc	$I_{IN,No load}$		20		mA
($V_{IN} = V_{IN, nom}$, Io = 0, module enabled)	$V_{O,set} = 3.3$Vdc	$I_{IN,No load}$		45		mA
Input Stand-by Current ($V_{IN} = V_{IN, nom}$, module disabled)	All	$I_{IN,stand-by}$		0.6		mA
Inrush Transient	All	I^2t			0.04	A^2s
Input Reflected Ripple Current, peak-to-peak (5Hz to 20MHz, 1μH source impedance; $V_{IN, min}$ to $V_{IN, max}$, $I_O= I_{Omax}$; See Test configuration section)	All			35		mAp-p
Input Ripple Rejection (120Hz)	All			30		dB

CAUTION: This power module is not internally fused. An input line fuse must always be used.

This power module can be used in a wide variety of applications, ranging from simple standalone operation to being part of a complex power architecture. To preserve maximum flexibility, internal fusing is not included, however, to achieve maximum safety and system protection, always use an input line fuse. The safety agencies require a fast-acting fuse with a maximum rating of 6 A (see Safety Considerations section). Based on the information provided in this data sheet on inrush energy and maximum dc input current, the same type of fuse with a lower rating can be used. Refer to the fuse manufacturer's data sheet for further information.

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Electrical Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
Output Voltage Set-point ($V_{IN}=_{IN, min}$, $I_O=I_{O, max}$, T_A=25°C)	All	$V_{O, set}$	-2.0	—	+2.0	% $V_{O, set}$
Output Voltage (Over all operating input voltage, resistive load, and temperature conditions until end of life)	All	$V_{O, set}$	–3.0	—	+3.0	% $V_{O, set}$
Adjustment Range Selected by an external resistor	All	V_O	0.7525		3.63	Vdc
Output Regulation						
Line ($V_{IN}=V_{IN, min}$ to $V_{IN, max}$)	All		—	0.3	—	% $V_{O, set}$
Load ($I_O=I_{O, min}$ to $I_{O, max}$)	All		—	0.4	—	% $V_{O, set}$
Temperature ($T_{ref}=T_{A, min}$ to $T_{A, max}$)	All		—	0.4	—	% $V_{O, set}$
Output Ripple and Noise on nominal output ($V_{IN}=V_{IN, nom}$ and $I_O=I_{O, min}$ to $I_{O, max}$ Cout = 1µF ceramic//10µFtantalum capacitors)						
RMS (5Hz to 20MHz bandwidth)	All		—	10	15	mV_{rms}
Peak-to-Peak (5Hz to 20MHz bandwidth)	All		—	40	50	mV_{pk-pk}
External Capacitance						
ESR ≥ 1 mΩ	All	$C_{O, max}$	—	—	1000	µF
ESR ≥ 10 mΩ	All	$C_{O, max}$	—	—	3000	µF
Output Current	All	I_O	0		6	Adc
Output Current Limit Inception (Hiccup Mode) (V_O= 90% of $V_{O, set}$)	All	$I_{O, lim}$	—	220	—	% I_O
Output Short-Circuit Current (V_O≤250mV) (Hiccup Mode)	All	$I_{O, s/c}$	—	2	—	Adc
Efficiency	$V_{O, set}$ = 0.75Vdc	η		81.0		%
V_{IN}= $V_{IN, nom}$, T_A=25°C	$V_{O, set}$ = 1.2Vdc	η		87.0		%
$I_O=I_{O, max}$, V_O= $V_{O,set}$	$V_{O,set}$ = 1.5Vdc	η		89.0		%
	$V_{O,set}$ = 1.8Vdc	η		90.0		%
	$V_{O,set}$ = 2.5Vdc	η		93.0		%
	$V_{O,set}$ = 3.3Vdc	η		96.0		%
Switching Frequency	All	f_{sw}	—	300	—	kHz
Dynamic Load Response						
(dIo/dt=2.5A/µs; V_{IN} = $V_{IN, nom}$; T_A=25°C) Load Change from Io= 50% to 100% of Io,max; 1µF ceramic// 10 µF tantalum Peak Deviation	All	V_{pk}	—	130	—	mV
Settling Time (Vo<10% peak deviation)	All	t_s	—	25	—	µs
(dIo/dt=2.5A/µs; V_{IN} = $V_{IN, nom}$; T_A=25°C) Load Change from Io= 100% to 50%of Io,max: 1µF ceramic// 10 µF tantalum Peak Deviation	All	V_{pk}	—	130	—	mV
Settling Time (Vo<10% peak deviation)	All	t_s	—	25	—	µs

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Electrical Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
Dynamic Load Response						
(dIo/dt=2.5A/μs; V V_{IN} = $V_{IN, nom}$; T_A=25°C) Load Change from Io= 50% to 100% of Io,max; Co = 2×150 μF polymer capacitors Peak Deviation	All	V_{pk}	—	50	—	mV
Settling Time (Vo<10% peak deviation)	All	t_s	—	50	—	μs
(dIo/dt=2.5A/μs; V_{IN} = $V_{IN, nom}$; T_A=25°C) Load Change from Io= 100% to 50%of Io,max: Co = 2×150 μF polymer capacitors Peak Deviation	All	V_{pk}	—	50	—	mV
Settling Time (Vo<10% peak deviation)	All	t_s	—	50	—	μs

General Specifications

Parameter	Min	Typ	Max	Unit
Calculated MTBF ($I_O=I_{O, max}$, T_A=25°C) per Telecordia SR-332 Issue 1: Method 1 Case 3		12,841,800		Hours
Weight	—	2.8 (0.1)	—	g (oz.)

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Feature Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Device	Symbol	Min	Typ	Max	Unit
On/Off Signal interface						
Device code with Suffix "4" – Positive logic						
(On/Off is open collector/drain logic input;						
Signal referenced to GND - See feature description section)						
Input High Voltage (Module ON)	All	V_{IH}	—	—	$V_{IN, max}$	V
Input High Current	All	I_{IH}	—	—	10	µA
Input Low Voltage (Module OFF)	All	V_{IL}	-0.2	—	0.3	V
Input Low Current	All	I_{IL}	—	0.2	1	mA
Device Code with no suffix – Negative Logic						
(On/OFF pin is open collector/drain logic input with						
external pull-up resistor; signal referenced to GND)						
Input High Voltage (Module OFF)	All	V_{IH}	1.5	—	$V_{IN,max}$	Vdc
Input High Current	All	I_{IH}		0.2	1	mA
Input Low Voltage (Module ON)	All	V_{IL}	-0.2	—	0.3	Vdc
Input low Current	All	I_{IL}		—	10	µA
Turn-On Delay and Rise Times						
($I_O=I_{O, max}$, $V_{IN} = V_{IN, nom}$, $T_A = 25$ ºC,)						
Case 1: On/Off input is set to Logic Low (Module ON) and then input power is applied (delay from instant at which $V_{IN} = V_{IN, min}$ until Vo=10% of Vo,set)	All	Tdelay	—	3.9	—	msec
Case 2: Input power is applied for at least one second and then the On/Off input is set to logic Low (delay from instant at which Von/Off=0.3V until Vo=10% of Vo, set)	All	Tdelay	—	3.9	—	msec
Output voltage Rise time (time for Vo to rise from 10% of $V_{o,set}$ to 90% of Vo, set)	All	Trise	—	4.2	8.5	msec
Output voltage overshoot – Startup				—	1	% $V_{O, set}$
$I_O= I_{O, max}$; $V_{IN} = 2.4$ to 5.5Vdc, $T_A = 25$ ºC						
Sequencing Delay time						
Delay from $V_{IN, min}$ to application of voltage on SEQ pin	All	$T_{SEQ-delay}$	10			msec
Tracking Accuracy (Power-Up: 2V/ms)	All	$|V_{SEQ} - V_o|$		100	200	mV
(Power-Down: 1V/ms)	All	$|V_{SEQ} - V_o|$		200	400	mV
($V_{IN, min}$ to $V_{IN, max}$; $I_{o, min}$ to $I_{o, max}$ $V_{SEQ} < V_o$)						
Overtemperature Protection	All	T_{ref}	—	150	—	°C
(See Thermal Consideration section)						
Input Undervoltage Lockout						
Turn-on Threshold	All			2.2		V
Turn-off Threshold	All			2.0		V

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Characteristic Curves

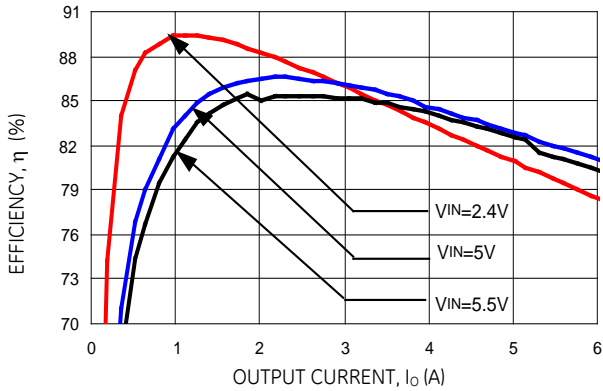The following figures provide typical characteristics for the Austin MicroLynx™ II SIP modules at 25ºC.

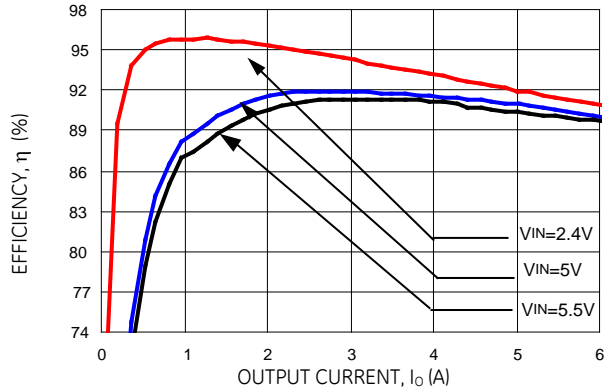**Figure 1. Converter Efficiency versus Output Current (Vout = 0.75Vdc).**

Figure 4. Converter Efficiency versus Output Current (Vout = 1.8Vdc).
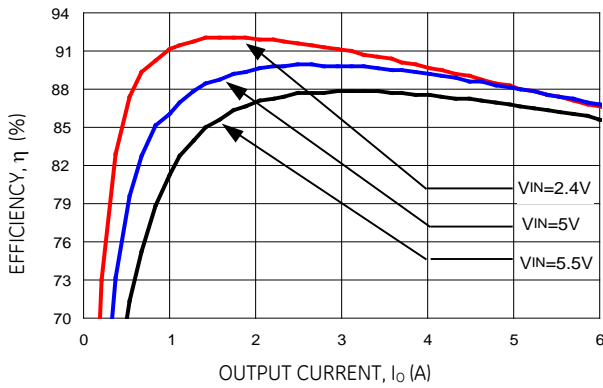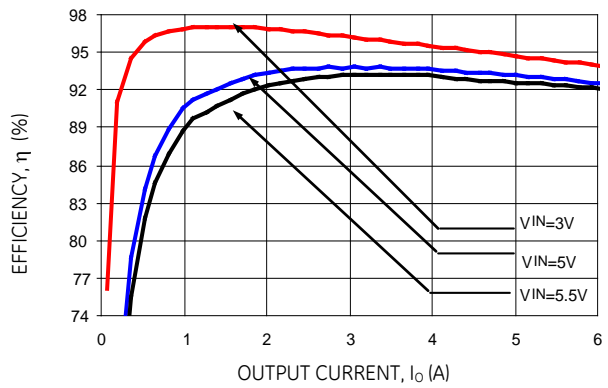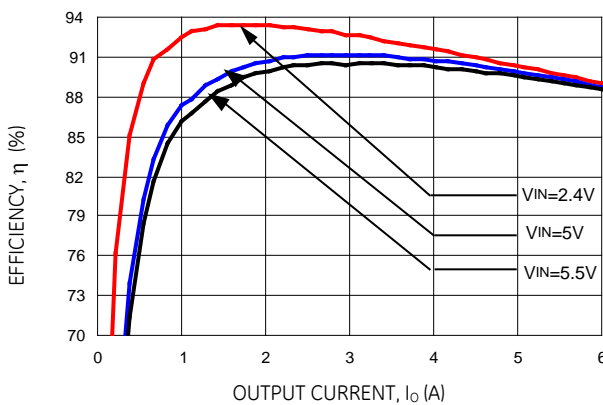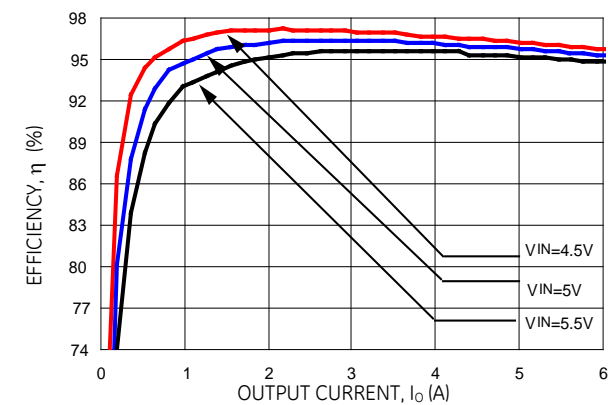
Figure 2. Converter Efficiency versus Output Current (Vout = 1.2Vdc).

Figure 5. Converter Efficiency versus Output Current (Vout = 2.5Vdc).

Figure 3. Converter Efficiency versus Output Current (Vout = 1.5Vdc).

Figure 6. Converter Efficiency versus Output Current (Vout = 3.3Vdc).

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Characteristic Curves (continued)

The following figures provide typical characteristics for the MicroLynx™ II SIP modules at 25ºC.
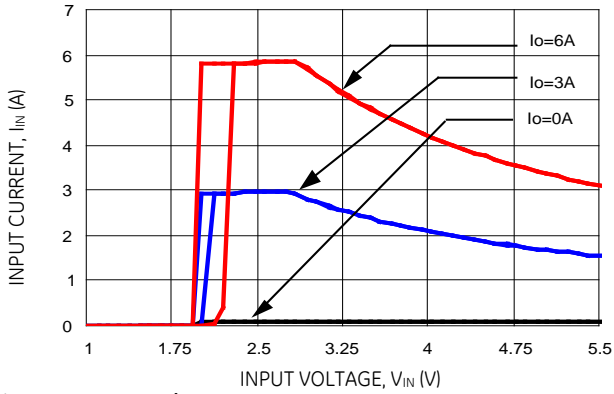
Figure 7. Input voltage vs. Input Current
 (Vout =2.5Vdc).

Figure 8. Typical Output Ripple and Noise
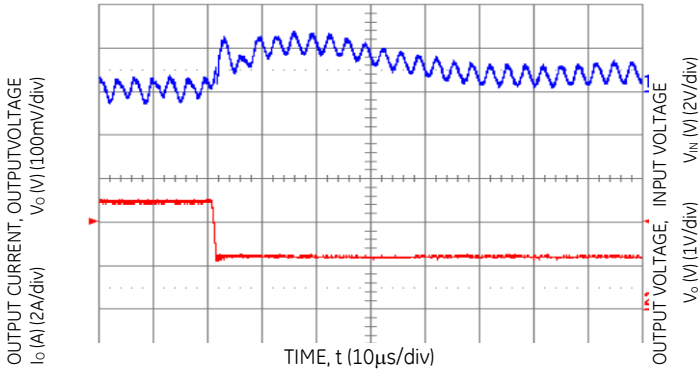(Vin = 5.0V dc, Vo = 0.75 Vdc, Io=6A).

Figure 9. Typical Output Ripple and Noise
(Vin = 5.0V dc, Vo = 3.3 Vdc, Io=6A).
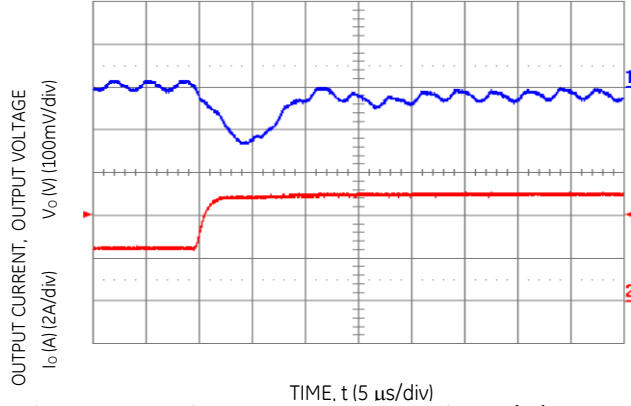
Figure 10. Transient Response to Dynamic Load Change
 from 50% to 100% of full load (Vo = 3.3Vdc).
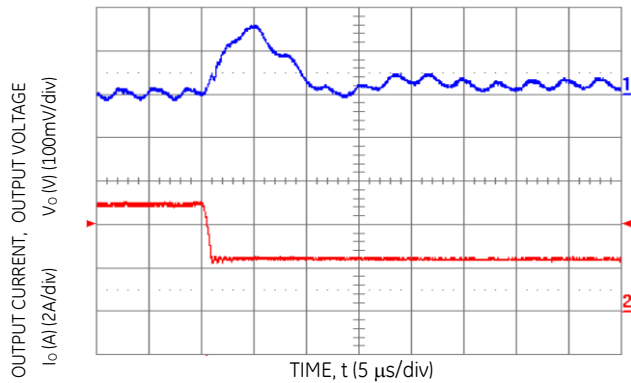
Figure 11. Transient Response to Dynamic Load Change
 from 100% to 50% of full load (Vo = 3.3 Vdc).
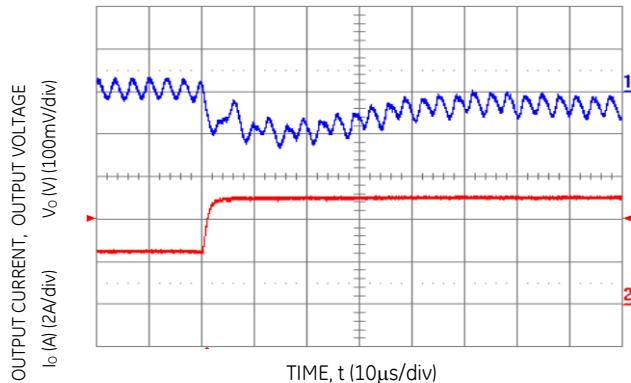
Figure 12. Transient Response to Dynamic Load Change
 from 50% to 100% of full load (Vo = 3.3 Vdc, Cext = 2x150
 µF Polymer Capacitors).

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Characteristic Curves (continued)

The following figures provide typical characteristics for the Austin MicroLynx™ II SIP modules at 25ºC.

Figure 13. Transient Response to Dynamic Load Change from 100% of 50% full load (Vo = 3.3Vdc, Cext = 2x150 µF Polymer Capacitors).
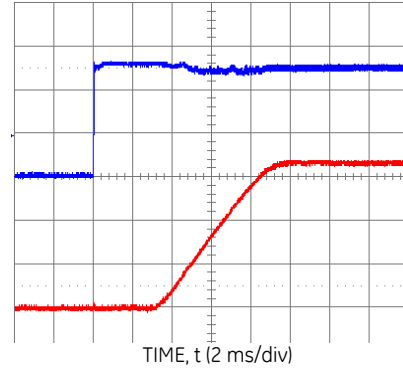
Figure 16. Typical Start-Up with application of Vin (Vin = 5.0Vdc, Vo = 3.3Vdc, Io = 6A).
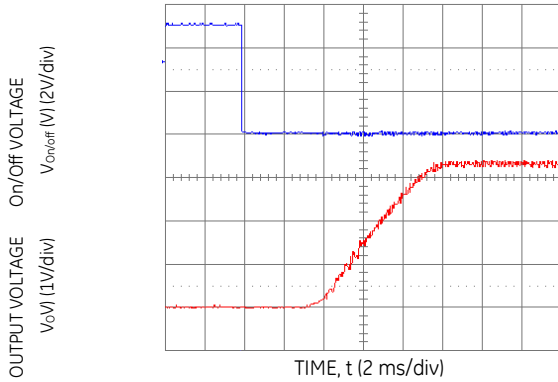
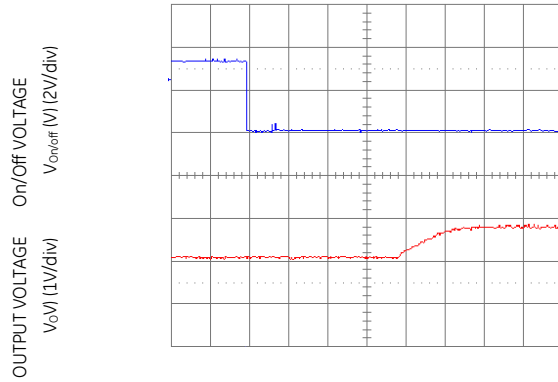**Figure 14. Typical Start-Up Using Remote On/Off (Vin = 5.0Vdc, Vo = 3.3Vdc, Io = 6A).**

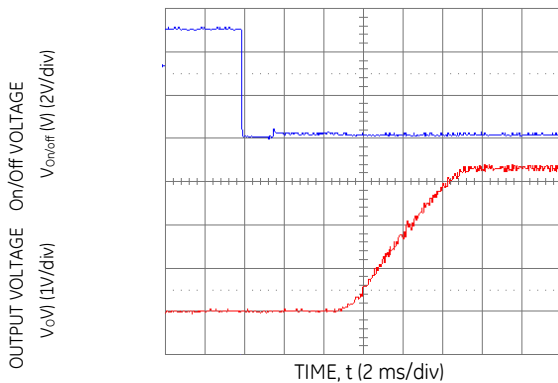**Figure 17 Typical Start-Up Using Remote On/Off with Prebias (Vin = 3.3Vdc, Vo = 1.8Vdc, Io = 1.0A, Vbias =1.0Vdc).**

Figure 15. Typical Start-Up Using Remote On/Off with Low-ESR external capacitors (7x150uF Polymer) (Vin = 5.0Vdc, Vo = 3.3Vdc, Io = 6A, Co = 1050µF).
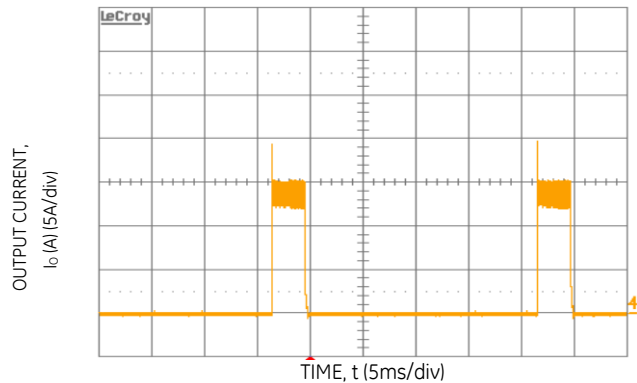

Figure 18. Output short circuit Current (Vin = 5.0Vdc, Vo = 0.75Vdc).

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Characteristic Curves (continued)

The following figures provide thermal derating curves for the Austin MicroLynx™ II SIP modules.
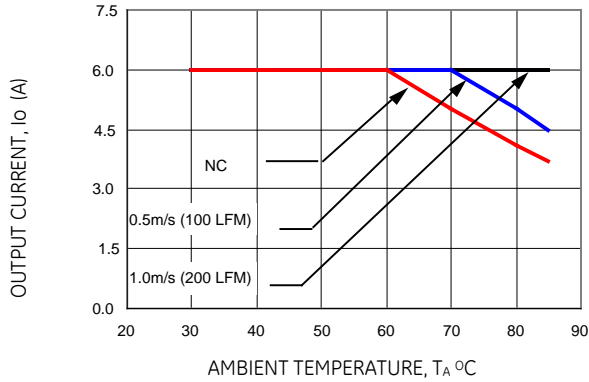

Figure 19. Derating Output Current versus Local Ambient Temperature and Airflow (Vin = 5.0, Vo=3.3Vdc).
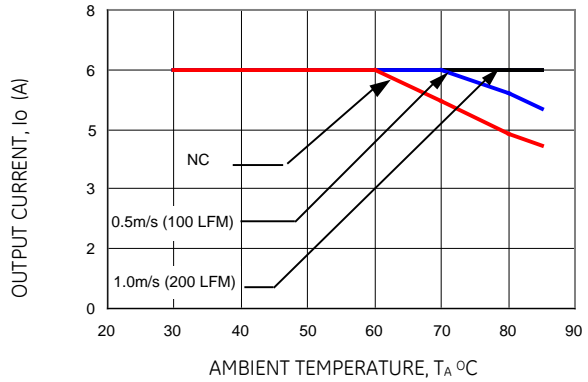

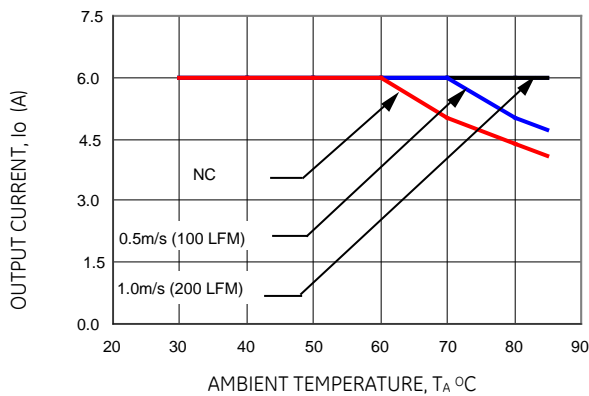Figure 22.   Derating Output Current versus Local Ambient Temperature and Airflow (Vin = 3.3dc, Vo=0.75 Vdc).

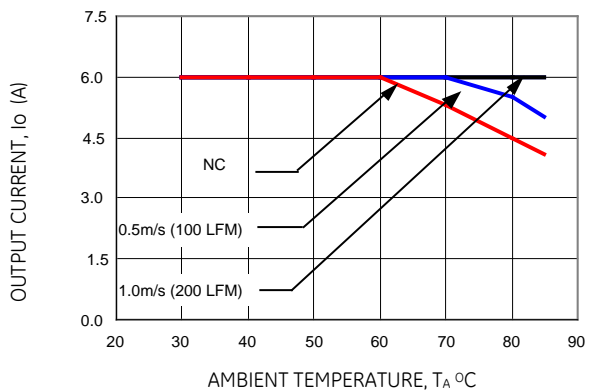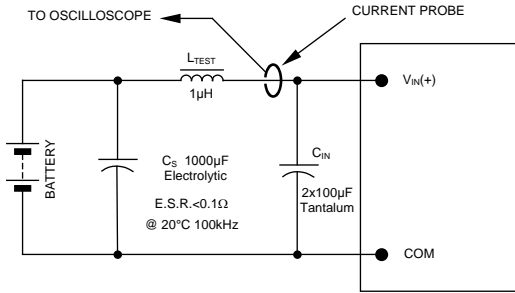Figure 20. Derating Output Current versus Local Ambient Temperature and Airflow (Vin = 5.0Vdc, Vo=0.75 Vdc).

Figure 21. Derating Output Current versus Local Ambient Temperature and Airflow (Vin = 3.3Vdc, Vo=2.5 Vdc).

Test Configurations

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NOTE: Measure input reflected ripple current with a simulated source inductance (L$_{TEST}$) of 1µH. Capacitor C$_S$ offsets possible battery impedance. Measure current as shown above.

Figure 23. Input Reflected Ripple Current Test Setup.
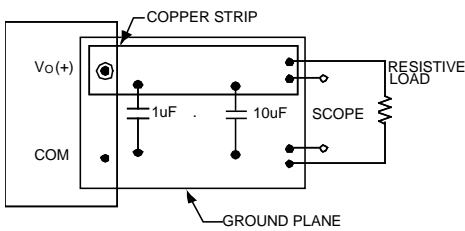
NOTE: All voltage measurements to be taken at the module terminals, as shown above. If sockets are used then Kelvin connections are required at the module terminals to avoid measurement errors due to socket contact resistance.

Figure 24. Output Ripple and Noise Test Setup.
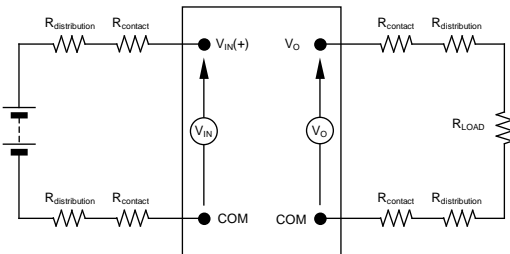
NOTE: All voltage measurements to be taken at the module terminals, as shown above. If sockets are used then Kelvin connections are required at the module terminals to avoid measurement errors due to socket contact resistance.

Figure 25. Output Voltage and Efficiency Test Setup.

$$\text{Efficiency} \quad \eta = \frac{V_O \cdot I_O}{V_{IN} \cdot I_{IN}} \times 100 \ \%$$

Design Considerations

Input Filtering

The Austin MicroLynx™ II SIP module should be connected to a low-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, low-ESR polymer and ceramic capacitors are recommended at the input of the module. Figure 26 shows the input ripple voltage (mVp-p) for various outputs with 1×150 µF polymer capacitors (Panasonic p/n: EEFUE0J151R, Sanyo p/n: 6TPE150M) in parallel with 1 × 47 µF ceramic capacitor (Panasonic p/n: ECJ-5YB0J476M, Taiyo- Yuden p/n: CEJMK432BJ476MMT) at full load. Figure 27 shows the input ripple with 2×150 µF polymer capacitors in parallel with 2 × 47 µF ceramic capacitor at full load.
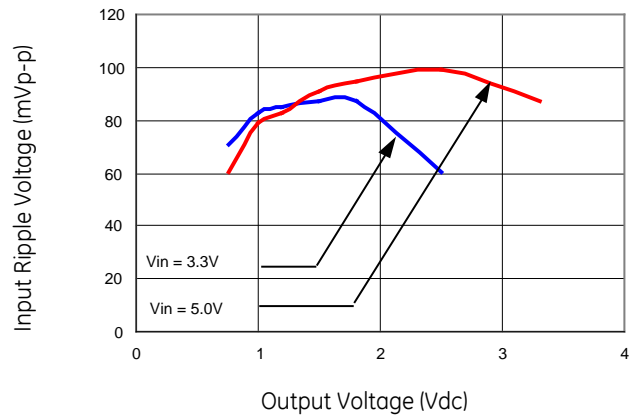

Figure 26. Input ripple voltage for various output with 1x150 µF polymer and 1x47 µF ceramic capacitors at the input (80% of Io,max).
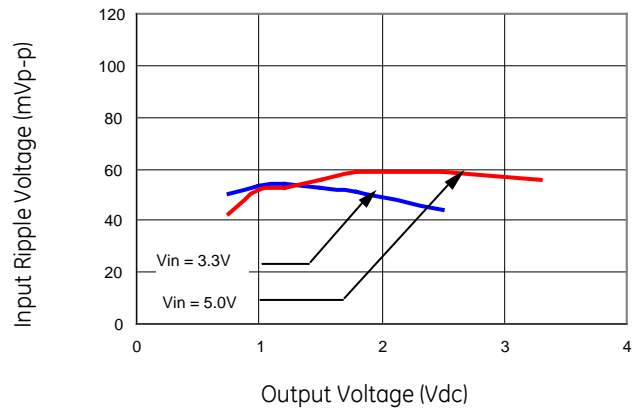

Figure 27. Input ripple voltage for various output with 2x150 µF polymer and 2x47 µF ceramic capacitors at the input (80% of Io,max).

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Design Considerations (continued)

Output Filtering

The Austin MicroLynx™ II SIP module is designed for low output ripple voltage and will meet the maximum output ripple specification with 1 µF ceramic and 10 µF tantalum capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table.

Safety Considerations

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1, CSA C22.2 No. 60950-1-03, and VDE 0850:2001-12 (EN60950-1) Licensed.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a fast-acting fuse with a maximum rating of 6A in the positive input lead.

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2.4Vdc –5.5Vdc input; 0.75Vdc to 3.63Vdc output; 6A Output Current

Feature Description

Remote On/Off

The Austin Lynx™ II SIP power modules feature an On/Off pin for remote On/Off operation. Two On/Off logic options are available in the Austin Lynx™ II series modules. Positive Logic On/Off signal, device code suffix "4", turns the module ON during a logic High on the On/Off pin and turns the module OFF during a logic Low. Negative logic On/Off signal, no device code suffix, turns the module OFF during logic High on the On/Off pin and turns the module ON during logic Low.

For positive logic modules, the circuit configuration for using the On/Off pin is shown in Figure 28. The On/Off pin is an open collector/drain logic input signal (Von/Off) that is referenced to ground. During a logic-high (On/Off pin is pulled high internal to the module) when the transistor Q1 is in the Off state, the power module is ON. Maximum allowable leakage current of the transistor when $V_{on/off} = V_{IN,max}$ is 10µA. Applying a logic-low when the transistor Q1 is turned-On, the power module is OFF. During this state VOn/Off must be less than 0.3V. When not using positive logic On/off pin, leave the pin unconnected or tie to V_{IN}.
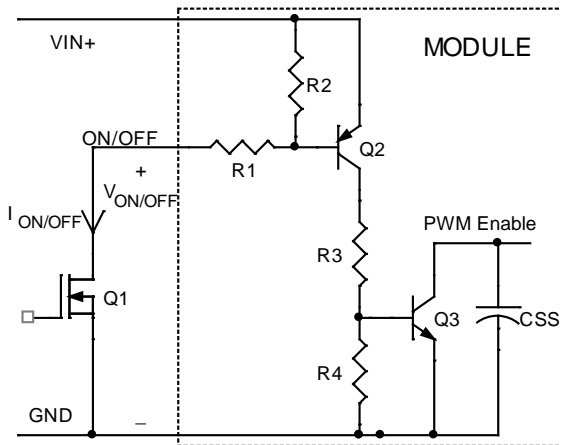

Figure 28. Circuit configuration for using positive logic On/OFF.

For negative logic On/Off devices, the circuit configuration is shown is Figure 29. The On/Off pin is pulled high with an external pull-up resistor (typical $R_{pull-up}$ = 5k, +/- 5%). When transistor Q1 is in the Off state, logic High is applied to the On/Off pin and the power module is Off. The minimum On/off voltage for logic High on the On/Off pin is 1.5Vdc. To turn the module ON, logic Low is applied to the On/Off pin by turning ON Q1. When not using the negative logic On/Off, leave the pin unconnected or tie to GND.
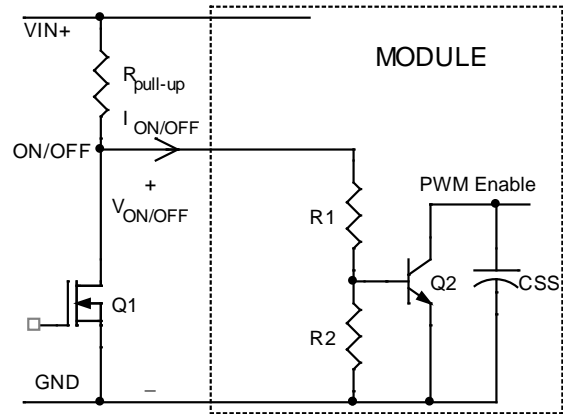

Figure 29. Circuit configuration for using negative logic On/OFF.

Overcurrent Protection

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range. The typical average output current during hiccup is 2A.

Input Undervoltage Lockout

At input voltages below the input undervoltage lockout limit, module operation is disabled. The module will begin to operate at an input voltage above the undervoltage lockout turn-on threshold.

Overtemperature Protection

To provide over temperature protection in a fault condition, the unit relies upon the thermal protection feature of the controller IC. The unit will shutdown if the thermal reference point T_{ref}, exceeds 150ºC (typical), but the thermal shutdown is not intended as a guarantee that the unit will survive temperatures beyond its rating. The module will automatically restart after it cools down.

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Feature Descriptions (continued)

Output Voltage Programming

The output voltage of the Austin MicroLynx™ II SIP can be programmed to any voltage from 0.75 Vdc to 3.3 Vdc by connecting a single resistor (shown as Rtrim in Figure 30) between the TRIM and GND pins of the module. Without an external resistor between TRIM pin and the ground, the output voltage of the module is 0.7525 Vdc. To calculate the value of the resistor *Rtrim* for a particular output voltage Vo, use the following equation:

$$Rtrim = \left[\frac{21070}{Vo - 0.7525} - 5110\right]\Omega$$

For example, to program the output voltage of the Austin MicroLynx™ II module to 1.8 Vdc, *Rtrim* is calculated is follows:

$$Rtrim = \left[\frac{21070}{1.8 - 0.7525} - 5110\right]$$

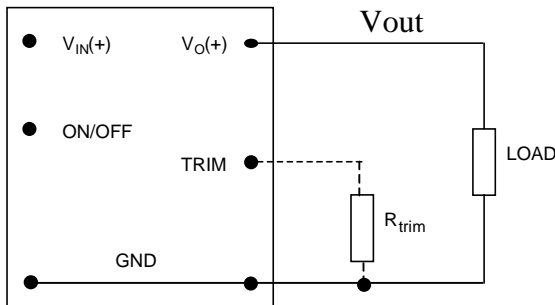$$Rtrim = 15.004 k\Omega$$

Figure 30. Circuit configuration to program output voltage using an external resistor.

Table 1 provides *Rtrim* values required for some common output voltages.

Table 1

$V_{O, set}$ (V)	*Rtrim* (KΩ)
0.7525	Open
1.2	41.973
1.5	23.077
1.8	15.004
2.5	6.947
3.3	3.160

By using a 1% tolerance trim resistor, set point tolerance of ±2% is achieved as specified in the electrical specification. The POL Programming Tool, available at www.gecriticalpower.com under the Design Tools section, helps determine the required external trim resistor needed for a specific output voltage.

Voltage Margining

Output voltage margining can be implemented in the Austin MicroLynx™ II modules by connecting a resistor, $R_{margin-up}$, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, $R_{margin-down}$, from the Trim pin to the Output pin for margining-down. Figure 31 shows the circuit configuration for output voltage margining. The POL Programming Tool, available at www.gecriticalpower.com under the Design Tools section, also calculates the values of $R_{margin-up}$ and $R_{margin-down}$ for a specific output voltage and % margin. Please consult your local GE technical representative for additional details.
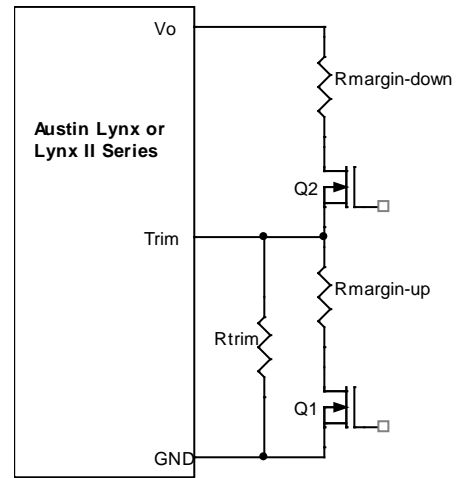

Figure 31. Circuit Configuration for margining Output voltage.

6A Austin MicroLynx™II: SIP Non-Isolated DC-DC Power Modules
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Feature Descriptions (continued)

Voltage Sequencing

Austin MicroLynx™ II series of modules include a sequencing feature, EZ-SEQUENCE™ that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, either tie the SEQ pin to V_{IN} or leave it unconnected.

When an analog voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The SEQ voltage must be set higher than the set-point voltage of the module. The output voltage follows the voltage on the SEQ pin on a one-to-one volt basis. By connecting multiple modules together, customers can get multiple modules to track their output voltages to the voltage applied on the SEQ pin.

For proper voltage sequencing, first, input voltage is applied to the module. The On/Off pin of the module is left unconnected (or tied to GND for negative logic modules or tied to V_{IN} for positive logic modules) so that the module is ON by default. After applying input voltage to the module, a minimum of 10msec delay is required before applying voltage on the SEQ pin. During this time, potential of 50mV (± 10 mV) is maintained on the SEQ pin. After 10msec delay, an analog voltage is applied to the SEQ pin and the output voltage of the module will track this voltage on a one-to-one volt bases until output reaches the set-point voltage. To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. Output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential to ensure a controlled shutdown of the modules.

When using the EZ-SEQUENCE™ feature to control start-up of the module, pre-bias immunity feature during start-up is disabled. The pre-bias immunity feature of the module relies on the module being in the diode-mode during start-up. When using the EZ-SEQUENCE™ feature, modules goes through an internal set-up time of 10msec, and will be in synchronous rectification mode when voltage at the SEQ pin is applied. This will result in sinking current in the module if pre-bias voltage is present at the output of the module. When pre-bias immunity during start-up is required, the EZ-SEQUENCE™ feature must be disabled. For additional guidelines on using EZ-SEQUENCE™ feature of Austin MicroLynx™ II , contact GE technical representative for preliminary application note on output voltage sequencing using Austin Lynx II series.

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Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should be provided to help ensure reliable operation.

Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 33. Note that the airflow is parallel to the long axis of the module as shown in figure 32. The derating data applies to airflow in either direction of the module's long axis.

The output power of the module should not exceed the rated power of the module (Vo,set × Io,max).

Please refer to the Application Note "Thermal Characterization Process For Open-Frame Board-Mounted Power Modules" for a detailed discussion of thermal aspects including maximum device temperatures.
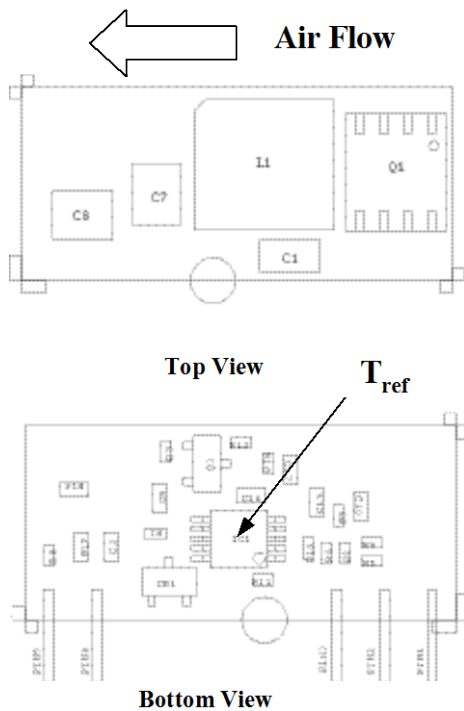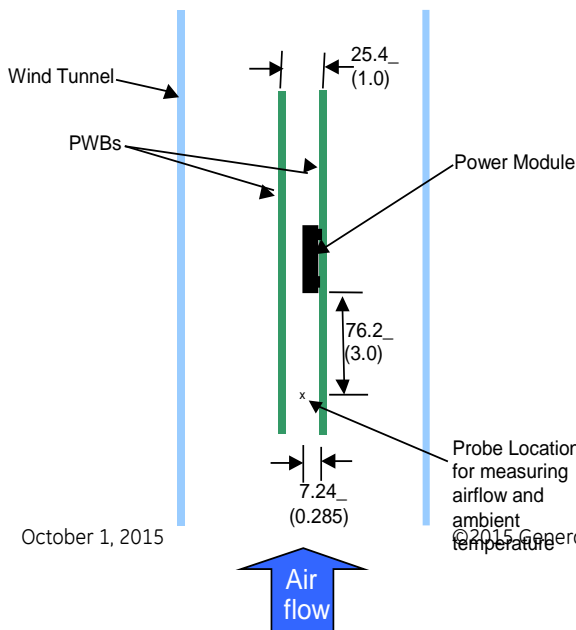

Air Flow

Top View

T_{ref}

Bottom View

Figure 33. Thermal Test Set-up.

Heat Transfer via Convection

Increased airflow over the module enhances the heat transfer via convection. Thermal derating curves showing the maximum output current that can be delivered by various module versus local ambient temperature (T_A) for natural convection and up to 1m/s (200 ft./min) are shown in the Characteristics Curves section.

Figure 32. T_{ref} Temperature measurement location.

The thermal reference point, $T_{ref\ 1}$ used in the specifications of thermal derating curves is shown in Figure 32. For reliable operation this temperature should not exceed 125°C.

Wind Tunnel

25.4_ (1.0)

PWBs

Power Module

76.2_ (3.0)

7.24_ (0.285)

Probe Location for measuring airflow and ambient temperature

Air flow

Post solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to *Board Mounted Power Modules: Soldering and Cleaning* Application Note.

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Through-Hole Lead-Free Soldering Information

The RoHS-compliant through-hole products use the SAC (Sn/Ag/Cu) Pb-free solder and RoHS-compliant components. They are designed to be processed through single or dual wave soldering machines. The pins have an RoHS-compliant finish that is compatible with both Pb and Pb-free wave soldering processes. A maximum preheat rate of 3°C/s is suggested. The wave preheat process should be such that the temperature of the power module board is kept below 210°C. For Pb solder, the recommended pot temperature is 260°C, while the Pb-free solder pot is 270°C max. Not all RoHS-compliant through-hole products can be processed with paste-through-hole Pb or Pb-free reflow process. If additional information is needed, please consult with your GE technical representative for more details.

6A Austin MicroLynx™II: SIP Non-Isolated DC-DC Power Modules
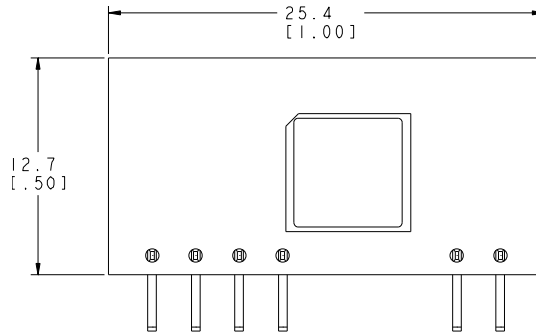## 2.4Vdc –5.5Vdc input; 0.75Vdc to 3.63Vdc output; 6A Output Current

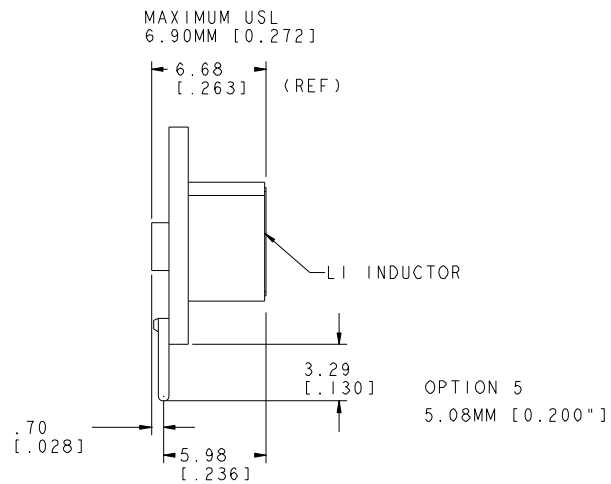## Mechanical Outline

Dimensions are in millimeters and (inches).

Tolerances: x.x mm ± 0.5 mm (x.xx in. ± 0.02 in.) [unless otherwise indicated]

x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in.)

Top View

Side View

Bottom View

PIN	FUNCTION
1	Vo
2	Trim
3	GND
A	SEQ
4	V$_{IN}$
5	On/Off

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Recommended Pad Layout

Dimensions are in millimeters and (inches).

Tolerances: x.x mm ± 0.5 mm (x.xx in. ± 0.02 in.) [unless otherwise indicated]
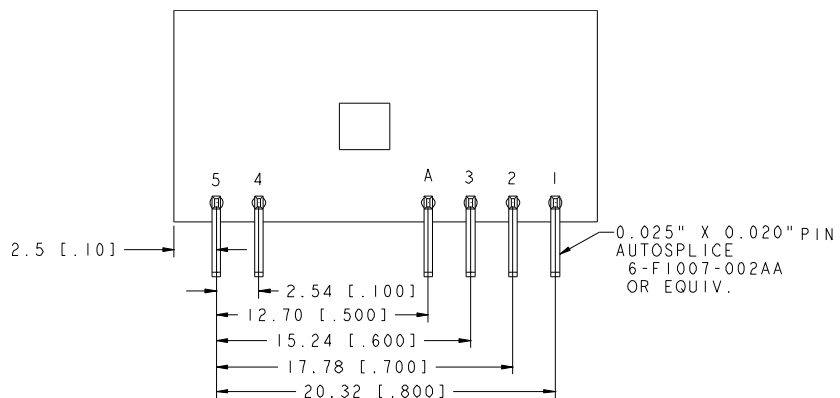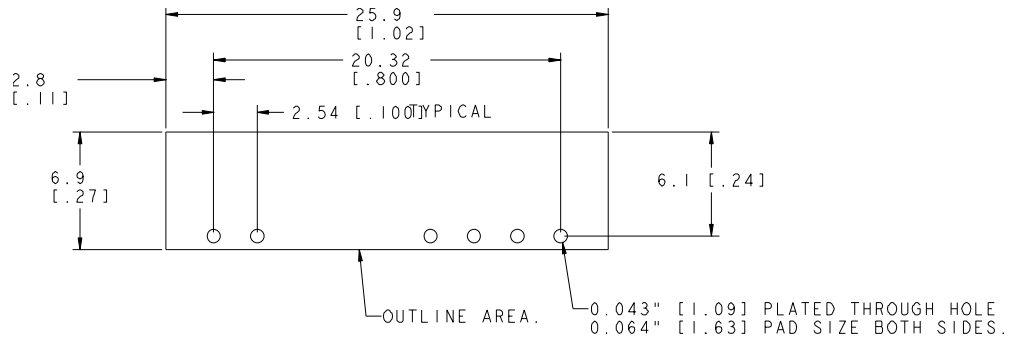
x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in.)

PIN	FUNCTION
1	Vo
2	Trim
3	GND
A	SEQ
4	V$_{IN}$
5	On/Off

25.9 [1.02]
20.32 [.800]
2.8 [.11]
2.54 [.100] TYPICAL
6.9 [.27]
6.1 [.24]
OUTLINE AREA.
0.043" [1.09] PLATED THROUGH HOLE
0.064" [1.63] PAD SIZE BOTH SIDES.

Through-Hole Pad Layout – Back view

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Ordering Information

Please contact your GE Sales Representative for pricing, availability and optional features.

Table 2. Device Codes

Device Code	Input Voltage	Output Voltage	Output Current	Efficiency 3.3V@ 6A	Connector Type	Comcodes
ATH006A0X	2.4 – 5.5Vdc	0.75 – 3.63Vdc	6 A	96.0%	SIP	108989018
ATH006A0XZ	2.4 – 5.5Vdc	0.75 – 3.63Vdc	6 A	96.0%	SIP	CC109104717
ATH006A0X4	2.4 – 5.5Vdc	0.75 – 3.63Vdc	6 A	96.0%	SIP	108989026
ATH006A0X4Z	2.4 – 5.5Vdc	0.75 – 3.63Vdc	6 A	96.0%	SIP	CC109104725

-Z refers to RoHS-compliant versions.

Contact Us

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