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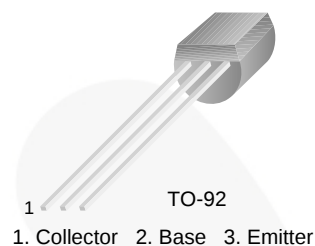


November 2014

BC546 / BC547 / BC548 / BC549 / BC550 NPN Epitaxial Silicon Transistor

Features

- Switching and Amplifier
- High-Voltage: BC546, $V_{CEO} = 65\text{ V}$
- Low-Noise: BC549, BC550
- Complement to BC556, BC557, BC558, BC559, and BC560



Ordering Information

Part Number	Marking	Package	Packing Method
BC546ABU	BC546A	TO-92 3L	Bulk
BC546ATA	BC546A	TO-92 3L	Ammo
BC546BTA	BC546B	TO-92 3L	Ammo
BC546BTF	BC546B	TO-92 3L	Tape and Reel
BC546CTA	BC546C	TO-92 3L	Ammo
BC547ATA	BC547A	TO-92 3L	Ammo
BC547B	BC547B	TO-92 3L	Bulk
BC547BBU	BC547B	TO-92 3L	Bulk
BC547BTA	BC547B	TO-92 3L	Ammo
BC547BTF	BC547B	TO-92 3L	Tape and Reel
BC547CBU	BC547C	TO-92 3L	Bulk
BC547CTA	BC547C	TO-92 3L	Ammo
BC547CTFR	BC547C	TO-92 3L	Tape and Reel
BC548BU	BC548	TO-92 3L	Bulk
BC548BTA	BC548B	TO-92 3L	Ammo
BC548CTA	BC548C	TO-92 3L	Ammo
BC549BTA	BC549B	TO-92 3L	Ammo
BC549BTF	BC549B	TO-92 3L	Tape and Reel
BC549CTA	BC549C	TO-92 3L	Ammo
BC550CBU	BC550C	TO-92 3L	Bulk
BC550CTA	BC550C	TO-92 3L	Ammo

BC546 / BC547 / BC548 / BC549 / BC550 — NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{CBO}	Collector-Base Voltage	BC546	80	V
		BC547 / BC550	50	
		BC548 / BC549	30	
V_{CEO}	Collector-Emitter Voltage	BC546	65	V
		BC547 / BC550	45	
		BC548 / BC549	30	
V_{EBO}	Emitter-Base Voltage	BC546 / BC547	6	V
		BC548 / BC549 / BC550	5	
I_C	Collector Current (DC)		100	mA
P_C	Collector Power Dissipation		500	mW
T_J	Junction Temperature		150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-65 to +150	$^\circ\text{C}$

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
I _{CBO}	Collector Cut-Off Current		V _{CB} = 30 V, I _E = 0			15	nA
h _{FE}	DC Current Gain		V _{CE} = 5 V, I _C = 2 mA	110		800	
V _{CE(sat)}	Collector-Emitter Saturation Voltage		I _C = 10 mA, I _B = 0.5 mA		90	250	mV
			I _C = 100 mA, I _B = 5 mA		250	600	
V _{BE(sat)}	Base-Emitter Saturation Voltage		I _C = 10 mA, I _B = 0.5 mA		700		mV
			I _C = 100 mA, I _B = 5 mA		900		
V _{BE(on)}	Base-Emitter On Voltage		V _{CE} = 5 V, I _C = 2 mA	580	660	700	mV
			V _{CE} = 5 V, I _C = 10 mA			720	
f _T	Current Gain Bandwidth Product		V _{CE} = 5 V, I _C = 10 mA, f = 100 MHz		300		MHz
C _{ob}	Output Capacitance		V _{CB} = 10 V, I _E = 0, f = 1 MHz		3.5	6.0	pF
C _{ib}	Input Capacitance		V _{EB} = 0.5 V, I _C = 0, f = 1 MHz		9		pF
NF	Noise Figure	BC546 / BC547 / BC548	V _{CE} = 5 V, I _C = 200 μA, f = 1 kHz, R _G = 2 kΩ		2.0	10.0	dB
		BC549 / BC550			1.2	4.0	
		BC549	V _{CE} = 5 V, I _C = 200 μA, R _G = 2 kΩ, f = 30 to 15000 MHz		1.4	4.0	
		BC550			1.4	3.0	

h_{FE} Classification

Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800

Typical Performance Characteristics

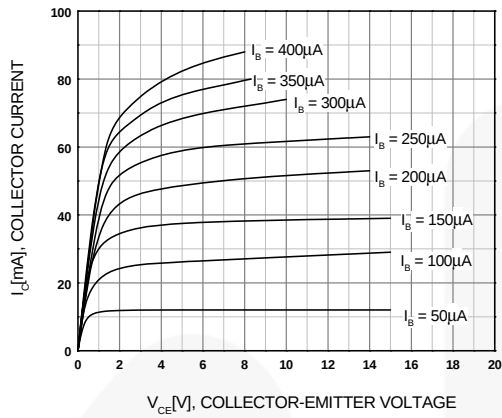


Figure 1. Static Characteristic

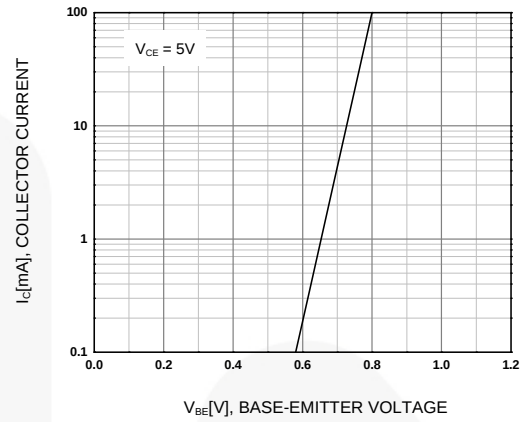


Figure 2. Transfer Characteristic

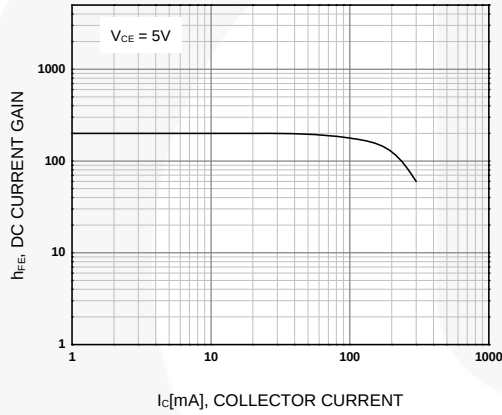


Figure 3. DC Current Gain

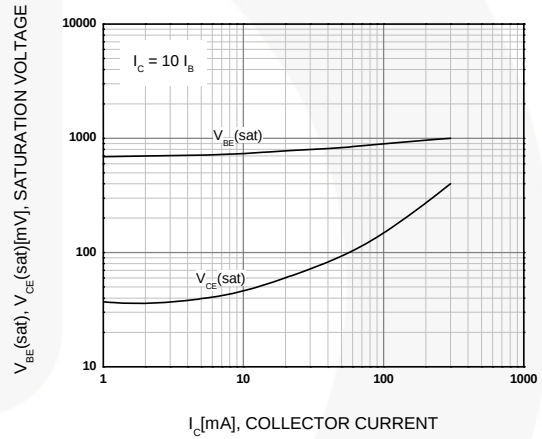


Figure 4. Base-Emitter Saturation Voltage and Collector-Emitter Saturation Voltage

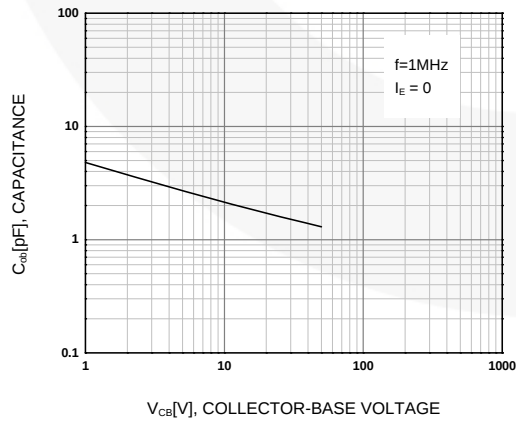


Figure 5. Output Capacitance

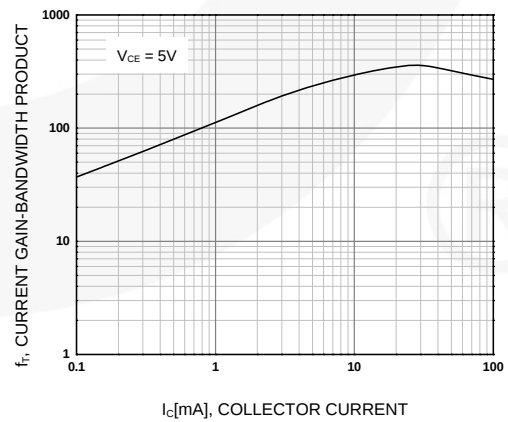
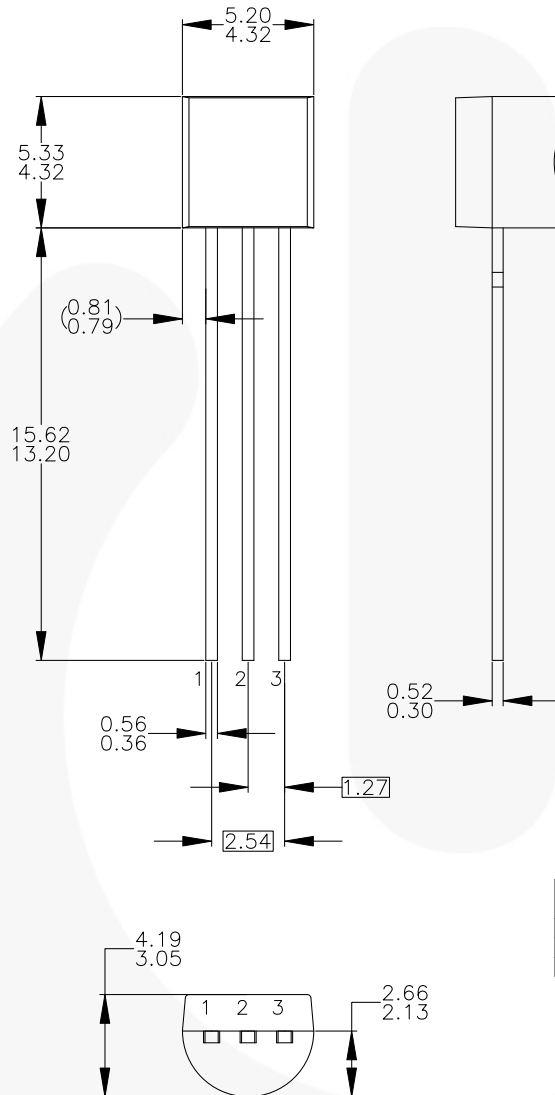


Figure 6. Current Gain Bandwidth Product

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

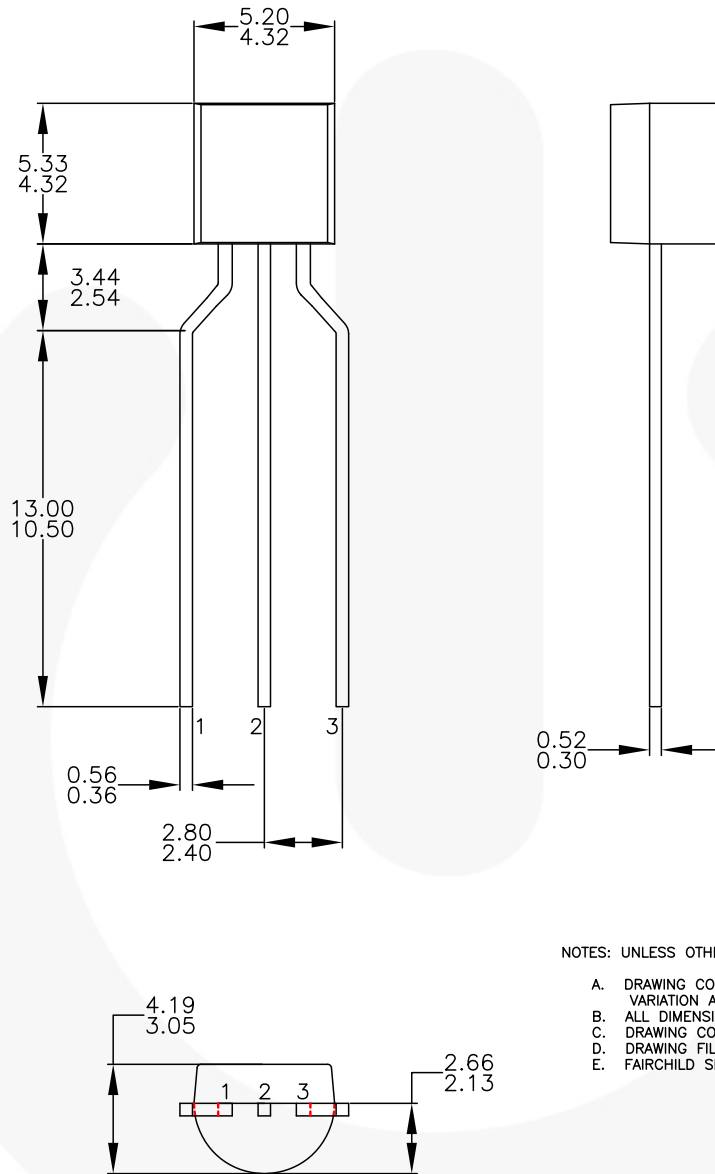
LEGEND:

P — BIPOLAR E — EMITTER D — DRAIN
F — JFET B — BASE S — SOURCE
M — DMOS C — COLLECTOR G — GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98:
PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 7. 3-Lead, TO-92, JEDEC TO-92 Compliant Straight Lead Configuration, Bulk Type

Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREVS.
- E. FAIRCHILD SEMICONDUCTOR.

Figure 8. 3-Lead, TO-92, Molded, 0.2 In Line Spacing Lead Form, Ammo, Tape and Reel Type



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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