Single-Supply, High Speed, Fixed G = +2, Rail-to-Rail Output Video Amplifier

Data Sheet

ADA4856-3

FEATURES

- Voltage feedback architecture
- Rail-to-rail output swing: 0.1 V to 4.9 V
- High speed amplifier
  - −3 dB bandwidth: 225 MHz
  - 0.1 dB flatness at 2 V p-p: 74 MHz
  - Slew rate: 800 V/µs
  - Settling time to 0.1% with 2 V step: 5 ns
- High input common-mode voltage range
  - $-V_S - 0.2$ V to $+V_S - 1$ V
- Supply range: 3 V to 5.5 V
- Differential gain error: 0.01%
- Differential phase error: 0.01°
- Low power
  - 7.8 mA/amplifier typical supply current
  - Power-down feature
- Available in 16-lead LFCSP

CONNECTION DIAGRAM

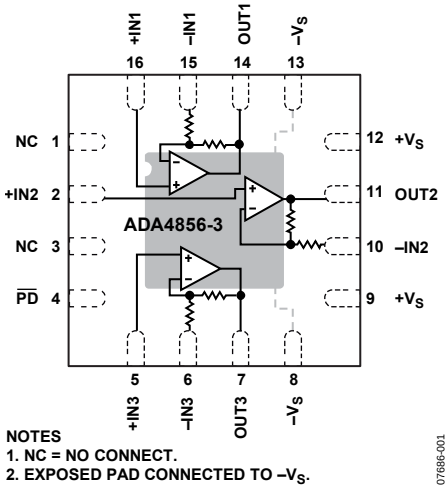

Figure 1.

APPLICATIONS

- Professional video
- Consumer video
- Imaging
- Instrumentation
- Base stations
- Active filters
- Buffers

GENERAL DESCRIPTION

The ADA4856-3 (triple) is a fixed gain of +2, single-supply, rail-to-rail output video amplifier. It provides excellent video performance with 225 MHz, −3 dB bandwidth, 800 V/µs slew rate, and 74 MHz, 0.1 dB flatness into a 150 Ω load. It has a wide input common-mode voltage range that extends 0.2 V below ground and 1 V below the positive rail. In addition, the output voltage swings within 200 mV of either supply, making this video amplifier easy to use on single-supply voltages as low as 3.3 V.

The ADA4856-3 offers a typical low power of 7.8 mA per amplifier, while being capable of delivering up to 52 mA of load current. It also features a power-down function for power sensitive applications that reduces the supply current to 1 mA.

The ADA4856-3 is available in a 16-lead LFCSP and is designed to work over the extended industrial temperature range of −40°C to +105°C.

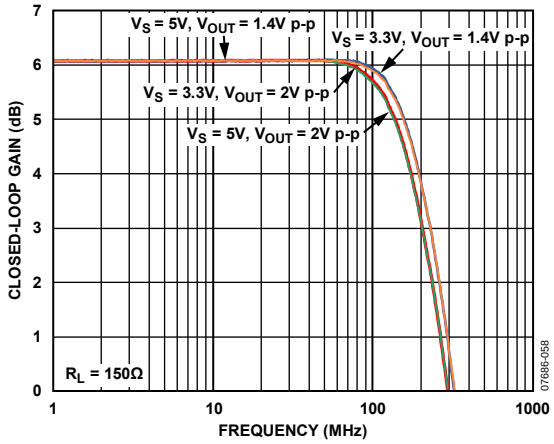

Figure 2. Large Signal Frequency Response

Document Feedback

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Changed Package from CP-16-14 to CP-16-23 (Throughout) ... 1
Updated Outline Dimensions ... 17
Changes to Ordering Guide ... 7

1/09—Rev. 0 to Rev. A

Changes to Figure 9 ... 7
Changes to Figure 13, Figure 15, and Figure 16 ... 8
Added Figure 17 and Figure 20; Renumbered Sequentially ... 9

10/08—Revision 0: Initial Version

SPECIFICATIONS

5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, G = +2, R_L = 150 Ω to midsupply, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.1 V p-p		370		MHz
	V_O = 1.4 V p-p		225		MHz
	V_O = 2 V p-p		200		MHz
Bandwidth for 0.1 dB Flatness	V_O = 1.4 V p-p		90		MHz
	V_O = 2 V p-p		74		MHz
Slew Rate	V_O = 2 V step		800		V/µs
Settling Time to 0.1% (Rise/Fall)	V_O = 2 V step		4.8/5.2		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−92/−110		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−68/−71		dBc
Crosstalk, Output to Output	f = 5 MHz		−80		dB
Input Voltage Noise	f = 100 kHz		14		nV/√Hz
Input Current Noise	f = 100 kHz		2		pA/√Hz
Differential Gain Error			0.01		%
Differential Phase Error			0.01		Degrees
DC PERFORMANCE					
Input Offset Voltage			1.3	3.4	mV
Input Offset Voltage Drift			5.5		µV/°C
Input Bias Current			−3.8		µA
Input Offset Current			±0.05		µA
Closed-Loop Gain		1.95	2	2.05	V/V
Open-Loop Gain			90		dB
INPUT CHARACTERISTICS					
Input Resistance			3.2		MΩ
Input Capacitance			0.5		pF
Input Common-Mode Voltage Range		$-V_S$ − 0.2		$+V_S$ − 1	V
Common-Mode Rejection Ratio	V_{CM} = −0.2 V to +4 V		94		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing			0.1 to 4.9		V
Linear Output Current Per Amplifier	HD2 ≤ −60 dBc, R_L = 10 Ω		52		mA
POWER-DOWN					
Turn-On Time			78		ns
Turn-Off Time			950		ns
Input Bias Current	Enabled		0.2		µA
	Powered down		−125		µA
Turn-On Voltage			3.75		V
POWER SUPPLY					
Operating Range		3		5.5	V
Quiescent Current per Amplifier			7.8		mA
Supply Current When Disabled			1.1		mA
Power Supply Rejection Ratio	ΔV_S = 4.5 V to 5.5 V		96		dB

3.3 V OPERATION

T_A = 25°C, $+V_S$ = 3.3 V, $-V_S$ = 0 V, G = +2, R_L = 150 Ω to midsupply, unless otherwise noted.

Table 2.

Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.1 V p-p		370		MHz
	V_O = 2 V p-p		225		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p		77		MHz
Slew Rate	V_O = 2 V step		800		V/µs
Settling Time to 0.1% (Rise/Fall)	V_O = 2 V step		4.8/7		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f_C = 5 MHz, V_O = 1 V p-p, R_L = 1 kΩ		−95/−128		dBc
	f_C = 20 MHz, V_O = 1 V p-p, R_L = 1 kΩ		−74/−101		dBc
Crosstalk, Output to Output	f = 5 MHz		−78		dB
Input Voltage Noise	f = 100 kHz		14		nV/√Hz
Input Current Noise	f = 100 kHz		2		pA/√Hz
Differential Gain Error			0.01		%
Differential Phase Error			0.01		Degrees
DC PERFORMANCE					
Input Offset Voltage			1.2	3	mV
Input Offset Voltage Drift			5.5		µV/°C
Input Bias Current			−3.8		µA
Input Offset Current			±0.05		µA
Closed-Loop Gain		1.95	2	2.05	V/V
Open-Loop Gain			90		dB
INPUT CHARACTERISTICS					
Input Resistance			3.2		MΩ
Input Capacitance			0.5		pF
Input Common-Mode Voltage Range		$-V_S$ − 0.2		$+V_S$ − 1	V
Common-Mode Rejection Ratio	V_{CM} = −0.2 V to +2.3 V		94		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing			0.1 to 3.22		V
Linear Output Current Per Amplifier	HD2 ≤ −60 dBc, R_L = 10 Ω		49		mA
POWER-DOWN					
Turn-On Time			78		ns
Turn-Off Time			950		ns
Turn-On Voltage			2.05		V
POWER SUPPLY					
Operating Range		3		5.5	V
Quiescent Current per Amplifier			7.5		mA
Quiescent Current When Powered Down			0.98		mA
Power Supply Rejection Ratio	ΔV_S = 2.97 V to 3.63 V		94		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Internal Power Dissipation[1]	See Figure 3
Common-Mode Input Voltage	($-V_S$ – 0.2 V) to ($+V_S$ – 1 V)
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Observe power curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for device in free air.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead LFCSP	67	17.5	°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADA4856-3 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

To ensure proper operation, it is necessary to observe the maximum power derating curves.

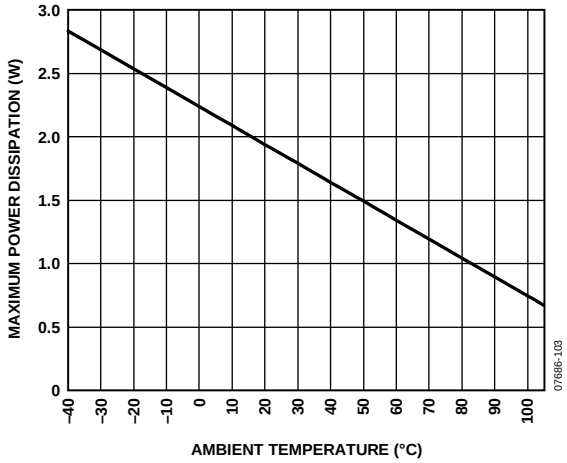


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

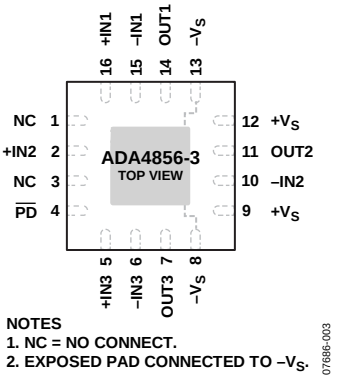


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	+IN2	Noninverting Input 2.
3	NC	No Connect.
4	$\overline{PD}$	Power Down.
5	+IN3	Noninverting Input 3.
6	–IN3	Inverting Input 3.
7	OUT3	Output 3.
8	$-V_S$	Negative Supply.
9	$+V_S$	Positive Supply.
10	–IN2	Inverting Input 2.
11	OUT2	Output 2.
12	$+V_S$	Positive Supply.
13	$-V_S$	Negative Supply.
14	OUT1	Output 1.
15	–IN1	Inverting Input 1.
16	+IN1	Noninverting Input 1.
17 (EPAD)	Exposed Pad (EPAD)	The exposed pad must be connected to $-V_S$.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $+V_S$ = 5 V, G = +2, R_L = 150 Ω, large signal V_{OUT} = 2 V p-p, small signal V_{OUT} = 100 mV p-p, unless otherwise noted.

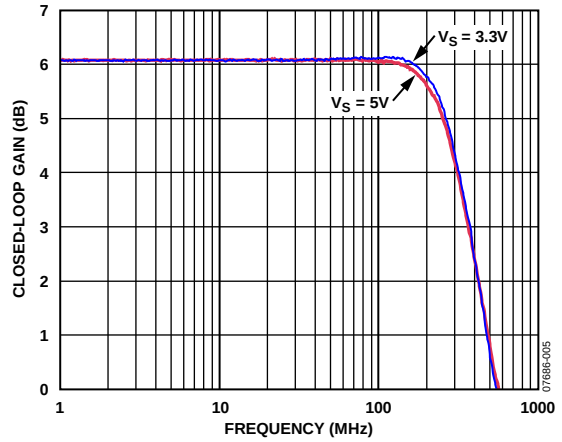


Figure 5. Small Signal Frequency Response vs. Supply Voltage

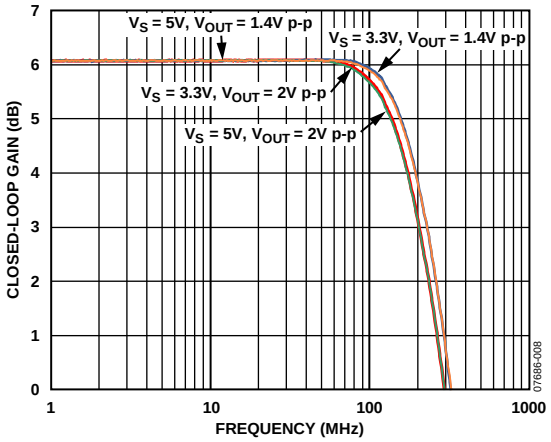


Figure 8. Large Signal Frequency Response vs. Supply Voltage

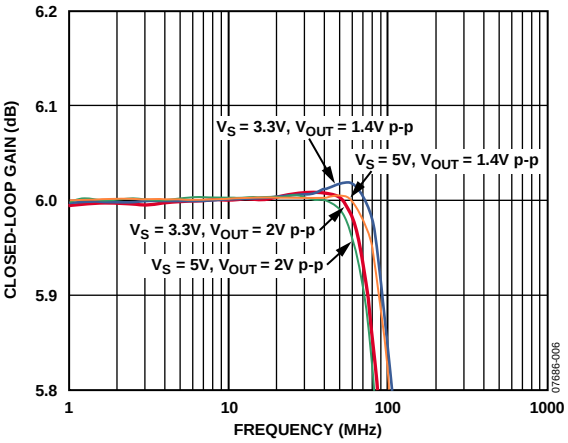


Figure 6. Large Signal 0.1 dB Flatness vs. Supply Voltage

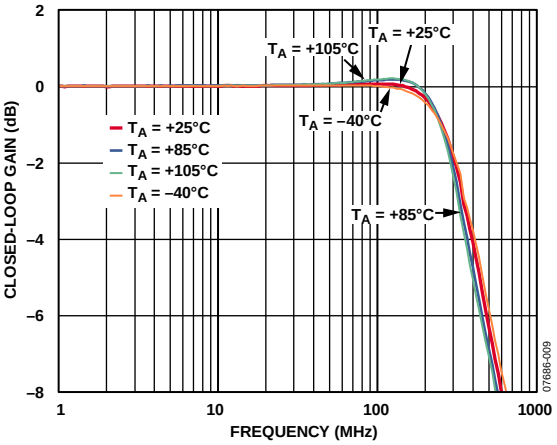


Figure 9. Small Signal Frequency Response vs. Temperature

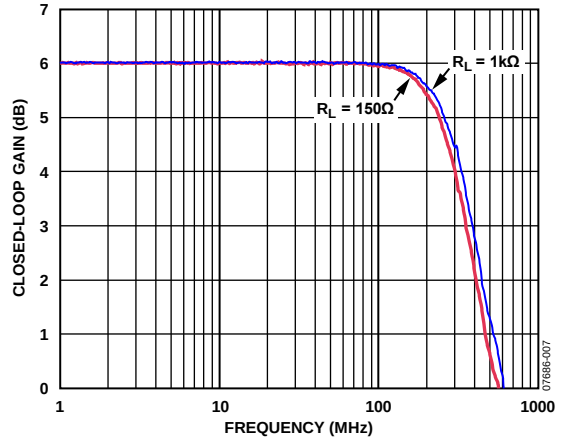


Figure 7. Small Signal Frequency Response vs. Load Resistance

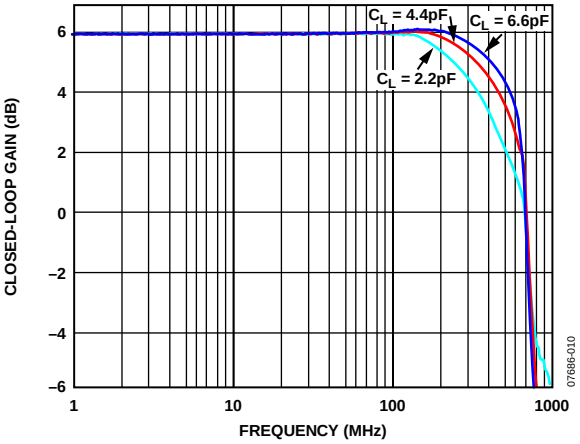


Figure 10. Small Signal Frequency Response vs. Capacitive Load

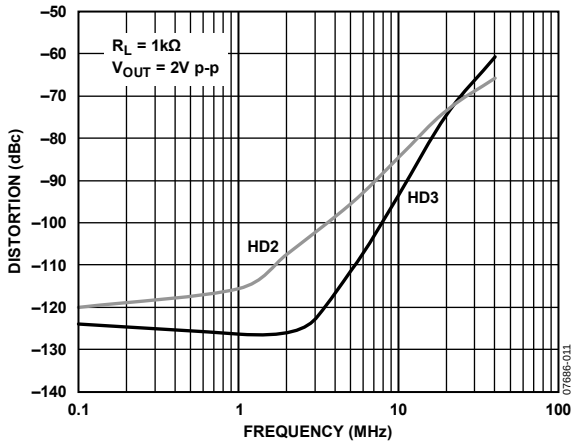


Figure 11. Harmonic Distortion vs. Frequency

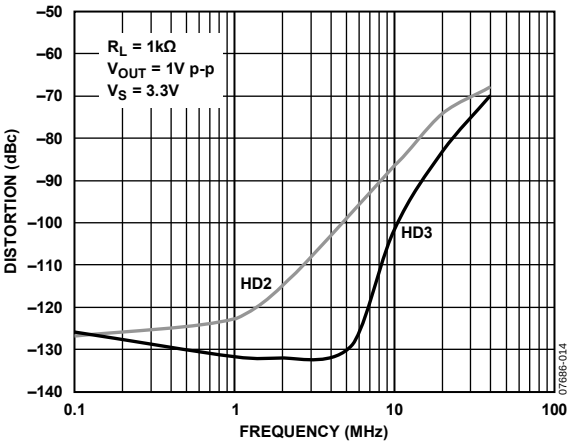


Figure 14. Harmonic Distortion vs. Frequency

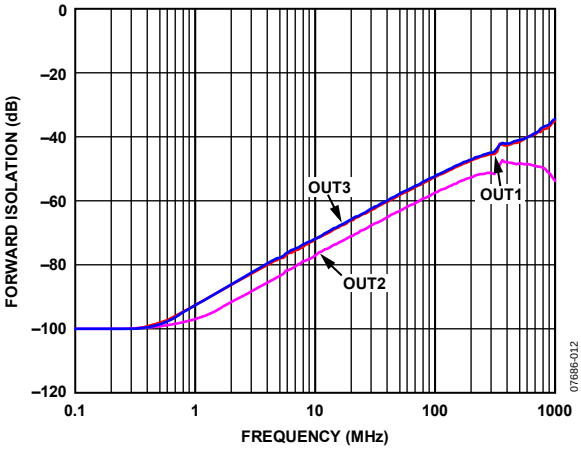


Figure 12. Forward Isolation vs. Frequency

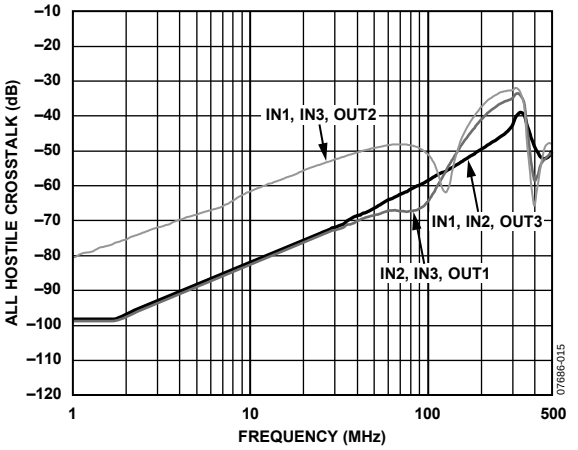


Figure 15. Crosstalk vs. Frequency

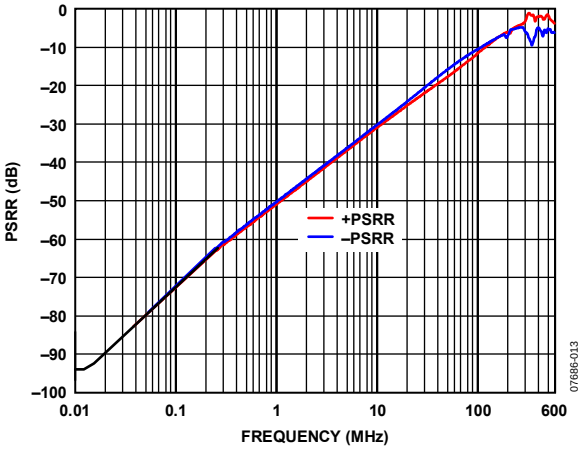


Figure 13. Power Supply Rejection Ratio (PSRR) vs. Frequency

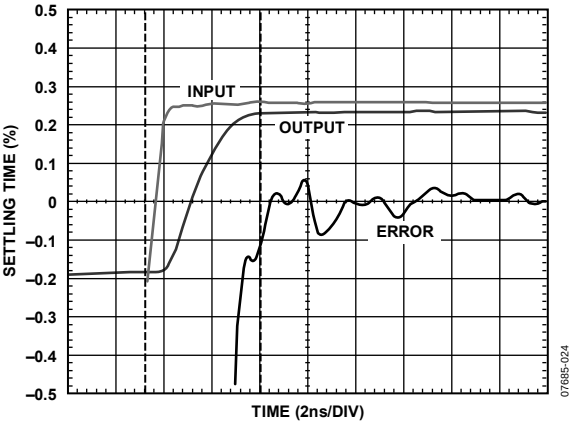


Figure 16. Settling Time

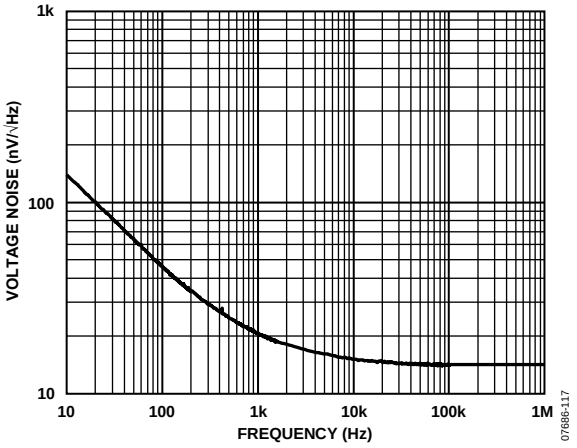


Figure 17. Output Voltage Noise vs. Frequency

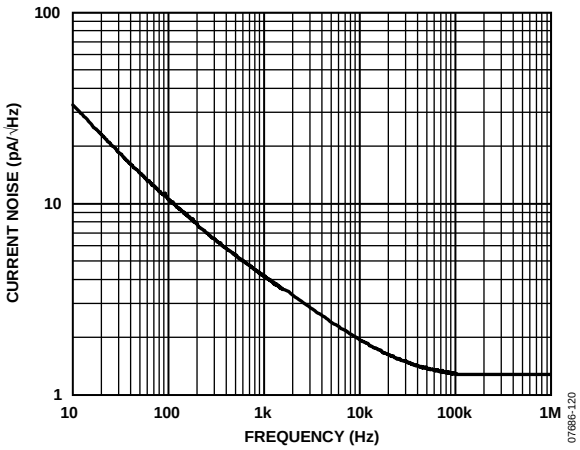


Figure 20. Output Current Noise vs. Frequency

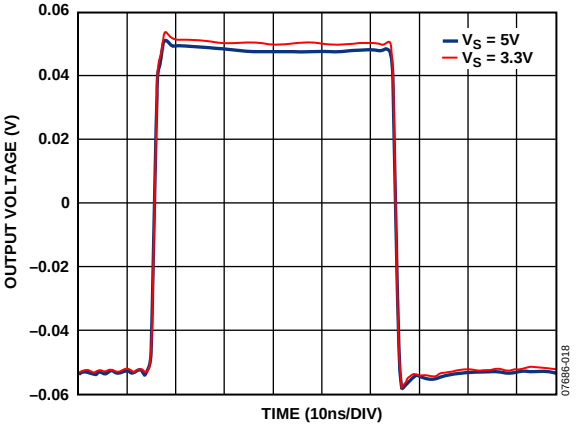


Figure 18. Small Signal Transient Response vs. Supply Voltage

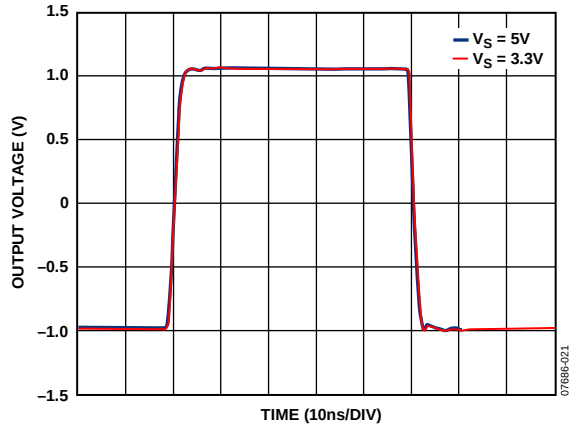


Figure 21. Large Signal Transient Response vs. Supply Voltage

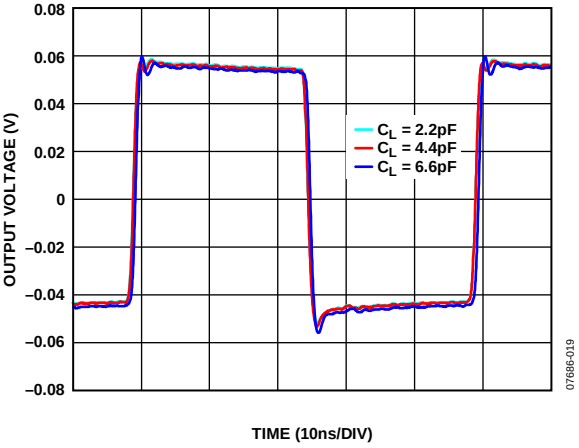


Figure 19. Small Signal Transient Response vs. Capacitive Load

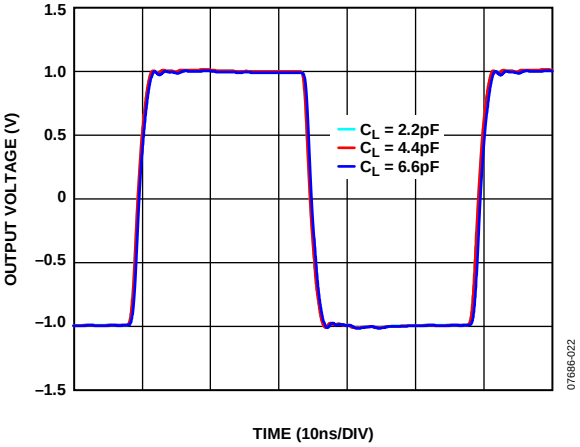


Figure 22. Large Signal Transient Response vs. Capacitive Load

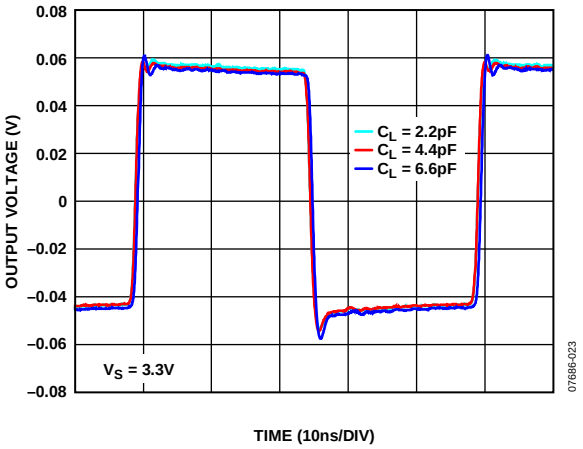


Figure 23. Small Signal Transient Response vs. Capacitive Load

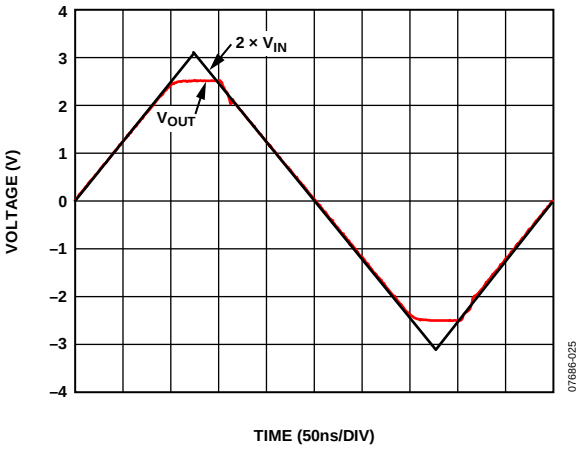


Figure 24. Output Overdrive Recovery

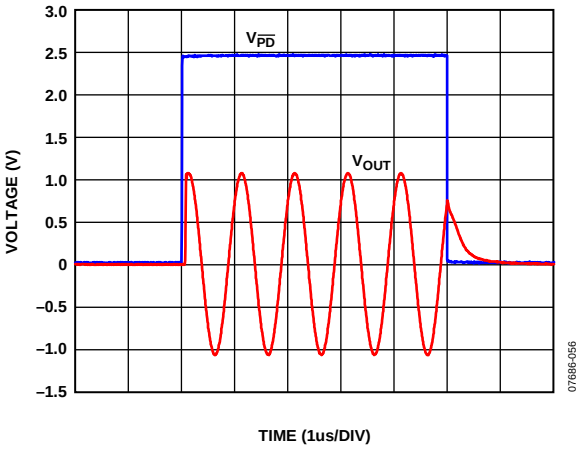


Figure 25. Turn-On/Turn-Off Time

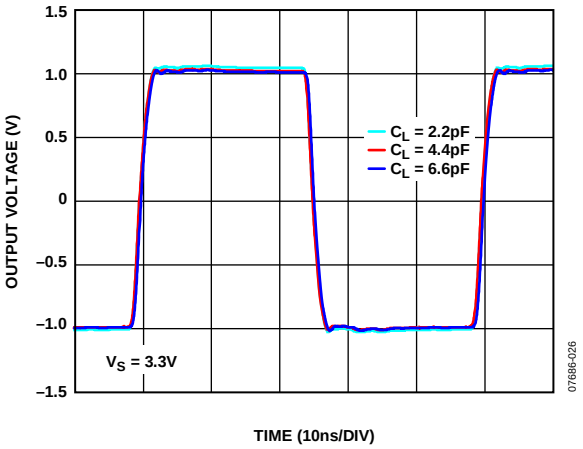
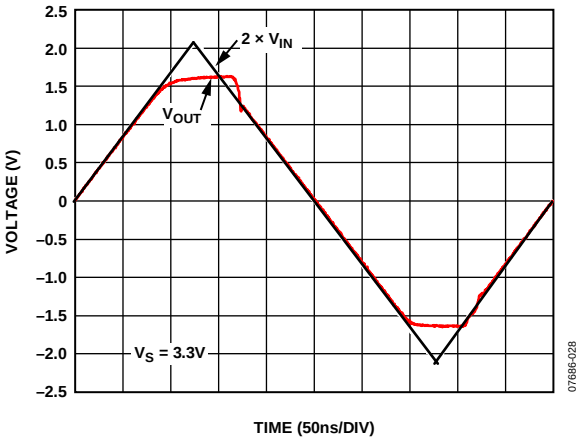


Figure 26. Large Signal Transient Response vs. Capacitive Load



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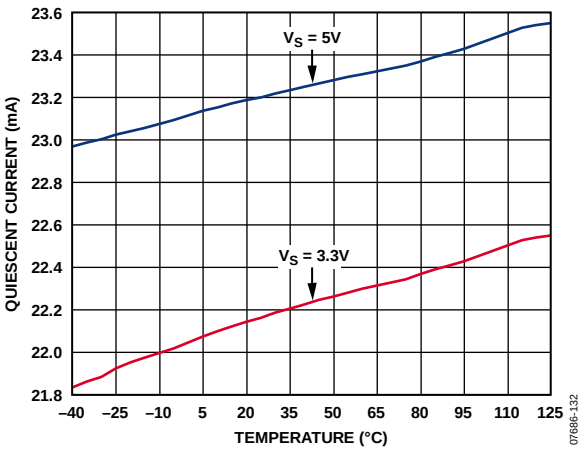


Figure 28. Quiescent Current vs. Temperature

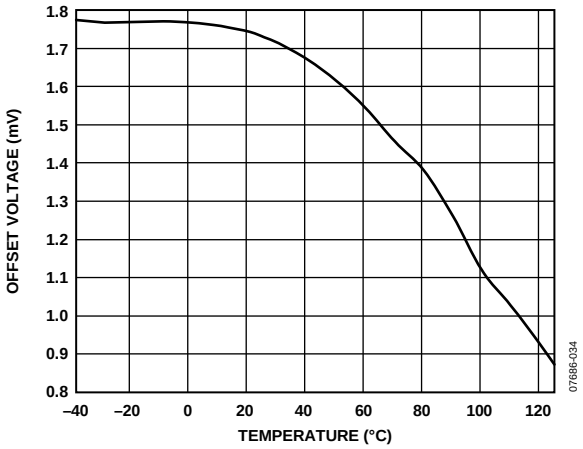


Figure 29. Offset Drift vs. Temperature

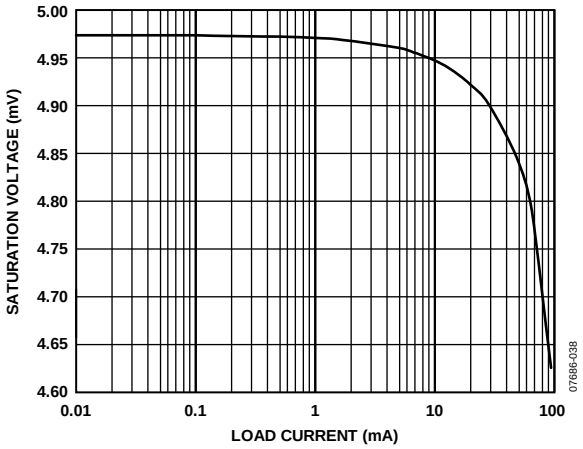


Figure 31. Output Saturation Voltage vs. Load Current

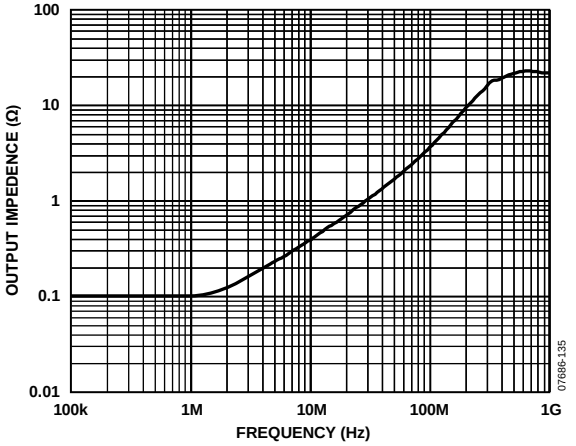


Figure 30. Output Impedance vs. Frequency

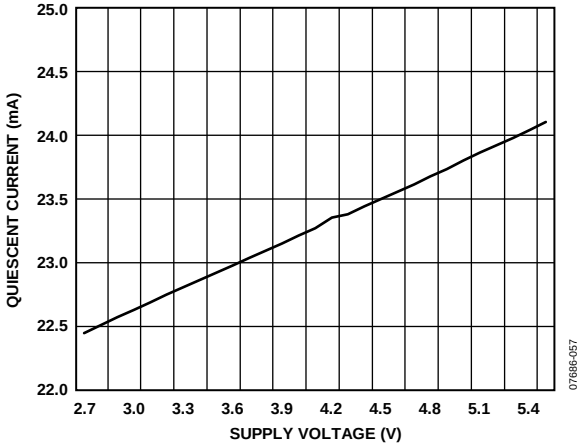


Figure 32. Quiescent Current vs. Supply Voltage

THEORY OF OPERATION

The ADA4856-3 is a voltage feedback op amp that employs a new input stage that achieves a high slew rate while maintaining a wide common-mode input range. The input common-mode range of the ADA4856-3 extends from 200 mV below the negative rail to about 1 V from the positive rail. This feature makes the ADA4856-3 ideal for low voltage single-supply applications. In addition, this new input stage does not sacrifice noise performance for slew rate. At 14 nV/√Hz, the ADA4856-3 is one of the lowest noise rail-to-rail output video amplifiers in the market.

Besides a novel input stage, the ADA4856-3 employs the Analog Devices, Inc., patented rail-to-rail output stage. This output stage makes an efficient use of the power supplies, allowing the op amp to drive up to three video loads to within 300 mV from both rails. In addition, this output stage provides the amplifier with very fast overdrive characteristics, an important property in video applications.

The ADA4856-3 comes in a 16-lead LFCSP that has an exposed thermal pad for lower operating temperature. This pad is connected internally to the negative rail. To avoid printed circuit board (PCB) layout problems, the ADA4856-3 features a new pinout flow that is optimized for video applications. As shown in Figure 4, the feedback and gain resistors are on-chip, which minimizes the number of components needed and improves the design layout. The ADA4856-3 is fabricated in Analog Devices dielectrically isolated eXtra Fast Complementary Bipolar 3 (XFCB3) process, which results in the outstanding speed and dynamic range displayed by the amplifier.

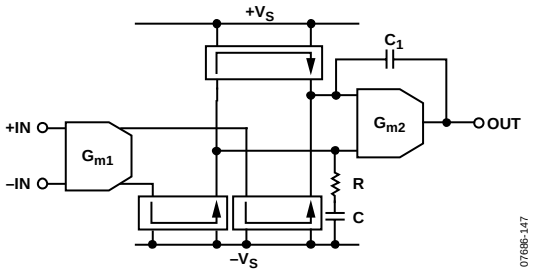


Figure 33. High Level Design Schematic

APPLICATIONS INFORMATION

USING THE ADA4856-3 IN GAINS EQUAL TO +1, −1

The ADA4856-3 was designed to offer outstanding video performance, simplify applications, and minimize board area.

The ADA4856-3 is a triple amplifier with on-chip feedback and gain set resistors. The gain is fixed internally at G = +2. The inclusion of the on-chip resistors not only simplifies the design of the application but also eliminates six surface-mount resistors, saving valuable board space and lowering assembly costs. Whereas the ADA4856-3 has a fixed gain of G = +2, it can be used in other gain configurations, such as G = −1 and G = +1.

Unity-Gain Operation

Option 1

There are two options for obtaining unity gain (G = +1). The first is shown in Figure 34. In this configuration, the –IN input pin is tied to the output (feedback is now provided with the two internal 402 Ω resistors in parallel), and the input is applied to the noninverting input. The noise gain for this configuration is 1.

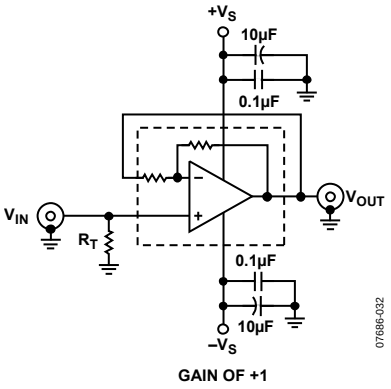


Figure 34. Unity Gain of Option 1

Option 2

Another option exists for running the ADA4856-3 as a unity-gain amplifier. In this configuration, the noise gain is +2, see Figure 35. The frequency response and transient response for this configuration closely match the gain of +2 plots because the noise gains are equal. This method does have twice the noise gain of Option 1; however, in applications that do not require low noise, Option 2 offers less peaking and ringing. By tying the inputs together, the net gain of the amplifier becomes 1. Equation 1 shows the transfer characteristic for the schematic shown in Figure 35.

$$V_{OUT} = V_{IN}\left(\frac{-R_F}{R_G}\right) + V_{IN}\left(\frac{R_F + R_G}{R_G}\right) \quad (1)$$

which simplifies to $V_{OUT} = V_{IN}$.

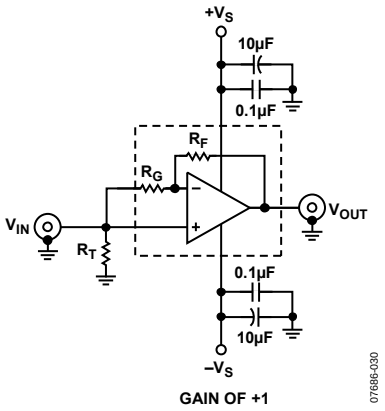


Figure 35. Unity Gain of Option 2

Inverting Unity-Gain Operation

In this configuration, the noninverting input is tied to ground and the input signal is applied to the inverting input. The noise gain for this configuration is +2, see Figure 36.

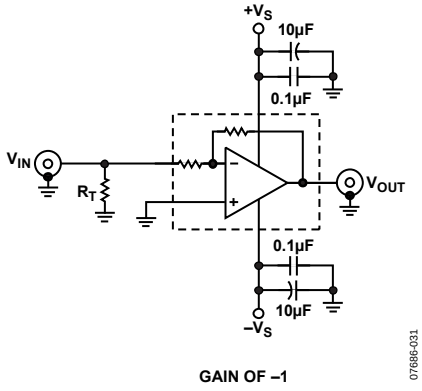


Figure 36. Inverting Configuration (G = −1)

Figure 37 shows the small signal frequency response for both gain of +1 (Option 1 and Option 2) and gain of −1 configurations. It is clear that G = +1, Option 2 has better flatness and no peaking compared to Option 1.

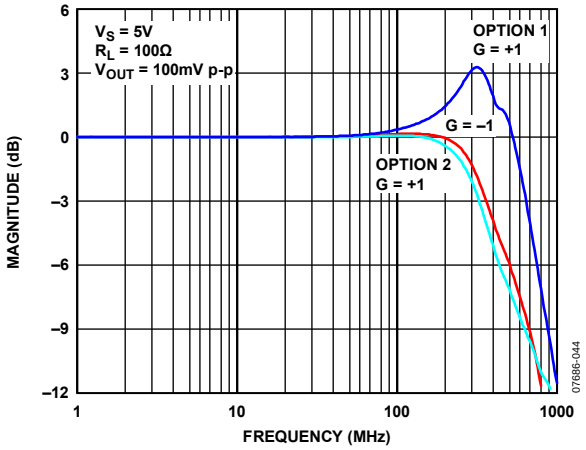


Figure 37. G = +1 and G = −1

USING THE ADA4856-3 IN GAINS EQUAL TO +3, +4, AND +5

Depending on certain applications, it might be useful to have a fixed gain amplifier that can provide various gains. The advantage of having a fixed gain amplifier is the ease of layout, the reduced number of components needed, and the matching of the gain and feedback resistors.

Gain of +3 Configuration

Figure 38 shows the ADA4856-3 used as an amplifier with a fixed gain of +3. No external resistors are required, just a simple trace connecting certain inputs and outputs. Connect V_{IN} to U1, which is set to a gain of +2, and U2, which is set to unity. U3 then takes the output of U1 and gains it up by +2 and subtracts the output of U2 to produce V_{OUT}. As shown in Figure 41, the large signal frequency response for G = +3 is flat out to 65 MHz, with a bandwidth of 165 MHz, a 2 V p-p output voltage, and a 100 Ω load.

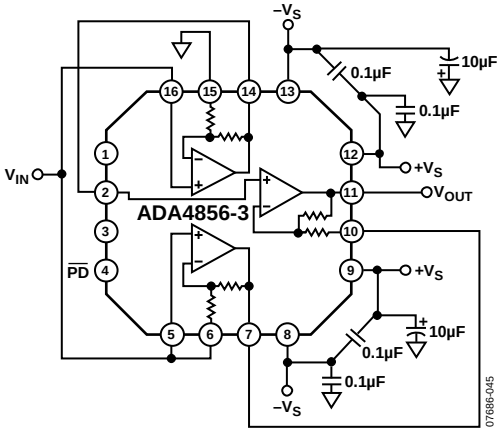


Figure 38. Gain of +3

Gain of +4 Configuration

To get a gain of +4, set one amplifier to a gain of +1 and set the other two amplifiers to a gain of +2. Figure 39 shows V_{IN} going in U2 at unity, then U1 takes the output of U2 and gains it by +2, and then feeds it to U3, which also gains it by +2 to produce V_{OUT}.

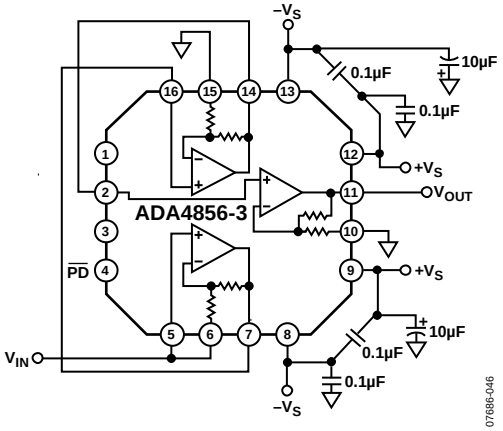


Figure 39. Gain of +4

As shown in Figure 41, the large signal frequency response for G = +4 is also flat out to 65 MHz, and it has a bandwidth of 180 MHz.

Gain of +5 Configuration

The gain of +5 is very similar to the G = +3 configuration but with U2 set to a gain of −1, which ends up being added to twice the output of U1 to generate V_{OUT} with G = +5.

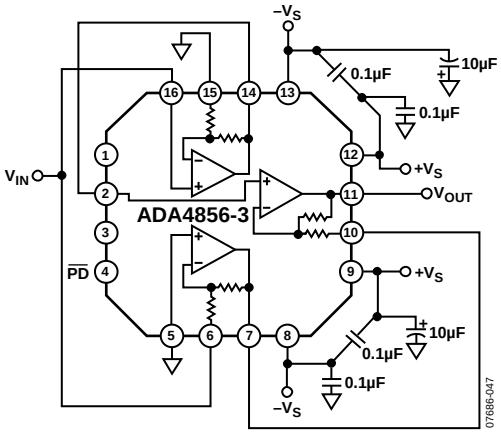


Figure 40. Gain of +5

Figure 41 shows the large signal frequency response of the three closed-loop gain sets (+3, +4, and +5) with flatness that extends to 65 MHz and a −3 dB bandwidth of 190 MHz.

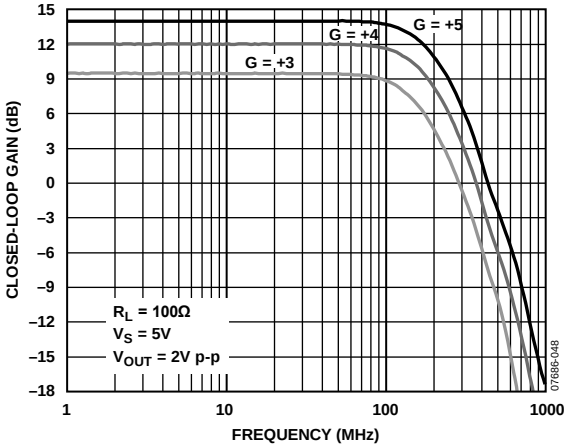


Figure 41. Large Signal Frequency Response for All Three Gains

20 MHz ACTIVE LOW-PASS FILTER

The ADA4856-3 triple amplifier lends itself to higher order active filters. Figure 42 shows a 20 MHz, 6-pole, Sallen-Key low-pass filter.

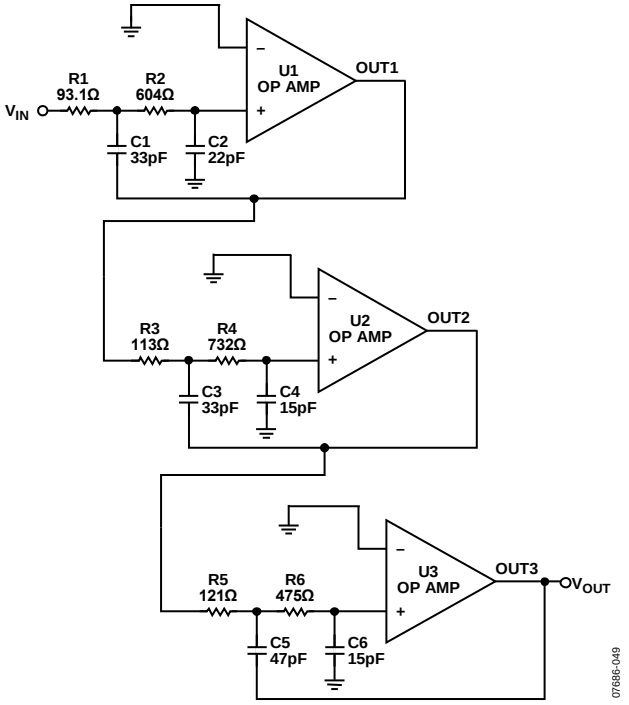


Figure 42. 20 MHz, 6-Pole Low-Pass Filter

The filter has a gain of approximately 18 dB, which is set by three fixed gain of 2 stages, and a flat frequency response out to 14 MHz. This type of filter is commonly used at the output of a video DAC as a reconstruction filter. The frequency response of the filter is shown in Figure 43.

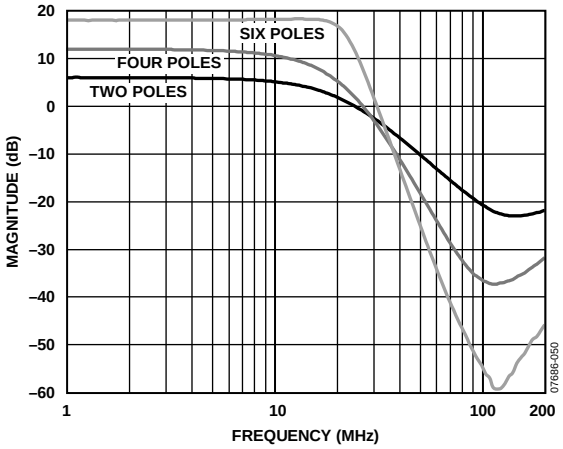


Figure 43. 20 MHz, Low-Pass Filter Frequency Response

VIDEO LINE DRIVER

The ADA4856-3 was designed to excel in video driver applications. Figure 44 shows a typical schematic for a video driver operating on bipolar supplies.

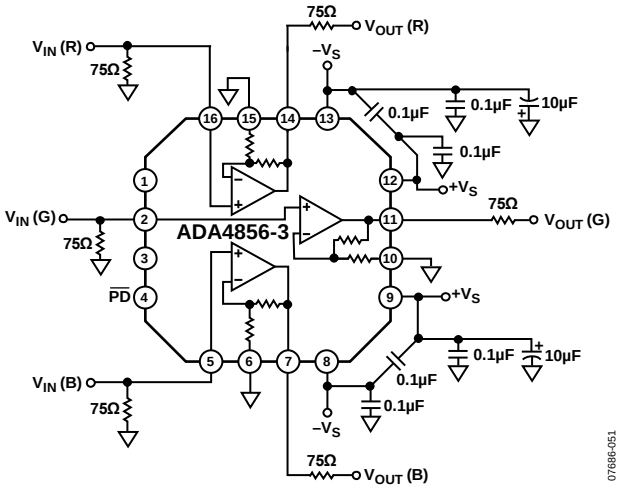


Figure 44. Video Driver Schematic

In applications that require multiple video loads be driven simultaneously, the ADA4856-3 can deliver. Figure 45 shows the ADA4856-3 configured with triple video loads. Figure 46 shows the triple video load performance.

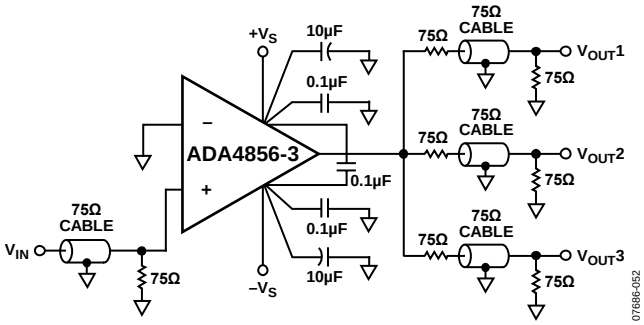


Figure 45. Video Driver Schematic for Triple Video Loads

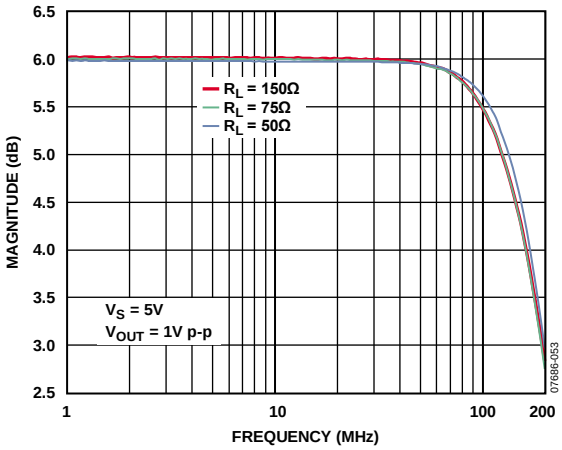


Figure 46. Large Signal Frequency Response for Various Loads

SINGLE-SUPPLY OPERATION

The ADA4856-3 can operate in single-supply applications. Figure 47 shows the schematic for a single 5 V supply video driver. Resistors R2 and R4 establish the midsupply reference. Capacitor C2 is the bypass capacitor for the midsupply reference. Capacitor C1 is the input coupling capacitor, and C6 is the output coupling capacitor. Capacitor C5 prevents constant current from being drawn through the internal gain set resistor. Resistor R3 sets the ac input impedance of the circuit.

For more information on single-supply operation of op amps, see "Avoiding Op-Amp Instability Problems In Single-Supply Applications", Analog Dialogue, Volume 35, Number 2, March-May, 2001, at www.analog.com.

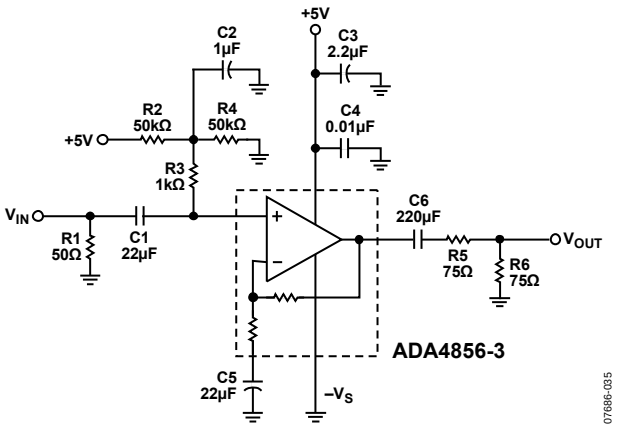


Figure 47. AC-Coupled, Single-Supply Video Driver Schematic

In addition, the ADA4856-3 can be configured in dc-coupled, single-supply operation. The common-mode input voltage can go about 200 mV below ground, which makes it a true single-supply part. However, in video applications, the black level is set at 0 V, which means that the output of the amplifier must go to the ground level as well. This part has a rail-to-rail output stage; it can go as close as 100 mV from either rail. Figure 48 shows the schematic for adding 50 mV dc offset to the input signal so that the output is not clipped while still properly terminating the input with 75 Ω.

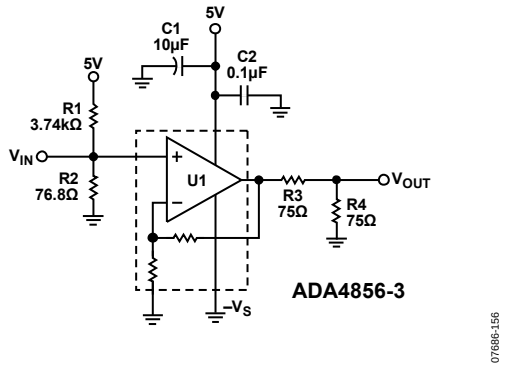


Figure 48. DC-Coupled Single Supply Video Driver Schematic

POWER DOWN

The ADA4856-3 is equipped with a $\overline{PD}$ (power-down) pin for all three amplifiers. This allows the user to reduce the quiescent supply current when an amplifier is inactive. The power-down threshold levels are derived from the voltage applied to the $+V_S$ pin. When used in single-supply applications, this is especially useful with conventional logic levels. The amplifier is enabled when the voltage applied to the $\overline{PD}$ pin is greater than $+V_S - 1.25$ V. In a 5 V single-supply application, the typical threshold voltage is +3.75 V, and in a 3.3 V dual-supply application, the typical threshold voltage is +2 V. The amplifier is also enabled when the $\overline{PD}$ pin is left floating (not connected). However, the amplifier is powered down when the voltage on the $\overline{PD}$ pin is lower than 2.5 V from $+V_S$. If the $\overline{PD}$ pin is not used, it is best to connect it to the positive supply

Table 6. Power-Down Voltage Control

$\overline{PD}$ Pin	5 V	±2.5 V	3.3 V
Not Active	>3.75 V	>1.25 V	>2.05 V
Active	<2 V	<0 V	<1.3 V

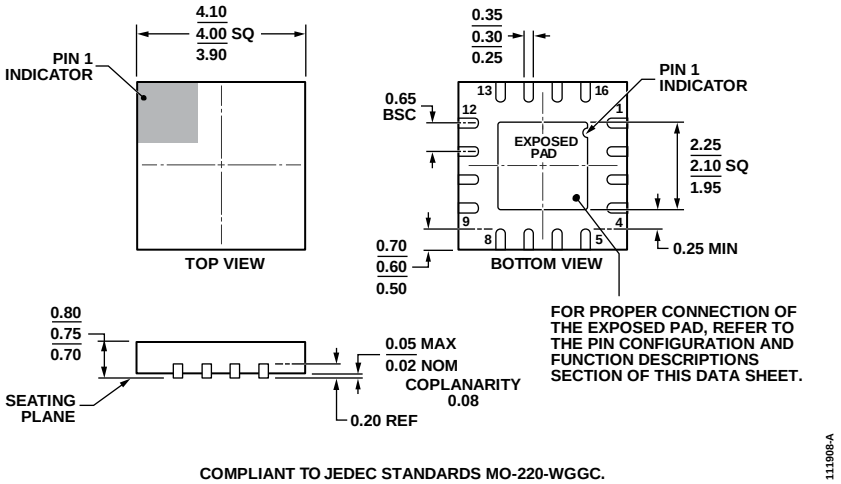
LAYOUT CONSIDERATIONS

As is the case with all high speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. Proper RF design technique is mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near the input and output pins reduces stray capacitance. Locate termination resistors and loads as close as possible to their respective inputs and outputs. Keep input and output traces as far apart as possible to minimize coupling (crosstalk) though the board. Adherence to microstrip or stripline design techniques for long signal traces (greater than about 1 inch) is recommended.

POWER SUPPLY BYPASSING

Careful attention must be paid to bypassing the power supply pins of the ADA4856-3. Use high quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), to minimize supply voltage ripple and power dissipation. A large, usually tantalum, 10 µF to 47 µF capacitor located in proximity to the ADA4856-3 is required to provide good decoupling for lower frequency signals. In addition, locate 0.1 µF MLCC decoupling capacitors as close to each of the power supply pins as is physically possible, no more than 1/8 inch away. The ground returns should terminate immediately into the ground plane. Locating the bypass capacitor return close to the load return minimizes ground loops and improves performance.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 49.16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4856-3YCPZ-R2	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-23	250
ADA4856-3YCPZ-R7	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-23	1,500
ADA4856-3YCPZ-RL	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-23	5,000
ADA4856-3YCP-EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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D07686-0-3/13(B)

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