

# XDPL8220 Digital PFC+Flyback Controller IC

## XDP™ Digital Power

Data Sheet

Revision 1.0

Quality Requirement Category: Industrial

## Features

- Universal AC input (90 - 305 VAC) or DC input (90 - 305 VDC)
- Applicable power range of 20 W to 150 W
- Small number of external parts optimizes **Bill of Materials (BOM)** and form factor
- High efficiency (> 90%)
- Multicontrol mode (**Constant Current (CC)/Constant Voltage (CV)/Limited Power (LP)**) reduces required product variety
- Important parameters can be configured after manufacturing
- Low harmonic distortion (**Total Harmonic Distortion (THD)** < 15%)
- Low output ripple current
- Integrated startup cell ensures fast time to light (< 250 ms)
- Adaptive Temperature Protection
- Ambient operating temperature -40 °C to 85 °C
- Automatic switching between **Quasi-Resonant Mode (QRM)** and **Discontinuous Conduction Mode (DCM)**
- Wide output voltage range
- **Pulse Width Modulation (PWM)** dimming control
- Output dimming by analog reduction of driving current down to 5%

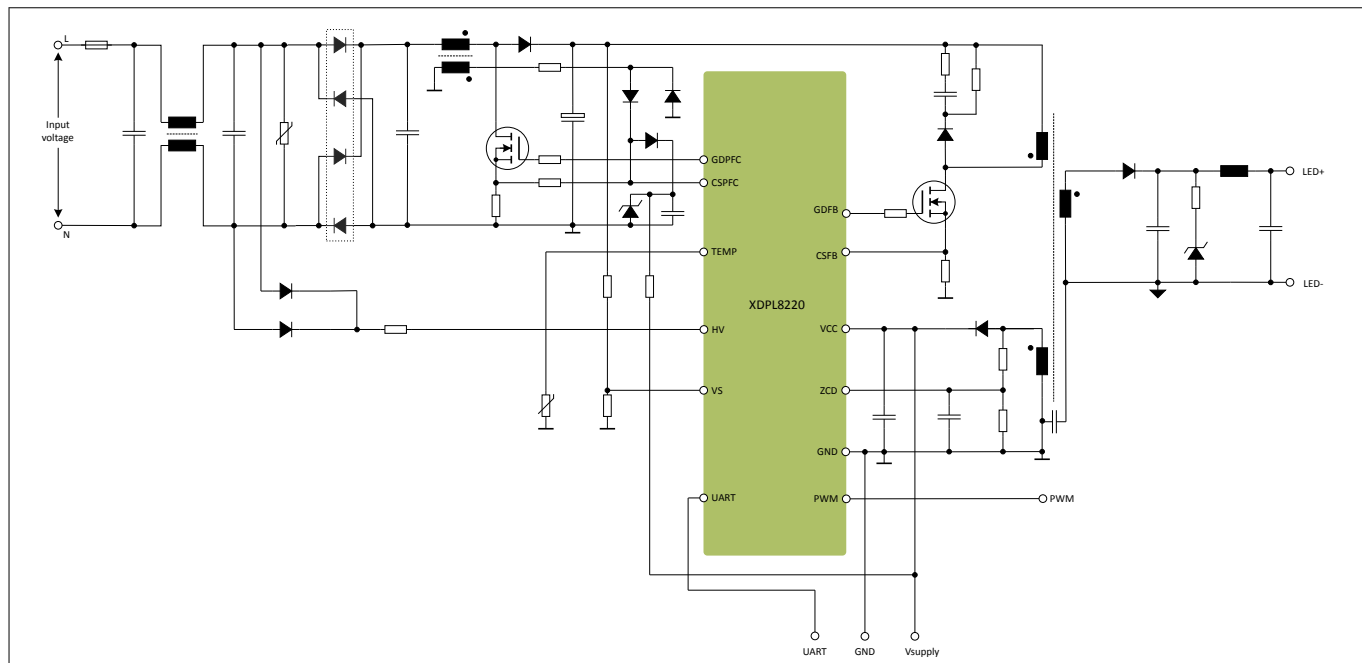
For safe operation, the XDPL8220 contains a comprehensive set of protection features:

- Output overvoltage protection (open load)
- Output undervoltage protection (output short)
- VCC over- and undervoltage lockout
- Input over- and undervoltage protection
- Bus over- and undervoltage protection
- Overcurrent protection for **Power Factor Correction (PFC)** and **Flyback (FB)** stage

## Applications

- Integrated **Electronic Control Gear (ECG)** for **Light Emitting Diode (LED)** luminaires

**Description**



**Figure 1 Typical Application for XDPL8220**

Product Type	Package
XDPL8220	PG-DSO-16

**Description**

XDPL8220 is a highly integrated next-generation device combining a boundary mode **PFC** plus a quasi-resonant **FB** controller with primary-side regulation. The integration of these functions enables saving of external parts and optimizes performance by harmonized operation of the two stages.

XDPL8220 uses a constant on-time scheme with a **THD** improvement algorithm to provide a high power factor and excellent **THD** performance.

With its unique control scheme of **CV**, **CC** and **LP**, the **LED** driver designer is provided with a large degree of flexibility and can utilize the system hardware to its limits.

The on-chip **One Time Programmable Memory (OTP)** memory has an area for parameters that control the behavior of the circuit, e. g. the output current or the maximum output power. This enables the user of the device to create a platform concept with significantly fewer different hardware versions while still covering the same application range.

The two-stage approach reduces any variation in the output current (flicker) to a non-visible level. By separating the **PFC** from the power conversion part (**FB**), both stages operate in a more stable manner and require fewer margins, which has a positive influence on the cost.

Lighting requires more and more 24/7 operation, making it necessary to have a stand-by mode with short wake-up times and low power consumption. The power consumption of less than 100 mW of the XDPL8220-based systems defines the new standard for stand-by power in lighting **ECGs**.

XDPL8220 enables adaptive temperature protection using either the internal sensor or an external **Negative Temperature Coefficient Thermistor (NTC)**, or both.

Futureproof flexibility with application-oriented programmable operating windows enables management of **LED** generations and portfolio complexity .

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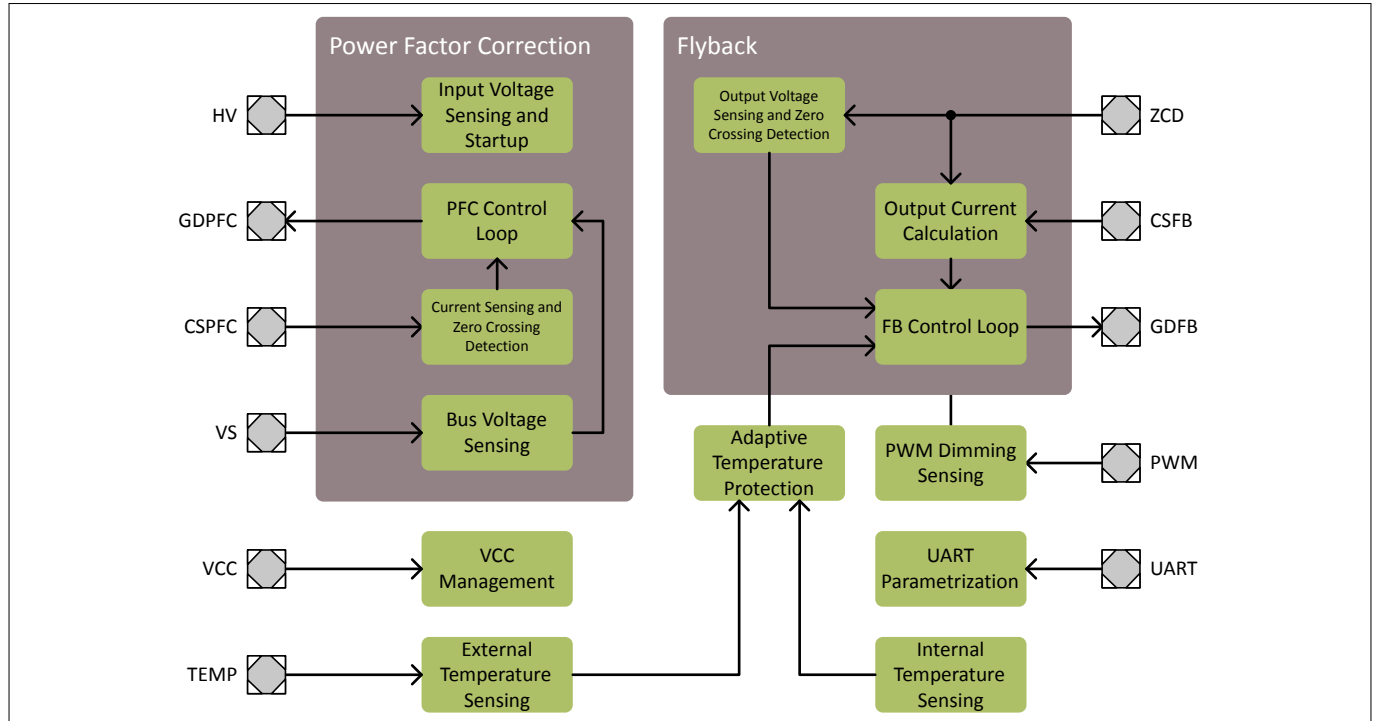
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**Functional Block Diagram**

**1 Functional Block Diagram**

The functional block diagram shows the basic data flow from input pins via signal processing to the output pins.

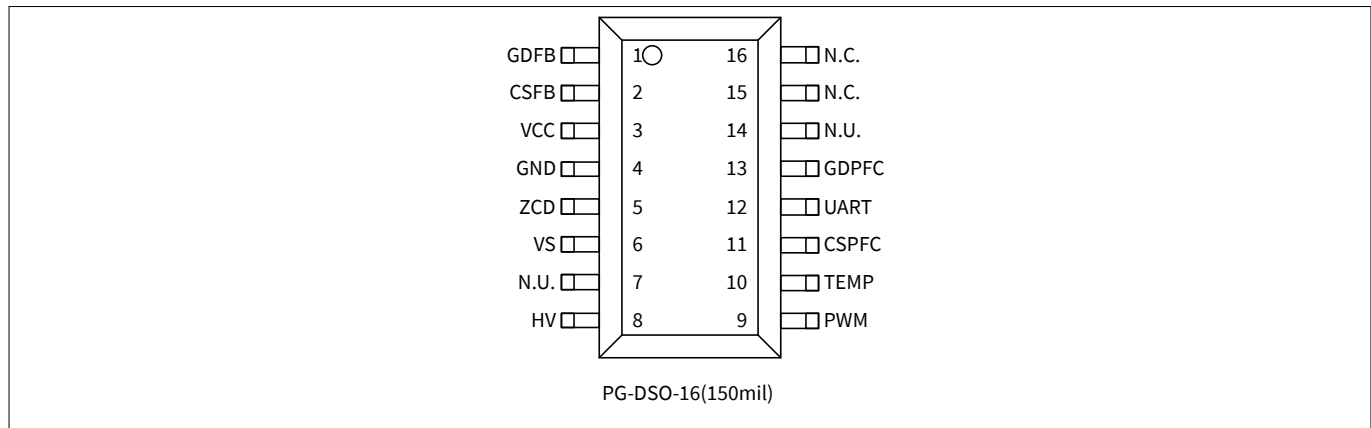


**Figure 2 XDPL8220 Simplified Functional Block Diagram**

**Pin Configuration**

## 2 Pin Configuration

Pin assignments and basic pin description information are shown below.



**Figure 3 Pinning of XDPL8220**

**Table 1 Pin Definitions and Functions**

Name	Pin	Type	Function
GDFB	1	O	Gate driver for <b>FB</b> : The GDFB pin is an output for directly driving a power MOSFET of the <b>FB</b> stage.
CSFB	2	I	Current sensing for <b>FB</b> : The CSFB pin is connected to an external shunt resistor and the source of the power MOSFET of the <b>FB</b> stage.
VCC	3	I	Voltage supply
GND	4	-	Power and signal ground
ZCD	5	I	Zero-crossing detection of the <b>FB</b> : The ZCD pin is connected to an auxiliary winding of the <b>FB</b> stage for zero-crossing detection as well as primary-side output voltage and backup bus voltage sensing for safety.
VS	6	I	Bus voltage sensing
N.U.	7	-	Not used. Externally to be connected to GND.
HV	8	I	High voltage: The HV pin is connected to the rectified input voltage via an external resistor. An internal 600 V HV startup-cell is used to initially charge VCC. In addition, sampled high-voltage sensing is also used for synchronization with the input frequency.
PWM	9	I	<b>PWM</b> dimming: The PWM pin is used as a dimming input.
TEMP	10	I	External temperature sensor: Measurement of external temperature using an <b>NTC</b> .
CSPFC	11	I	Current sensing for <b>PFC</b> : The CSPFC pin is connected to an external shunt resistor and the source of the power MOSFET of the <b>PFC</b> stage.

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## Pin Configuration

**Table 1 Pin Definitions and Functions (continued)**

Name	Pin	Type	Function
UART	12	I/O	<i>Universal Asynchronous Receiver Transmitter (UART)</i> communication: The UART pin is used for the <i>UART</i> interface to support parameterization.
GDPFC	13	O	Gate driver for <i>PFC</i> : The GDPFC pin is an output for directly driving a power MOSFET of the <i>PFC</i> stage.
N.U.	14	-	Not used. Externally to be connected to GND.
N.C.	15	-	Not connected.
N.C.	16	-	Not connected.

### **3 Functional Description**

This chapter provides a summary of the integrated functions and features, and describes the relationships between them. The parameters and equations are based on typical values at  $T_A = 25\text{ }^\circ\text{C}$ .

XDPL8220 is a digital dual-stage **PFC** and **FB** controller IC supporting **PWM** dimming functionality. Both stages use configurable multimode operation to select the best mode of operation for every operation condition. Multimode operation automatically switches between **Quasi-Resonant Mode, switching in valley n (QRMn)** and **DCM**.

XDPL8220 features a comprehensive set of configurable protection modes to detect fault conditions.

XDPL8220 provides a high degree of flexibility in design-in of the application. A **Graphic User Interface (GUI)** tool supports users in the configuration of the operational and protection parameters.



**Functional Description**

**3.1 PFC Controller Features**

The **PFC** stage ensures high power quality by maximizing the power factor and minimizing harmonic distortion.

The **PFC** stage operates in **Quasi-Resonant Mode, switching in valley 1 (QRM1)** and **QRMn**, to support low load conditions and ensure efficient operation.

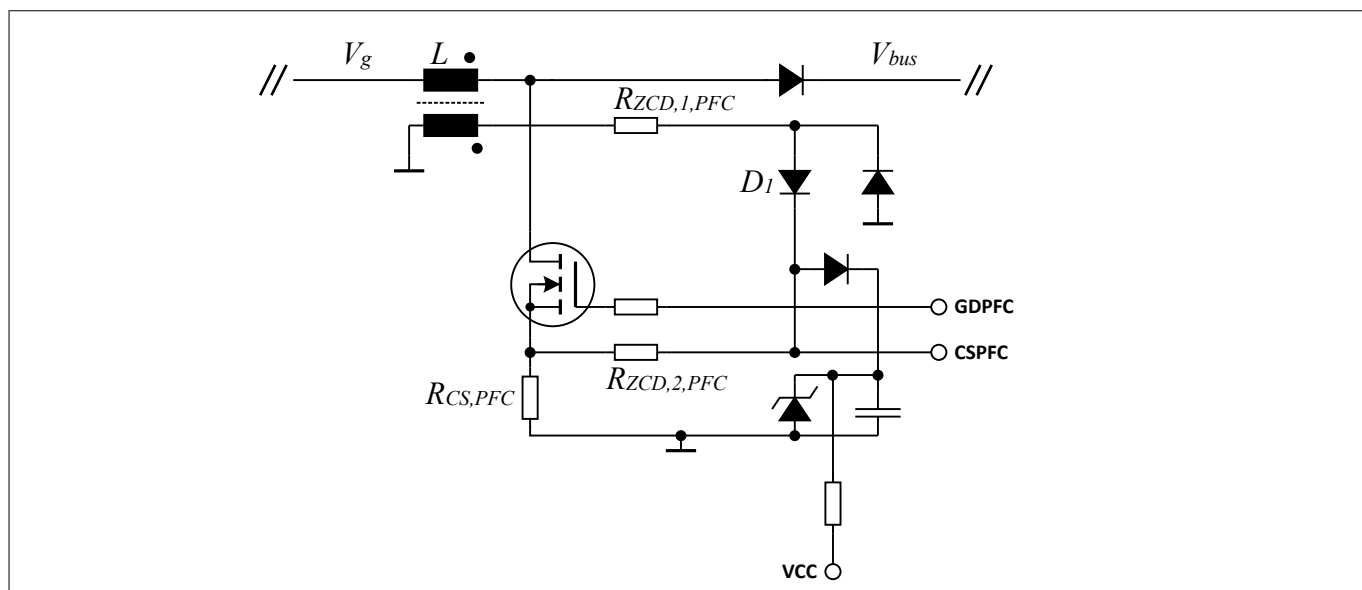
The **PFC** stage is implemented as a boost converter. It drains a sinusoidal current from the single-phase line supply and provides stabilized **Direct Current (DC)** voltage at the internal bus voltage rail. The power factor of the single-phase line supply is almost one. Fluctuations in line voltage as well as voltage drops of short duration are compensated.

**3.1.1 Shared CS/ZCD Function**

The **PFC** stage makes use of combined CS/ZCD functionality at the CSPFC pin.

During the gate driver on-time the pin acts as a current sense (CS), while during the gate driver off-time the pin acts as a zero-crossing-detector (ZCD). The CS senses the on-time current and implements overcurrent limitation; the ZCD exploits the quasi-resonant function to minimize conduction losses.

The CSPFC pin is connected via a resistor divider composed of  $R_{ZCD,1,PFC}$  and  $R_{ZCD,2,PFC}$  and a set of diodes to an auxiliary winding of the **PFC** choke inductor. It is used for detecting the valleys of the quasi-resonant oscillation to turn on the **PFC** MOSFET based on the desired valley computed by the multimode **PFC** control. The diode  $D_1$  allows positive voltage at the CSPFC pin as the valley detection is implemented by the internal hysteretic comparator with a positive reference of nominal  $THR_{HYS}$  for falling edges. The CSPFC pin senses the drain source current of the switching MOSFET. The CS voltage is measured after a programmable blanking time after turn-on of the switch. An appropriate current sensing resistor  $R_{CS,PFC}$  is selected on the basis of the maximum current flowing in the switching MOSFET and the dynamic voltage range of the input pin CSPFC.



**Figure 4 Shared CS/ZCD Schematic**

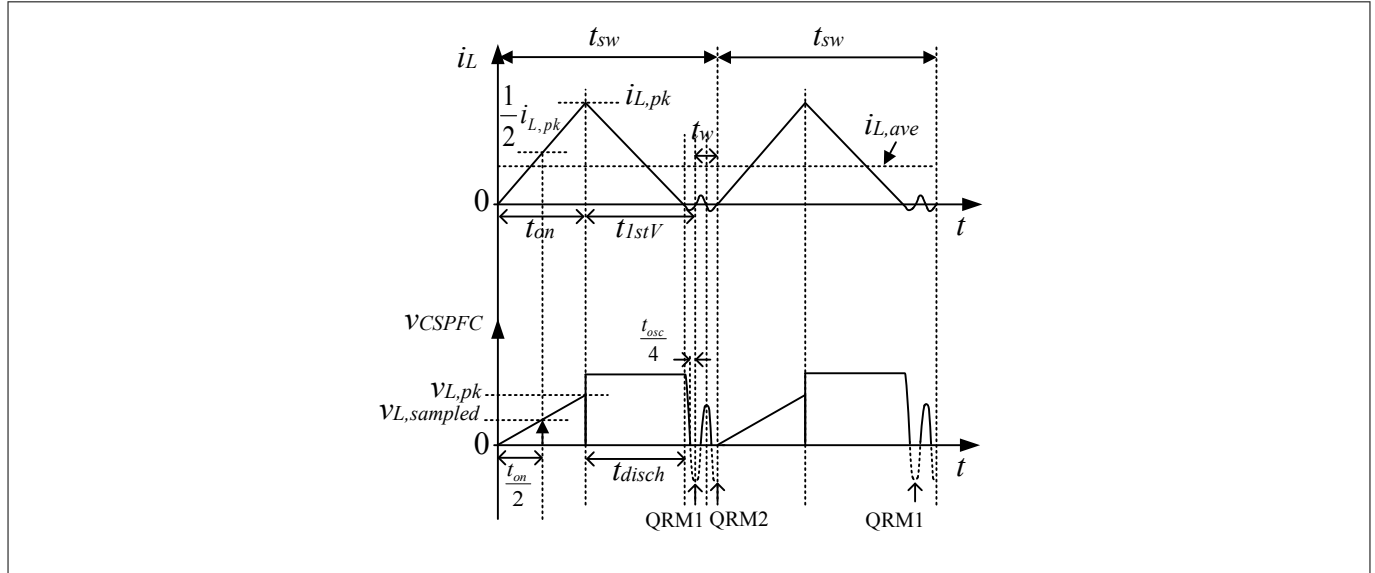
**3.1.2 Quasi-resonant Mode**

The quasi-resonant mode maintains a high efficiency level.

For **PFC** operating in **QRM1**, the main switch is turned on with a constant on-time for a line and load condition, while the off-time/demagnetization time varies within an **Alternating Current (AC)** half-cycle depending on the instantaneously rectified **AC** input voltage  $V_g$ . Subsequently, the switching frequency varies within each **AC** half-cycle with the lowest switching frequency at the peak of the **AC** input voltage and the highest switching frequency near the zero crossings of the input voltage. A new switching cycle starts immediately when the first QR valley is reached.

**Functional Description**

**QRM1** is ideal for full-load operation, where the on-time is large. However, the on-time reduces at light loads, resulting in very high switching frequencies, particularly near the zero crossings of the input voltage. The high switching frequency will increase switching losses, resulting in poor efficiency at light loads. The **PFC** multimode control can lower the switching frequency by selecting further valleys to achieve **QRM2** up to  $N_{\text{valley,max,PFC}}$  operation. The switching frequency is limited within a defined range and the efficiency at light loads improves.



**Figure 5 PFC QRM2 Waveforms**

The equations for the quasi-resonant operation are shown below, where  $t_w$  is an additional delay in each switching cycle when selecting subsequent valleys after the first QR valley and  $n$  is the valley number in **QRMn**.

$$\begin{aligned}
 i_{L,pk} &= \frac{V_g \cdot t_{on}}{L} \\
 t_{disch} &= \frac{i_{L,pk} \cdot L}{V_{bus} - V_g} \\
 t_{1stV} &= t_{disch} + t_{osc}/2 \\
 t_w &= t_{osc} \cdot (n - 1) \\
 t_{sw} &= t_{on} + t_{1stV} + t_w \\
 t_{off} &= t_{1stV} + t_w
 \end{aligned}$$

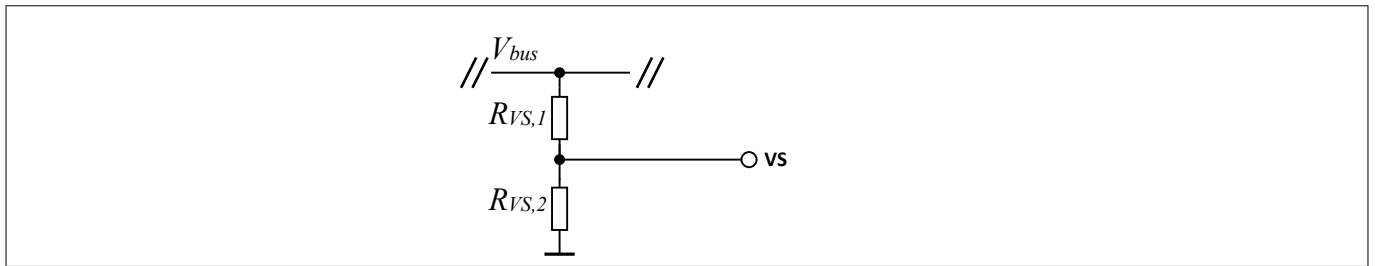
**Equation 1**

**3.1.3 Bus Voltage Sensing**

The bus voltage is measured at the VS pin.

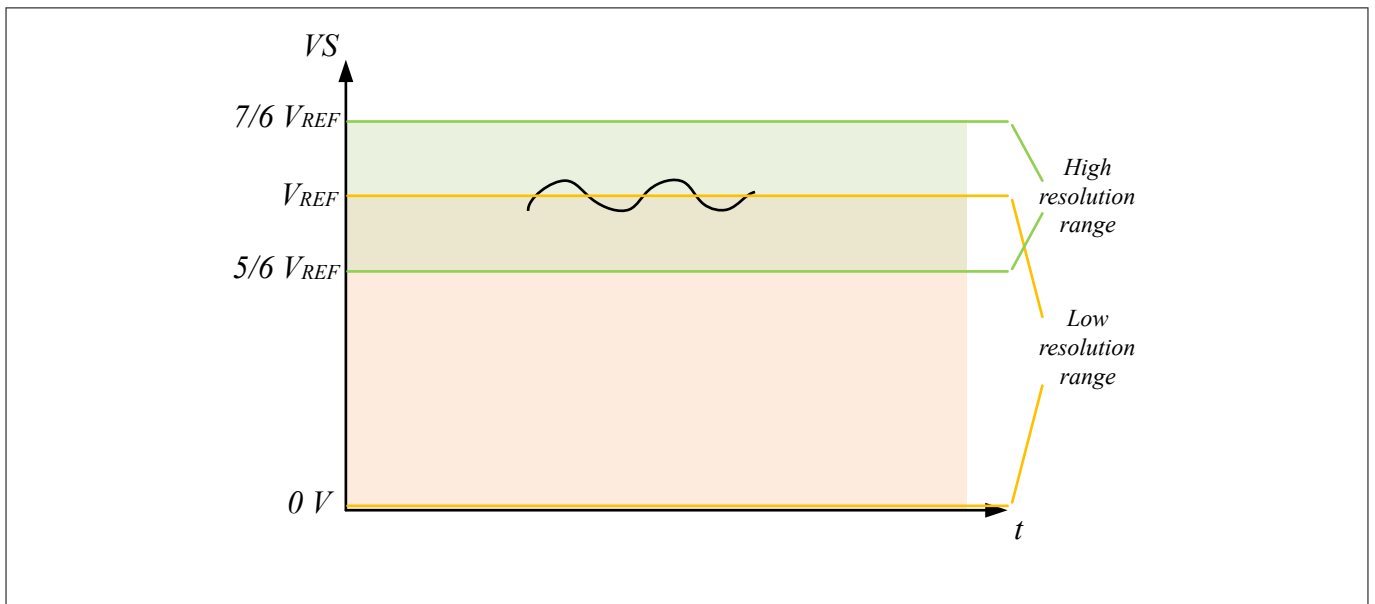
The VS pin implements **PFC** bus voltage sensing for bus voltage regulation. The bus voltage is scaled down using a simple resistor divider. A capacitor could in certain cases be added at the pin to ground to filter high-frequency switching noise. The bus voltage sensing is a low leakage input and no additional measures are needed to reduce the current consumption.

**Functional Description**



**Figure 6 Bus Voltage Sensing Schematic**

The **Analog-to-Digital Converter (ADC)** input at the VS pin utilizes two voltage ranges. The wider voltage range from 0 to  $V_{REF}$  results in lower resolution. The narrower voltage range from  $5/6 V_{REF}$  to  $7/6 V_{REF}$  gives better voltage resolution. Steady state operation therefore normally takes place in the high-resolution range and soft start operation in the low-resolution range.



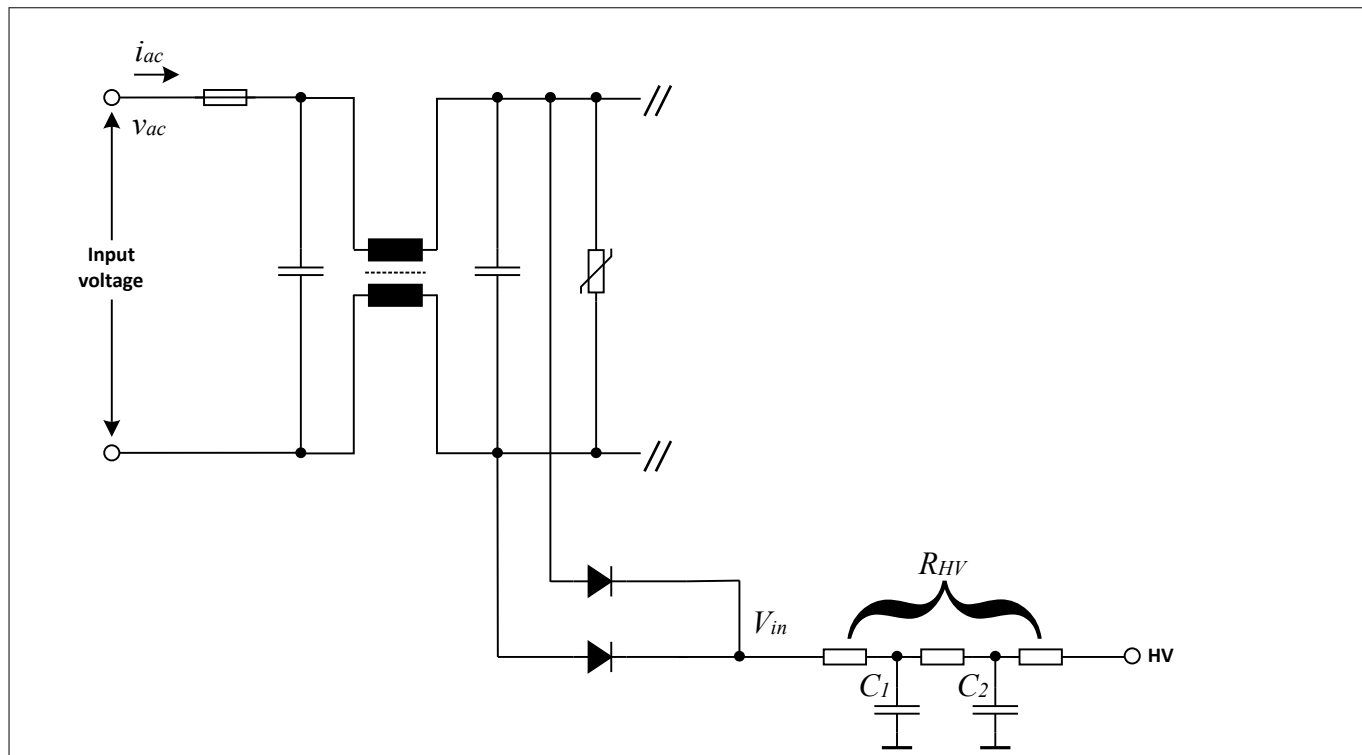
**Figure 7 Sensing Ranges**

**3.1.4 Input Voltage Sensing**

The input voltage is sensed using the HV pin.

The input voltage is used for protection, to generate **AC** zero-crossing signals and to detect the AC/DC source.

**Functional Description**



**Figure 8 Input Voltage Sensing Schematic**

The  $R_{HV}$  probing resistor is usually split into two, or three or more resistors for safety purposes. In fact in case of a resistor being shorted by damage, the high resistive path is maintained by the other resistors avoiding fire, shock to the user and further damage to the application.

A RC filter structure making use of the split resistors filters the unwanted noise for the high voltage input voltage measurement. The filtering effect is kept high due to the usage of the high impedance split resistors and the addition of small capacitance high voltage capacitors.

**3.1.5 Control Scheme**

The **PFC** bus voltage controller embeds a PIT1 controller that calculates a control output representing load and line conditions from the bus voltage error signal.

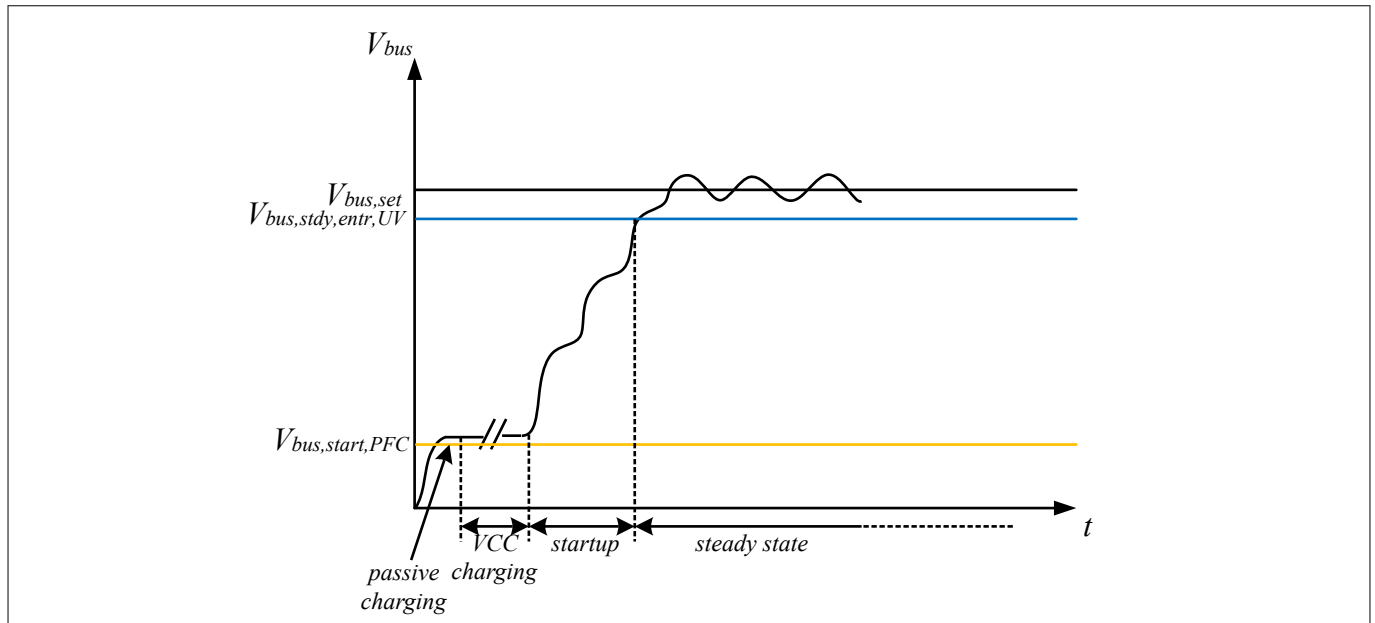
The bus voltage controller implements regulation during both soft start and steady states.

**3.1.5.1 Startup**

At system startup, the **PFC** initiates a soft start to minimize the switching stress for the power MOSFET, diode and inductor.

The soft start is executed when the bus voltage is higher than the  $V_{bus,start,PFC}$  threshold. This is the brown-in condition. The soft start is aborted if the input under- or overvoltage protection fire. During soft start, the **PFC** stays in **QRM1** operation. Once the  $V_{bus,steady,entr,UV}$  threshold is reached, the steady state **PFC** operation starts.

**Functional Description**



**Figure 9**  $V_{bus}$  Soft Start and Regulation

**3.1.6 Multimode Control Scheme**

The multimode control scheme provides a **PFC** option to dynamically change the operating point by switching between the MOSFET  $V_{ds}$  voltage valleys while following a frequency law and applying **THD** optimization.

The multimode controller uses two different modes of operation:

- **QRM1**: This operation maximizes the efficiency by switching on the 1st valley of the **PFC** ZCD signal. This ensures zero current switching with a minimum of switching losses.
- **QRMn**: The controller will extend to the next switching valley after the 1st valley to control the bus voltage following a frequency law.

The multimode optimization consists of the following:

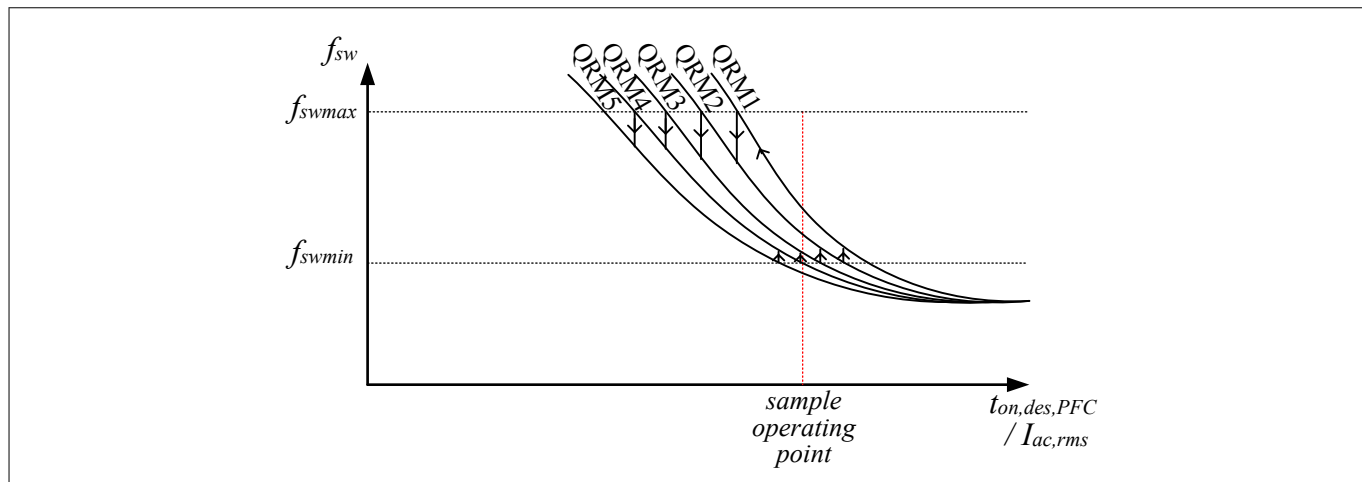
- Frequency law
- THD optimization

**3.1.6.1 Frequency Law**

The output of the **PFC** PIT1 bus voltage controller gives the desired on-time, which is constant within each **AC** half cycle. A **PFC** is used to emulate a resistive load  $r_e$  to the **AC** input such that  $i_{ac}$  follows  $v_{ac}$  in both wave shape and phase. The output of the **PFC** bus voltage controller  $t_{on,des,PFC}$  is inversely proportional to the emulated resistive load  $r_e$  such that a smaller  $r_e$  or a higher  $I_{ac,rms}$  will give a larger  $t_{on,des,PFC}$ . Thus,  $t_{on,des,PFC}$  is different for the same load at different line voltages and is proportional to the RMS input current  $I_{ac,rms}$ .

The rule for selecting **QRMn** is based on the frequency law. A maximum switching frequency  $f_{swmax}$  and a minimum switching frequency  $f_{swmin}$  are defined for the complete  $t_{on,des,PFC}/I_{ac,rms}$  range. The frequency law ensures that the switching frequency is within the desired frequency range. The frequency law is depicted in the figure below.

**Functional Description**



**Figure 10 PFC Frequency Law**

As long as the **PFC** controller operating mode fulfills the frequency law, the operating mode does not change. The QR-valley is increased when the highest frequency limit is reached. The QR-valley is decremented when the lowest frequency limit is reached.

To ensure good ZCD detection before the ZCD signal becomes too small in amplitude, only the first up to  $N_{valley,max,PFC}$  valleys operations are supported.

**3.1.6.2 THD Optimization**

**THD** optimization reduces the **THD** in the case of light loads and in the case of high **AC** input voltages.

The selection of higher valleys helps to reduce the switching frequency but it also distorts the input current waveform with constant on-time control and thus affects the **PFC THD** performance. The multimode **PFC** control also consists of a **THD** optimization algorithm that optimizes the applied on-time in order to ensure good input current shaping and improved **PFC THD** performance.

**3.1.7 Peak Current Limitation**

The peak current through the switching MOSFET is read via the **PFC** shunt resistor  $R_{CS,PFC}$  to limit the maximum current through the MOSFET, the choke, and freewheeling diode so as to avoid potential hard failure or lifetime stress.

The OCP causes the current to be limited to cases in which an overcurrent condition occurs. **Overcurrent Protection Level 1 (OCP1)** is implemented by hardware. If the voltage  $V_{CS,PFC}$  across the shunt resistor exceeds the overcurrent threshold  $V_{CS,OCP1,PFC}$  for longer than the blanking time  $t_{blank,OCP1,PFC}$ , the MOSFET is turned off. The MOSFET is turned on when ZCD occurs or the PFC maximum period time-out signal triggers the start of the next switching cycle. **Overcurrent Protection Level 2 (OCP2)** is a second-level overcurrent protection implemented by hardware. The **OCP2** overcurrent threshold is fixed. The **OCP2** blanking time is  $t_{blank,OCP2,PFC}$ .

**3.1.8 Bus Undervoltage Protection**

Undervoltage detection of the bus voltage  $V_{bus}$  is provided by measurement using the VS pin.

The bus voltage is compared to a configurable undervoltage protection threshold  $V_{bus,UV}$ . If the threshold is exceeded for longer than the blanking time  $t_{blank,Vbus,UV}$ , the protection will be triggered.

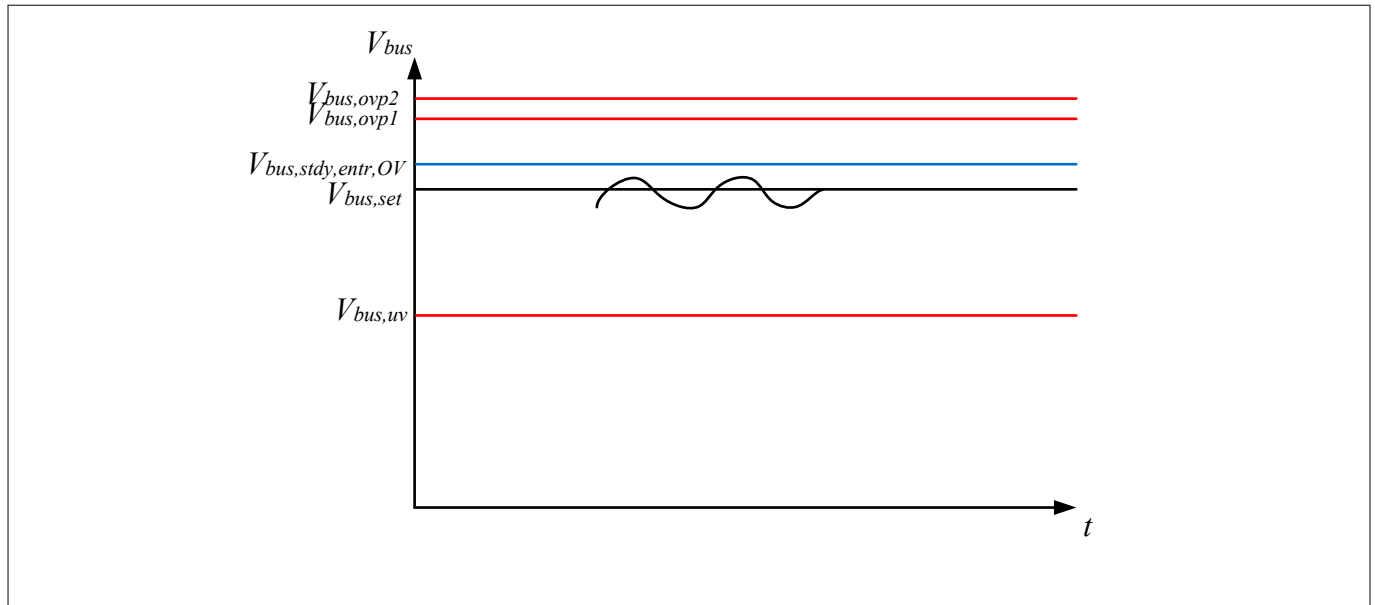
**Functional Description**

**3.1.9 Bus Overvoltage Protection**

Overvoltage detection of the bus voltage  $V_{bus}$  is provided by the measurement using the VS pin.

The bus voltage is compared to a configurable overvoltage protection threshold  $V_{bus,OV1}$  in **Firmware (FW)**. If a threshold is exceeded for longer than the blanking time  $t_{blank,Vbus,OV1}$ , the gate driver stops. The gate driver operation is resumed when  $V_{bus}$  falls below  $V_{bus,stdy,entr,OV}$ .

$V_{bus,OV2}$  is implemented in **Hardware (HW)** and it is fixed at a voltage which is represented as 2.8 V at the bus voltage sensing pin (VS). The HW permits a blanking time  $t_{blank,Vbus,OV2}$  to be programmed.



**Figure 11**  $V_{bus}$  protections

**3.1.10 Input Undervoltage Protection**

Undervoltage detection of the input voltage  $V_{in}$  is provided by measurement using the HV pin.

Values of  $V_{in,rms}$  are compared to a configurable input undervoltage protection threshold  $V_{in,UV}$ . If the threshold is exceeded for longer than the blanking time  $t_{blank,Vin,UV}$ , the protection will be triggered. XDPL8220 features a configurable startup threshold  $V_{in,start,min}$  to create hysteresis for flicker-free operation before the second stage starts switching. After startup checks when  $t_{rms,reset,PFC}$  expires, the comparison is restored to the threshold value  $V_{in,UV}$ .

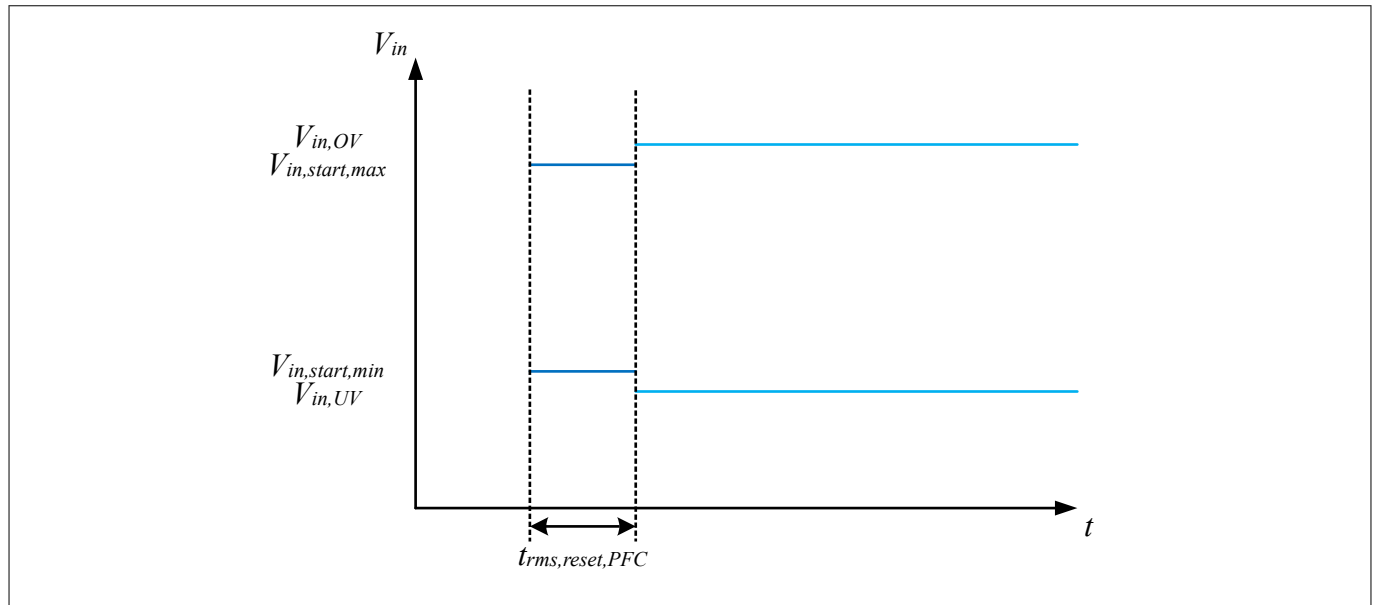
**3.1.11 Input Overvoltage Protection**

Overvoltage detection of the input voltage  $V_{in}$  is provided by measurement using the HV pin.

Values of  $V_{in,rms}$  are compared to a configurable input overvoltage protection threshold  $V_{in,OV}$ . If the threshold is exceeded for longer than the blanking time  $t_{blank,Vin,OV}$ , the protection will be triggered. XDPL8220 features a configurable startup threshold  $V_{in,start,max}$  to create hysteresis for flicker-free operation before the second stage starts switching. After startup checks when  $t_{rms,reset,PFC}$  expires, the comparison is restored to the threshold value  $V_{in,OV}$ .

*Note: In the csv file the input OVP shall be disabled by default.*

**Functional Description**



**Figure 12**  $V_{in}$  protections

**3.1.12 Other PFC Protections**

**CS Resistor Short Protection**

The input circuit breaker (fuse) shall be chosen appropriately in order to protect in case of current-sense resistor short.

**CS Resistor Open Protection**

The external circuitry for shared CS/ZCD pulls the CSPFC pin high in case of CS resistor missing so that the OCP2 protection is triggered.

**CSPFC Pin Short to GND Protection**

In case of CSPFC pin short to ground the lack of quasi-resonant oscillations shall trigger the CCM Protection.

**CCM Protection**

Continuous conduction mode (CCM) operation may occur during **PFC** startup for a limited time. It is considered as a failure in the system only if CCM operation of the **PFC** converter is observed over a longer period of time. The **PFC** converter may run into CCM operation for a longer period due to a shorted bypass diode, a heavy load step that is out of specification or very low input voltage outside the normal operating range.

When CCM occurs, the magnetizing current in the **PFC** choke does not have the chance to decay to zero before the MOSFET turns on. No quasi-resonant oscillation will be seen at the ZCD signal before the maximum switching period time-out is reached that turns the MOSFET on. This turn-on event without ZCD oscillation is monitored to protect the **PFC** converter from continuous CCM operation. The CCM protection is implemented by firmware.

If any quasi-resonant oscillation is seen at the ZCD signal for longer than the blanking time  $t_{blank,CCM,PFC}$ , the protection is triggered.

**Soft Start Failure**

The soft start may take a long time, potentially never reaching steady state operation due to heavy loads or very low input voltages. If  $t_{start,PFC}$  reaches  $t_{start,max,PFC}$  before the soft start has ended, the protection is triggered.



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## Functional Description

### 3.2 Flyback Controller Features

The **FB** stage provides primary side control that avoids secondary side control feedback loop circuitry usually needed in isolated power converters. This approach supports a low part count to reduce costs.

The **FB** stage features multi-mode operation and it selects the best mode of operation based on operating conditions.

#### 3.2.1 Primary Side Regulation

The **FB** in XDPL8220 provides primary side control of output current and output voltage. No external feedback components are necessary for the current control as the primary side regulation control loop is fully integrated.

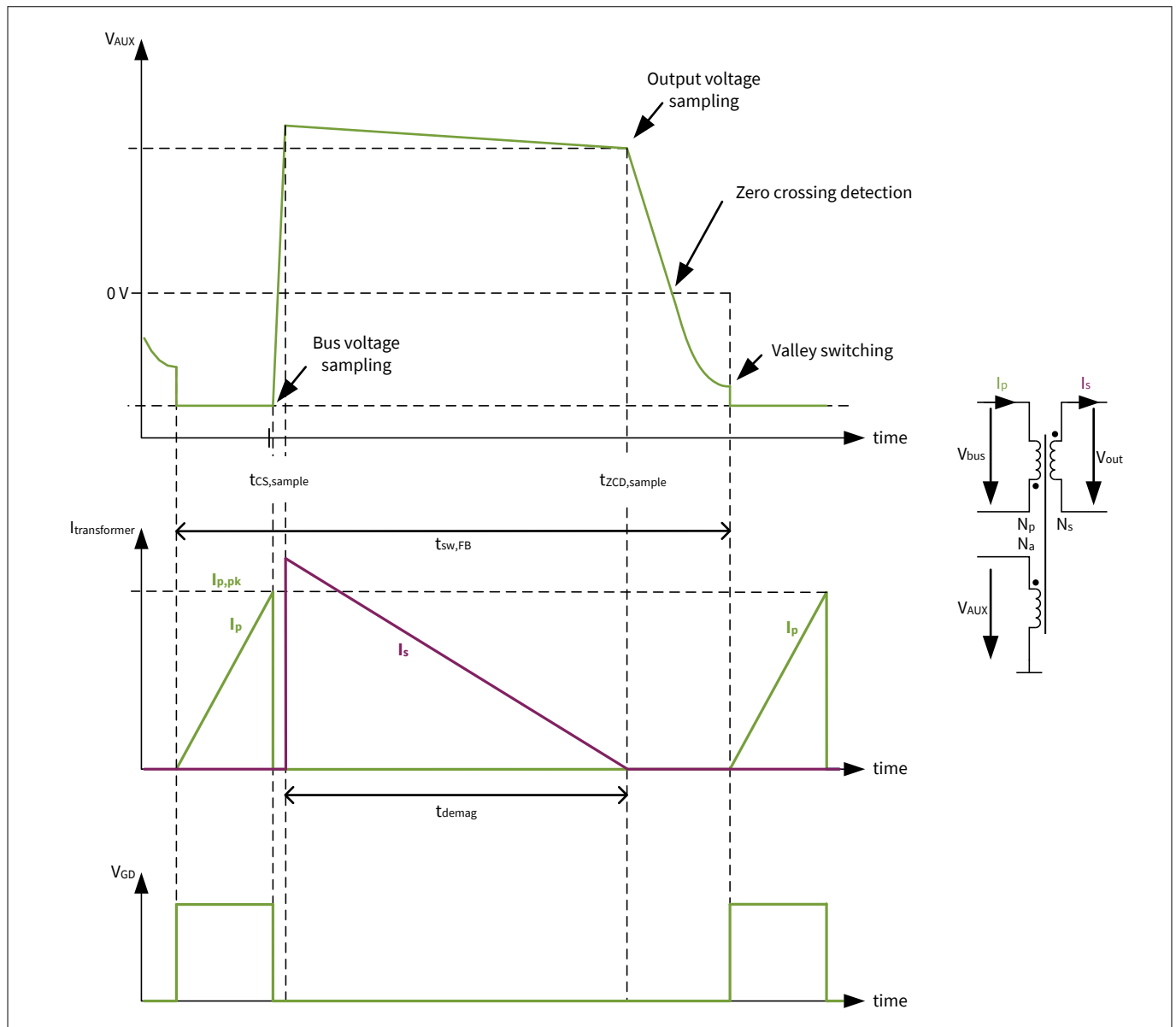
**Figure 13** shows typical current and voltage waveforms of the **FB** application operating in **QRM1**.

In **DCM**, the next switching cycle will not start at the first valley of  $V_{AUX}$ , but is instead delayed. As a consequence, the switching losses in **DCM** will be higher.

The primary peak current  $I_{p,pk}$ , the period of conduction of the output diode  $t_{demag}$  and the switching period  $t_{sw,FB}$  are used to calculate the average output current.

The voltage signal  $V_{AUX}$  of the auxiliary winding of the transformer contains information on the reflected output voltage  $V_{out}$ . The reflected output voltage is measured at the ZCD pin using a resistor divider.

**Functional Description**



**Figure 13 Typical Waveforms of a Flyback Converter**

**3.2.1.1 Primary Side Current Sensing**

The primary side peak current  $I_{p,pk}$  is controlled by the control loop using the  $V_{CS,OCPI}$  level at the CSFB pin. This control scheme ensures suppression of any variation in the bus voltage.

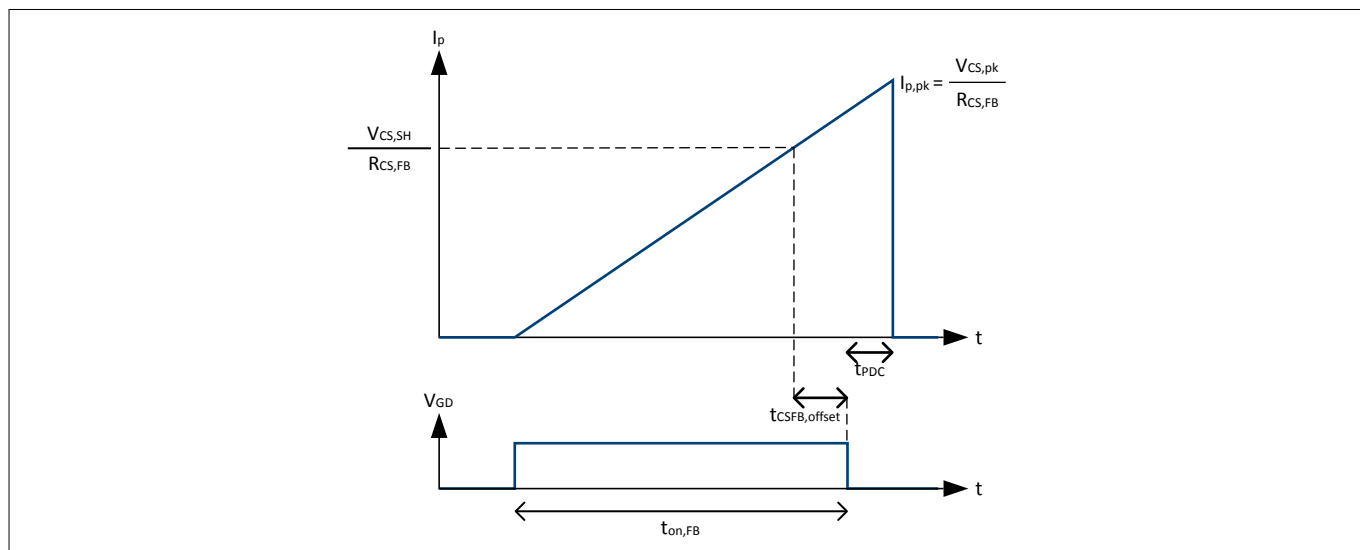
Several delays exist from the time at which the **OCPI** level  $V_{CS,OCPI}$  is exceeded at the CSFB pin until the gate switches off and the transformer current finally reaches its peak value. For a higher accuracy, the primary peak current  $V_{CS,SH}$  is sampled a fixed time before turn-off of the gate. The primary side peak current is used to calculate the secondary side current and for protection. The propagation delay compensation parameter  $t_{PDC}$  allows optimization of the accuracy of the primary side peak current:

$$I_{p,pk} = \frac{V_{CS,SH}}{R_{CS,FB}} \cdot \frac{t_{on,FB} + t_{PDC}}{t_{on,FB} - t_{CSFB,offset}}$$

**Equation 2**

**Functional Description**

*Note: If an RC low pass filter is added in front of the CSFB pin, the related low pass filter delay has to be included in  $t_{PDC}$ .*



**Figure 14 Propagation Delay Compensation for accurate Primary Peak Current Calculation**

**3.2.1.2 Primary Side Output Voltage Sensing**

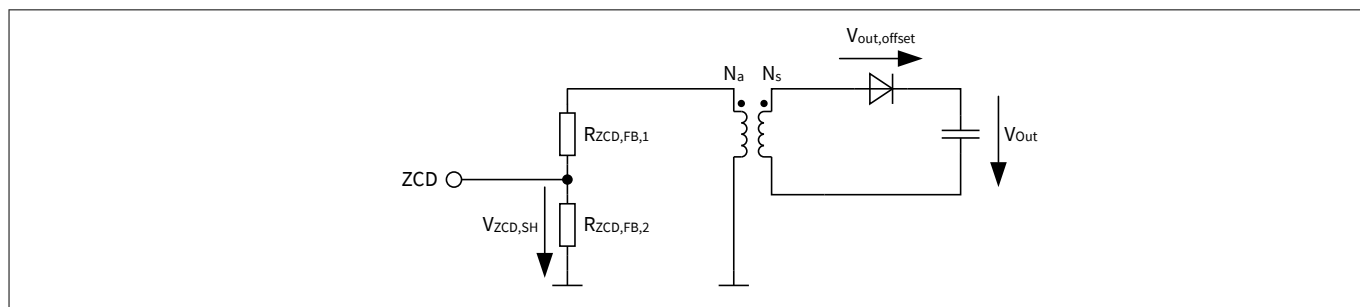
The output voltage is determined by measuring the reflected output voltage on the auxiliary winding. A resistor divider adapts the voltage to the operating range of the ZCD pin.

The output voltage is measured at the ZCD pin using the voltage  $V_{ZCD,SH}$  at the end of the demagnetization time at the time  $t_{ZCD,sample}$ . The voltage measured at the ZCD pin, the dimensioning of the resistor dividers  $R_{ZCD,FB,1}$  and  $R_{ZCD,FB,2}$ , transformer turns  $N_s$  and  $N_a$  as well as an offset  $V_{out,offset}$  (caused by the secondary diode, for example) are used to calculate the output voltage  $V_{out}$  as follows:

$$V_{out} = V_{ZCD,SH} \frac{R_{ZCD,FB,1} + R_{ZCD,FB,2}}{R_{ZCD,FB,2}} \frac{N_s}{N_a} + V_{out,offset}$$

**Equation 3**

$V_{out}$  is used for **Primary Side Regulated (PSR)** control loops in **CV** and **LP** modes as well as for output over- and undervoltage protections.



**Figure 15 Primary Side Output Voltage Sensing using ZCD S&H**

*Note: Any relation between VCC and ZCD in self-supplied applications can be decoupled – e.g. by adding a linear regulator for VCC.*

**Functional Description**

**Attention:** Please note that the time ( $t_{\text{demag}}$ ) has to be longer than 2.0  $\mu\text{s}$  to ensure that the reflected output voltage can be sensed correctly at the ZCD pin.

**3.2.1.3 Flyback Bus Voltage Sensing**

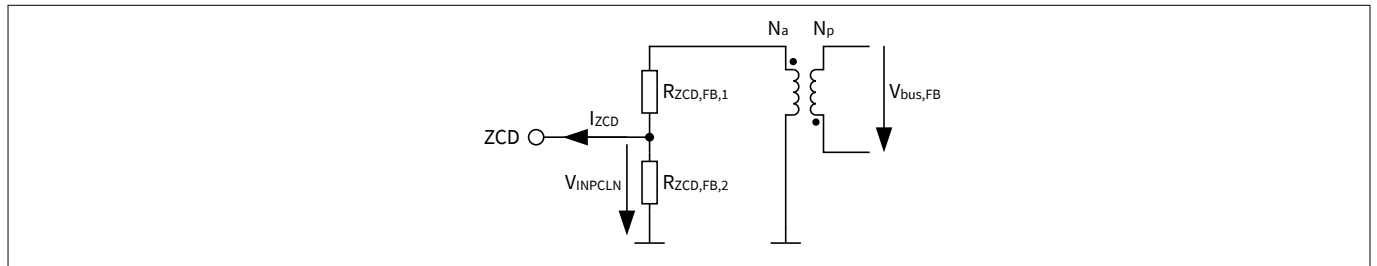
The **FB** can sense the bus voltage using the reflection of bus voltage on the auxiliary winding while the gate is turned on. A resistor divider adapts the negative voltage to the operating range of the ZCD pin. This second measurement path is required to protect against component failures in the VS measurement path (open loop protection for the **PFC** stage).

The reflected bus voltage appears as a negative voltage at  $V_{\text{AUX}}$ . This negative voltage is internally clamped at the ZCD pin to the negative voltage  $V_{\text{INPCLN}}$ . The internal clamping current  $I_{\text{ZCD}}$  is measured at the end of the on-time at the time  $t_{\text{CS,sample}}$ . The measured clamping current of the ZCD pin, the dimensioning of the resistor dividers  $R_{\text{ZCD,FB,1}}$  and  $R_{\text{ZCD,FB,2}}$  as well as the number of transformer turns  $N_a$  and  $N_p$  are used to calculate the bus voltage  $V_{\text{bus,FB}}$  as follows:

$$V_{\text{bus,FB}} = \left( I_{\text{ZCD}} + \frac{V_{\text{INPCLN}}}{R_{\text{ZCD,FB,2}}} \right) R_{\text{ZCD,FB,1}} \left( \frac{N_p}{N_a} \right)$$

**Equation 4**

$V_{\text{bus,FB}}$  is used for plausibility checks with the voltage  $V_{\text{bus}}$  as measured using the VS pin.



**Figure 16 Voltage Sensing using ZCD Clamp Current**

**3.2.1.4 Output Current Calculation**

The output current is calculated based on the primary side peak current and the timing of the switching cycle.

The output current  $I_{\text{out}}$  is calculated using the duration of conduction of the output diode  $t_{\text{demag}}$ , the switching period  $t_{\text{sw,FB}}$  as well as the number of transformer turns  $N_p$ ,  $N_s$  and the transformer coupling  $K_{\text{coupling}}$ . The following equation is valid both in **QRM1** and **DCM**:

$$I_{\text{out}} = \frac{1}{2} I_{p,\text{pk}} \cdot \frac{N_p}{N_s} \cdot K_{\text{coupling}} \cdot \frac{t_{\text{demag}}}{t_{\text{sw,FB}}}$$

**Equation 5**

The coupling of the transformer can be approximated using the transformer primary inductance  $L_p$  and the transformer primary leakage inductance  $L_{p,\text{lk}}$  as follows:

$$K_{\text{coupling}} \approx \frac{L_p}{L_p + L_{p,\text{lk}}}$$

**Equation 6**

The calculated current  $I_{\text{out}}$  is used for the control loop in the modes **CC** and **LP**. The calculated current is also used for output overcurrent protection.

**Functional Description**

**3.2.1.5 Output Control Scheme**

The XDPL8220 includes three different control schemes for a **CC**, **CV** or **LP** output.

Different use cases require the controller to operate according to different operation schemes:

- In the case of typical LED strings, the forward voltage of the LED string determines the output voltage of the driver. XDPL8220 operates in **CC** and drives a constant output current  $I_{out,full}$  to the load. The forward voltage of the connected LED string has to be below a configurable maximum value  $V_{out,set}$ .
- In the case of LED loads including a power stage (e.g. Infineon BCR linear regulators or Infineon DC/DC buck ILD2111), XDPL8220 operates in **CV**, ensuring a constant voltage  $V_{out,set}$  to the load. The total output current drawn by the load has to be below a configurable maximum value  $I_{out,full}$ .
- In the case of a high output current setpoint  $I_{out,full}$  and an overly long LED string which exceeds the configurable power limit  $P_{out,set}$ , XDPL8220 operates in **LP** to ensure that the power limit of the driver is not exceeded. The controller reduces the output current automatically, ensuring light output without any interruption even for overly long LED strings. The forward voltage of the connected LED string has to be below a configurable maximum value  $V_{out,set}$ .

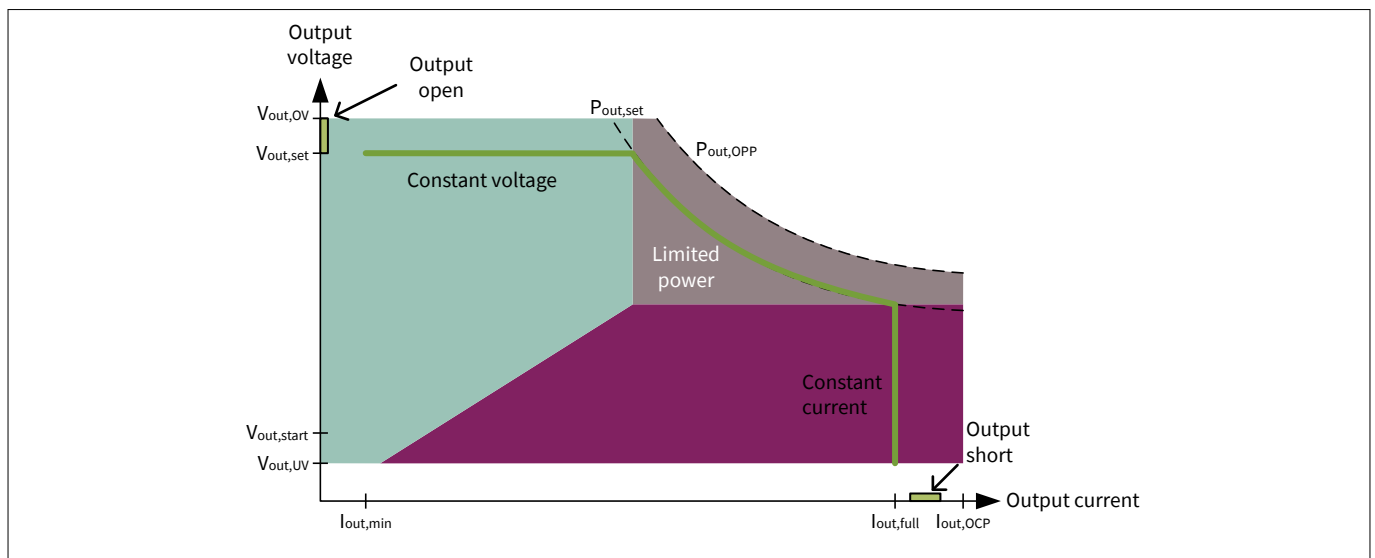
For every update of the control loop, the control scheme is selected on the basis of the current operation conditions (output voltage  $V_{out}$  and output current  $I_{out}$ ) and their distance to the three limiting setpoints ( $V_{out,set}$ ,  $P_{out,set}$  and  $I_{out,full}$ ):

- For **CC** schemes, the internal reference current  $I_{out,full}$  is weighted according to thermal management and a dimming curve to yield  $I_{out,set}$ . The calculated output current  $I_{out}$  is compared with the weighted reference current  $I_{out,set}$  to generate an error signal for the output current.
- For **CV** schemes, the sensed output voltage  $V_{out}$  at the ZCD pin is compared to a reference voltage  $V_{out,set}$  to generate an error signal for the output voltage.
- For **LP** schemes, the output current is limited to a maximum of  $I_{out,set} = P_{out,set} / V_{out}$ .

Out of these three schemes, for each step the most critical error is selected (see **Figure 17**):

1. If any setpoint is exceeded, the largest error for power decrease is selected to bring the controller back to the desired operating point as quickly as possible.
2. If the current operating conditions are below all three setpoints, the smallest error for power increase is selected to avoid overshooting any setpoint.

The selected error signal is fed into a compensator to control the gate driver switching parameters (i.e. duty cycle and frequency) for the power MOSFET of the **FB**.

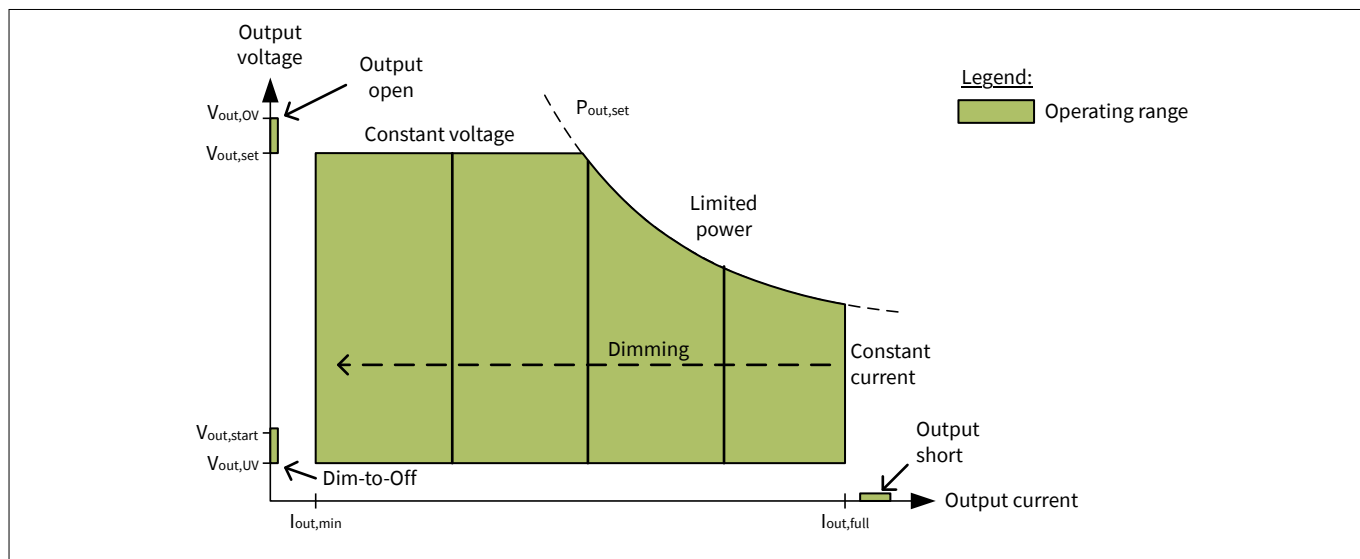


**Figure 17 Control Scheme for CC/CV/LP Modes (Non-Dimmed)**

In dimming cases, the output current setpoint  $I_{out,set}$  is located between  $I_{out,min}$  and  $I_{out,full}$  and varies according to the sensed **PWM** duty cycle  $D_{DIM}$ . Dimming can be visualized by moving the vertical line for the output current setpoint in **Figure 18** from right to left.

**Functional Description**

*Note: An operation in limited power mode can cause dimmer dead-travel until the controller enters constant current mode.*



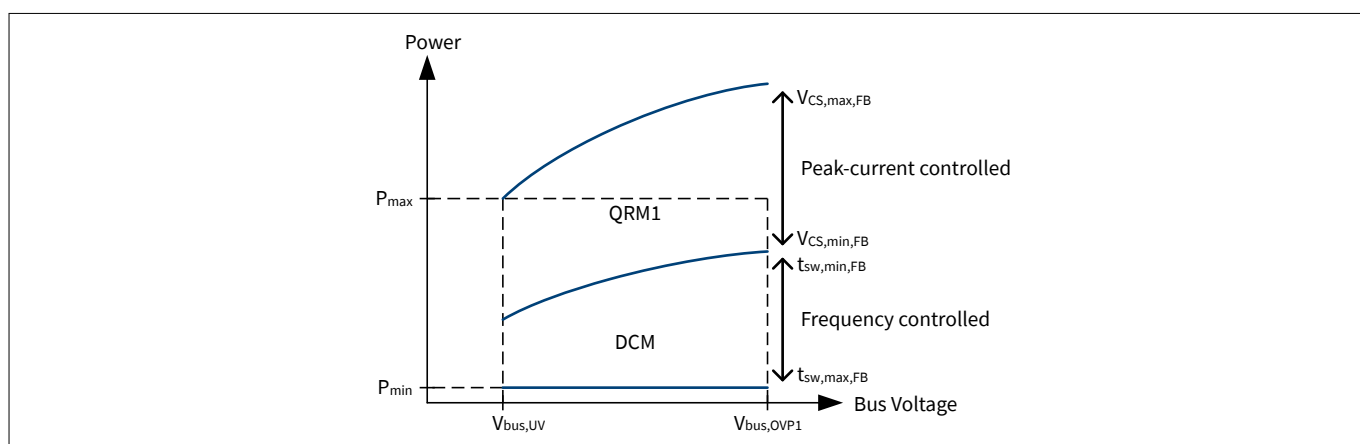
**Figure 18 Control Scheme for CC/CV/LP Modes (including Dimming)**

One or more of the output control schemes can be deactivated by configuration of the setpoints. Some examples are given below:

- The **LP** scheme is not active for  $P_{out,set} > V_{out,set} \cdot I_{out,full}$ . For such a configuration, the controller will only select between a **CC** and **CV** scheme.
- The **CV** scheme is not active for  $V_{out,set} = V_{out,OV}$  as the output overvoltage protection will be triggered.
- The **CC** scheme is not active for  $I_{out,full} = I_{out,OC}$  as the output overcurrent protection will be triggered.

**3.2.1.6 Multimode Scheme**

The control loop of XDPL8220 uses two different switching modes. **QRM1** is optimized for high efficiency at high loads while **DCM** is used in light load conditions.



**Figure 19 Flyback Multimode Operation Scheme**

- **QRM1**: This mode maximizes the efficiency by switching on the 1st valley of the  $V_{AUX}$  signal. This ensures zero current switching with a minimum of switching losses. The power is controlled by regulating the primary peak current using  $V_{CS, OCP1}$ .
- **DCM**: This mode is used if  $V_{CS, OCP1}$  has reached its minimum value  $V_{CS, min, FB}$ . To allow lower output power, the controller extends the switching period later than the 1st valley .

**Functional Description**

The minimum power is limited by the transformer primary inductance  $L_p$ , maximum switching period  $t_{sw,max,FB}$  and minimum primary peak current  $I_{p,pk,min}$ :

$$P_{min} = \frac{1}{2} \cdot L_p \cdot I_{p,pk,min}^2 \cdot \frac{1}{t_{sw,max,FB}}$$

**Equation 7**

The minimum primary peak current  $I_{p,pk,min}$  is restricted by:

$$I_{p,pk,min} = t_{demag,min} \cdot \frac{N_p}{N_s} \cdot \frac{V_{out,OV}}{L_p}$$

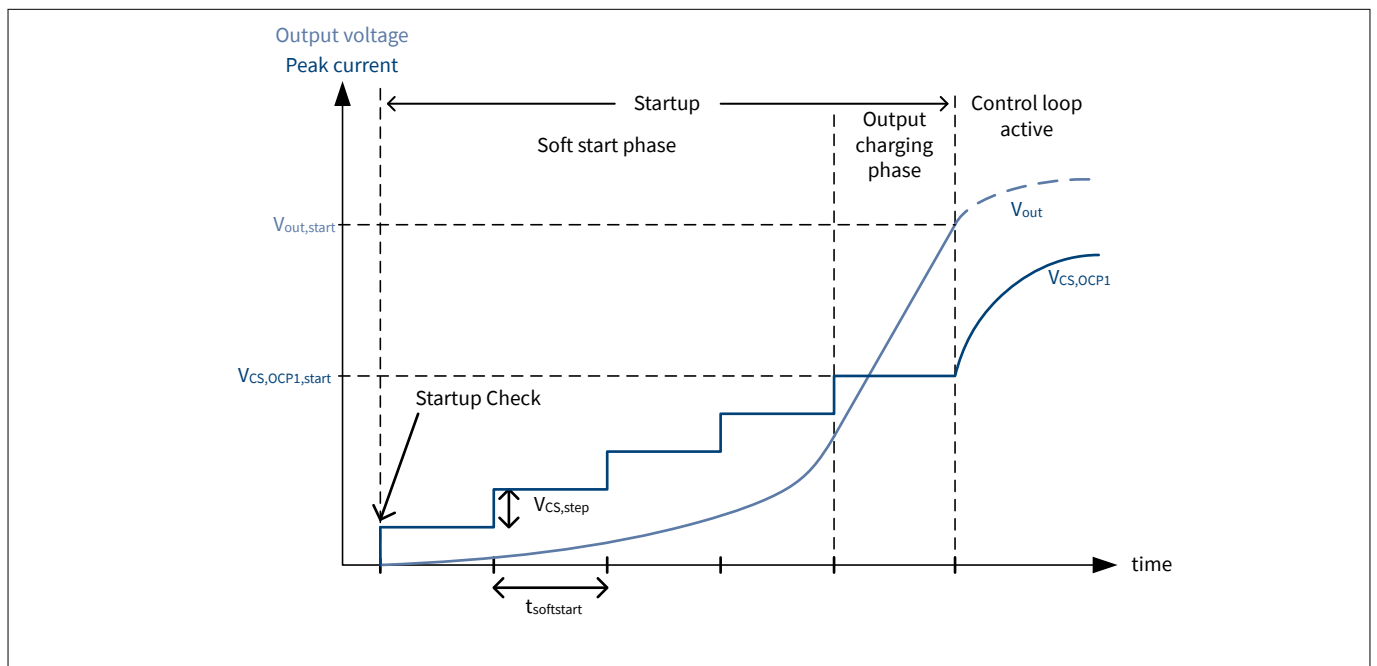
**Equation 8**

*Note: If the load drops below the minimum load of  $P_{min}$ , the output voltage will rise up to the output overvoltage threshold  $V_{out,OV}$  and trigger the protection. An auto-restart can be used to keep the output voltage close to  $V_{out,OV}$  until the load increases again.*

**3.2.2 Flyback Startup**

After startup, the **FB** of the XDPL8220 initiates a soft start to minimize the switching stress for the power MOSFET and secondary diode.

The cycle-by-cycle current limit is increased in steps of  $V_{CS,step}$  with a configurable duration  $t_{softstart}$  for each step. After the final  $V_{CS,OC1,start}$  limit level has been reached, the output will be charged until the minimum output voltage  $V_{out,start}$ , which ensures self-supply has been reached. At this condition, **Continuous Conduction Mode (CCM)** protection as well as output undervoltage protection are activated and the control loop takes over. The starting point for the control loop is to operate in DCM at lowest switching frequency and shortest on-time. These switching parameters avoid any overshoot of output current for short LED string in dimmed conditions.



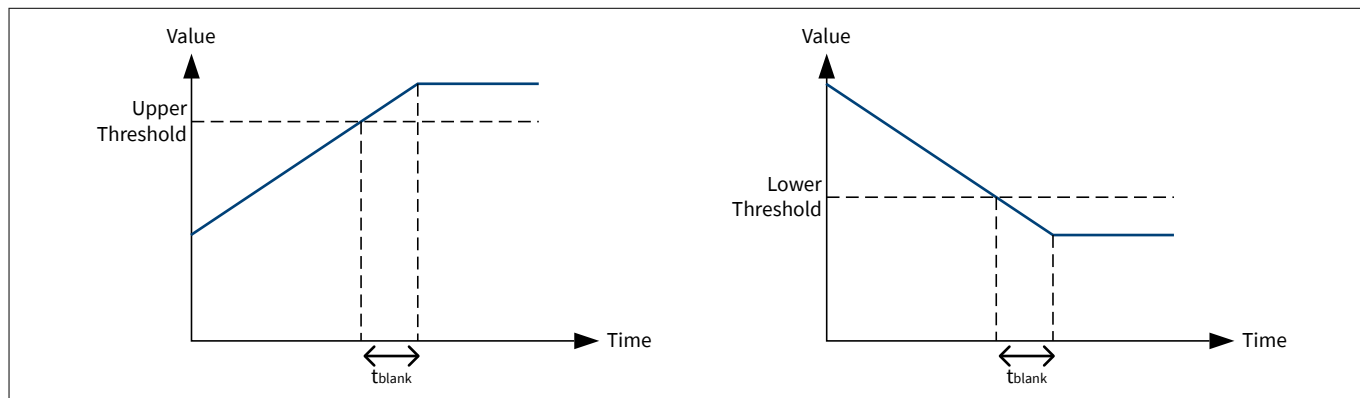
**Figure 20 Flyback Startup Sequence**

**Functional Description**

**3.2.3 Protection Features**

Protections ensure the operation of the controller under restricted conditions. Protections are triggered if fault conditions are present longer than the blanking times configured for each protection<sup>3)</sup>. The controller will react to a triggered protection as configured.

**Attention:** *The controller may continue operation after exceeding protection thresholds because of blanking times. All protection thresholds have to be set with respect to tolerances, blanking times and worst case transients.*



**Figure 21 Blanking Times cause Excess of Threshold**

**3.2.3.1 Primary Overcurrent Protection**

The primary side overcurrent protection implemented in hardware covers fault conditions like a short in the transformer primary winding or an open CS pin.

The primary side current is compared to a configurable overcurrent protection threshold  $V_{CS, OCP2}$ . If the threshold is exceeded for longer than the blanking time  $t_{OCP2, FB}$ , the protection will be triggered.

**3.2.3.2 Output Undervoltage Protection**

In the case of a short in the output, the output voltage may drop to a very low level. Detection of undervoltage in the output voltage  $V_{out}$  is enabled by measurement of the reflected voltage at the ZCD pin.

During operation, the output voltage is compared to a configurable undervoltage protection threshold  $V_{out, UV}$ . If the threshold is exceeded for longer than the blanking time  $t_{blank, out, UV}$ , the protection will be triggered. This protection threshold  $V_{out, UV}$  is disabled during startup.

During startup, the protection operates differently: In case the **FB** cannot charge the output voltage to  $V_{out, start}$  during a timeout of  $t_{start, max, FB}$ , the protection will be triggered. This timeout starts when the **FB** is started.

*Note:* *The startup threshold  $V_{out, start}$  has to be configured over and above the undervoltage threshold  $V_{out, UV}$  to allow undershoots at startup which may occur, especially for resistive loads.*

**3.2.3.3 Output Overvoltage Protection**

In case of an open output, the output voltage may rise to a high level. Overvoltage detection of the output voltage  $V_{out}$  is provided by measurement at the ZCD pin.

The output voltage is compared to a configurable overvoltage protection threshold  $V_{out, OV}$ . If the threshold is exceeded for longer than the blanking time  $t_{blank, out, OV}$ , the protection will be triggered.

<sup>3</sup> except VCC undervoltage protection



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## Functional Description

*Note:* The blanking time  $t_{\text{blank},V_{\text{out,OV}}}$  should be set to the minimum value to minimize overshoots of the output voltage above the protection threshold.

*Note:* This protection is usually triggered if the output is open or the output load drops below the minimum load  $P_{\text{min}}$ .

### 3.2.3.4 Output Overcurrent Protection

Overcurrent detection in the output current  $I_{\text{out}}$  is provided on the basis of the calculated output current. The calculated output current is compared to a configurable overcurrent protection threshold  $I_{\text{out,OC}}$ . If the threshold is exceeded for longer than the blanking time  $t_{\text{blank,out,OC}}$ , the protection will be triggered.

### 3.2.3.5 Output Overpower Protection

Overpower detection in the output power  $P_{\text{out}}$  is provided on the basis of the calculated output power. The calculated output power is compared to a configurable overpower protection threshold  $P_{\text{out,OP}}$ . If the threshold is exceeded for longer than the blanking time  $t_{\text{blank,out,OP}}$ , the protection will be triggered.

### 3.2.3.6 Other Flyback Protections

XDPL8220 includes additional protections to ensure the integrity and correct flow of the firmware.

- A hardware weak pull-up protects against an open CSFB pin.
- A firmware watchdog protects against the CSFB pin becoming shorted to GND.
- A firmware state monitor supervises correct operation of the flyback in **QRM1** or **DCM**. A protection is triggered if the flyback enters **CCM**.
- A firmware check ensures that the **PFC** has already boosted the bus voltage sufficiently before the **FB** starts.
- A firmware plausibility check ensures that the bus voltage measurement using the VS pin is correct.

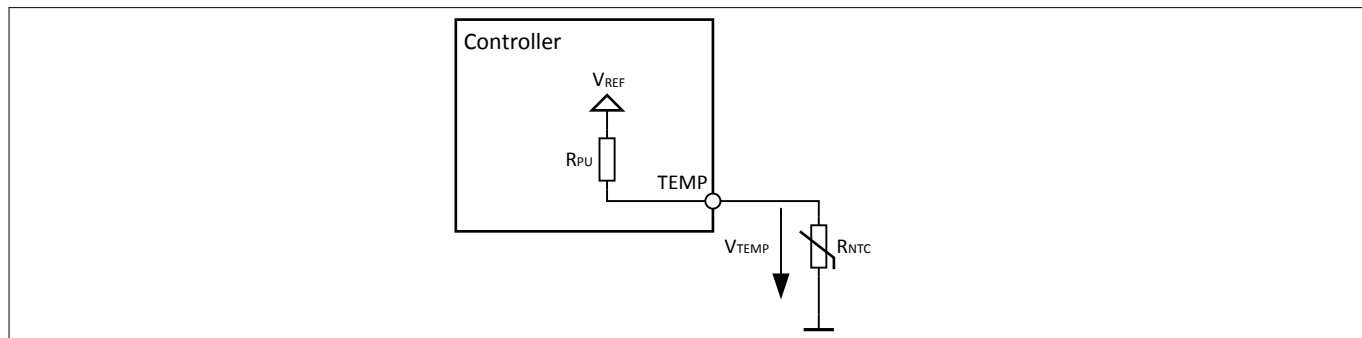
**Functional Description**

**3.3 General Controller Features**

XDPL8220 provides general features for firmware task scheduling, VCC control and temperature control which are independent of the target application.

**3.3.1 External Temperature Sensing**

The external temperature is measured by measuring the voltage of an **NTC** with respect to the internal  $V_{REF}$  voltage.



**Figure 22 External Temperature Sensing using NTC**

The controller calculates the resistance of the NTC based on the measured voltage  $V_{Temp}$ , the internal reference voltage  $V_{REF}$  and the internal pull-up resistance  $R_{PU}$ :

$$R_{NTC} = \frac{V_{Temp} \cdot R_{PU}}{V_{REF} - V_{Temp}}$$

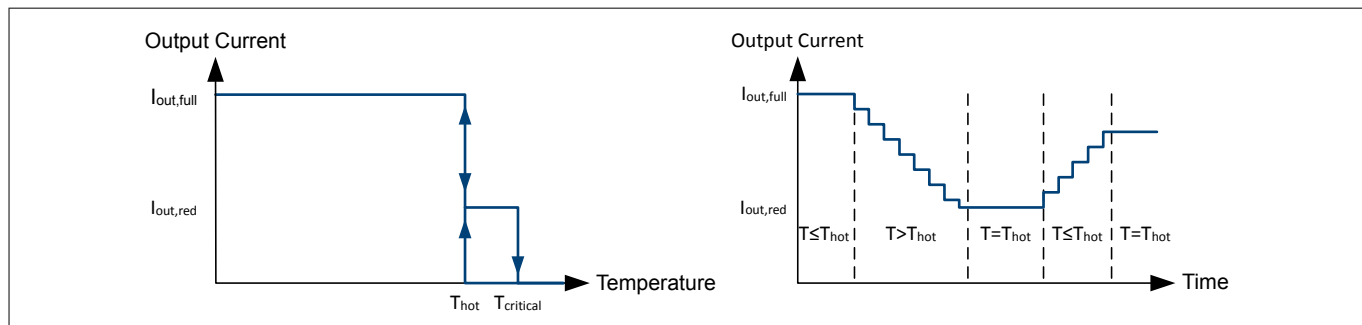
**Equation 9**

**3.3.2 Adaptive Temperature Protection**

XDPL8220 offers adaptive temperature protection using internal and/or external temperature sensors. This feature reduces the output current according to temperature to protect the load and driver against overtemperature.

Whenever the temperature  $T_{hot}$  is exceeded, the current is gradually reduced from the maximum current  $I_{out,set}$ , as shown in **Figure 23**. If the temperature drops below  $T_{hot}$ , the output current is increased again. This allows the controller to ensure operation at or below a temperature of  $T_{hot}$ .

If a reduction down to a minimum current  $I_{out,red}$  is not able to compensate for any continued increase in temperature, XDPL8220 will eventually trigger overtemperature protection if  $T_{critical}$  is exceeded. If the controller is configured to react with auto-restart to the overtemperature protection, it will only restart after the temperature dropped below  $T_{hot}$ .



**Figure 23 Adaptive Temperature Protection**

**Functional Description**

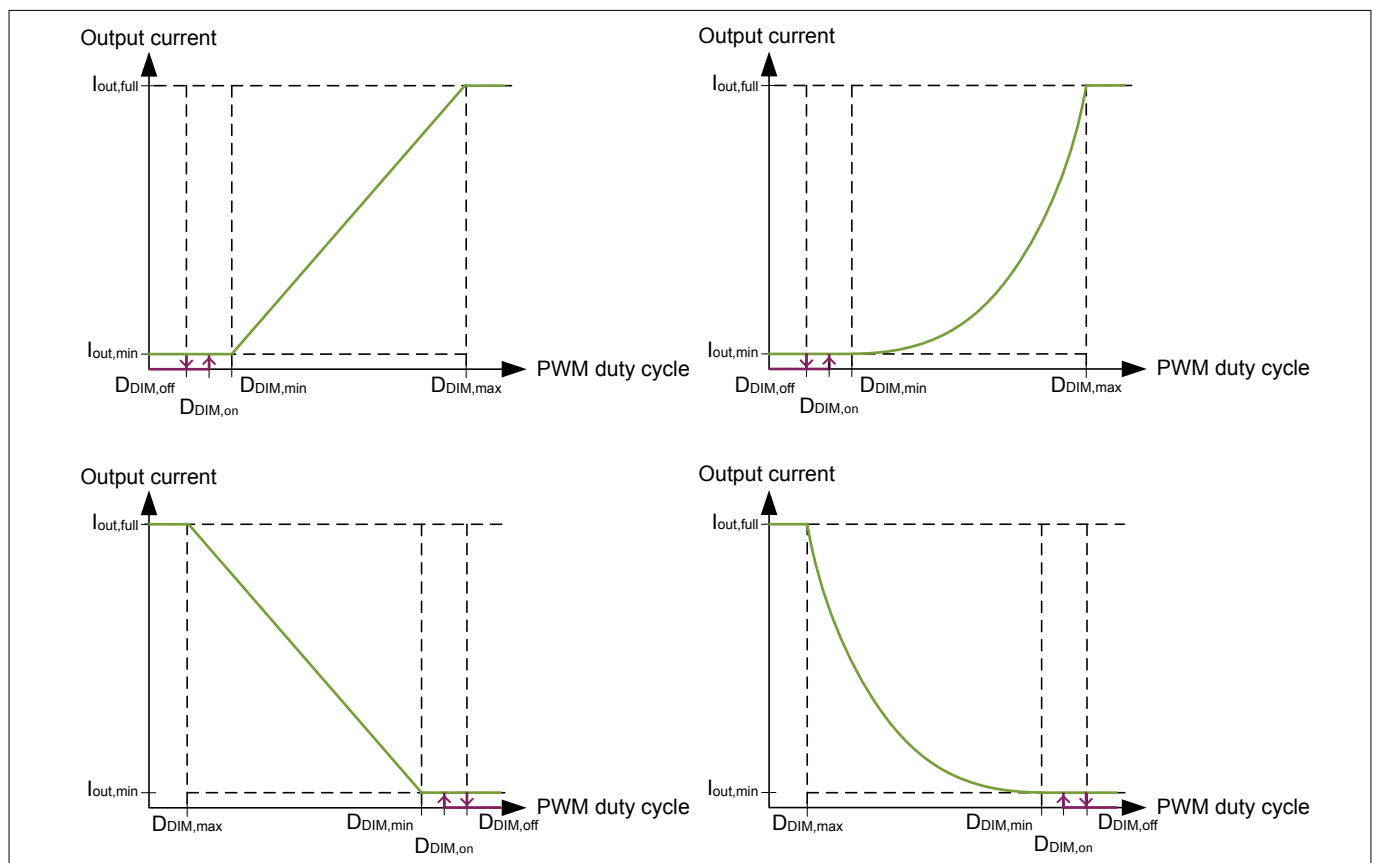
*Note: Please note that the internal temperature sensor can only protect external components which have sufficient thermal coupling to XDPL8220. The external temperature sensor can be used to protect the temperature of external components (e.g. power MOSFETs or linear regulators).*

**3.3.3 PWM Dimming Interface**

The duty cycle sensed at the PWM pin is used to determine the output current level. The XDPL8220 can be configured to use either a linear or a quadratic dimming curve. Either normal or inverted dimming curves can be selected.

Figure 24 shows the relationship of the PWM duty cycle to the output current target value. Configurable levels  $D_{DIM,min}$  and  $D_{DIM,max}$  ensure that the minimum current  $I_{out,min}$  and maximum current  $I_{out,set}$  can always be achieved, thereby making the application robust against component tolerances.

An optional hysteresis can be enabled for the sensing of the PWM signal. This hysteresis can suppress jitter in the PWM signal. Any change of the PWM duty cycle within the hysteresis will not affect the output current.



**Figure 24 Selectable Dimming Curves**

Using the optional Dim-to-Off feature, the light output can be stopped without removal of input voltage. In Dim-to-Off, the controller will enter auto-restart operation to minimize power consumption. The auto-restart recharges the output voltage to a minimum output voltage of  $V_{out,start}$  to measure the PWM duty cycle. With this feature, the output voltage can be maintained in a specific range by configuration of the startup voltage  $V_{out,start}$  and auto-restart time  $t_{AR}$ , and by dimensioning of an active or passive output bleeder. If  $V_{out,start}$  is configured to be low enough below the minimum forward voltage of the LED string, the LEDs will show no light in this state.

*Note: Either an active or passive output bleeder is required to allow the controller to maintain the output voltage if the Dim-to-Off feature is enabled.*

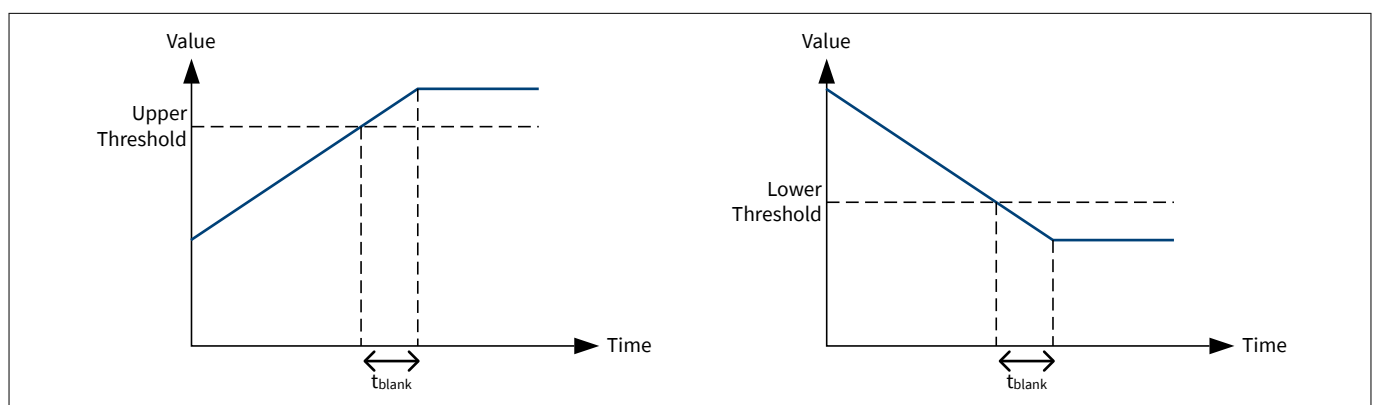
**Functional Description**

Dim-to-Off is entered if the **PWM** duty cycle exceeds the configurable threshold  $D_{DIM,off}$  (see purple line in **Figure 24**). As soon as the duty cycle exceeds  $D_{DIM,on}$ , the controller will start to continuously regulate output voltage or output current again.

**3.3.4 Protection Features**

Protections ensure the operation of the controller under restricted conditions. Protections are triggered if fault conditions are present longer than the blanking times configured for each protection<sup>4</sup>. The controller will react to a triggered protection as configured.

**Attention:** *The controller may continue operation after exceeding protection thresholds because of blanking times. All protection thresholds have to be set with respect to tolerances, blanking times and worst case transients.*



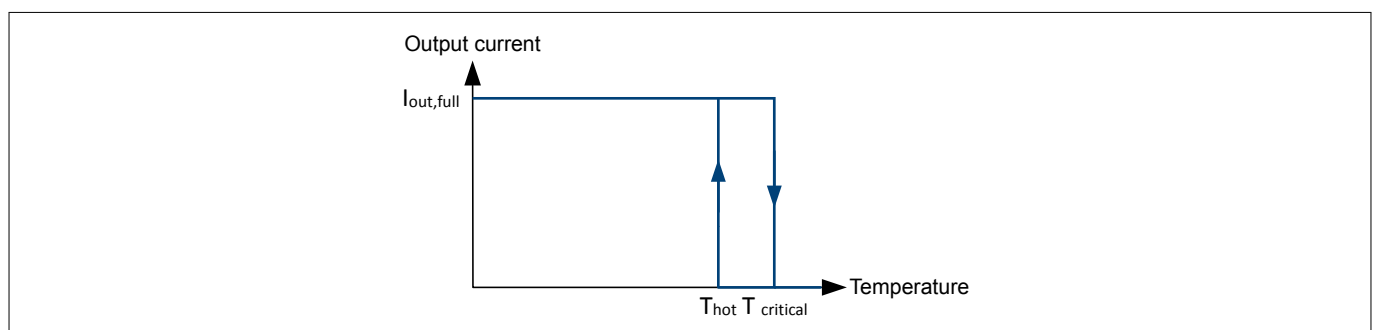
**Figure 25 Blanking Times cause Excess of Threshold**

**3.3.4.1 Overtemperature Protection**

Overtemperature protection initiates a shutdown once the critical temperature level  $T_{critical}$  is exceeded.

**Figure 26** shows the temperature hysteresis formed by the critical temperature  $T_{critical}$  and maximum turn-on threshold  $T_{hot}$  if auto-restart is enabled for temperature protection.

If latch mode is selected instead, the IC will turn off and only restart after recycling of input power with a temperature below  $T_{critical}$ .



**Figure 26 Temperature Protection**

<sup>4</sup> except VCC undervoltage protection

## Functional Description

### 3.3.4.2 VCC Undervoltage Protection

A **Undervoltage Lockout (UVLO)** is implemented in hardware. It ensures defined enabling and disabling of the **Integrated Circuit (IC)** operation depending on the supply voltage  $V_{VCC}$  at the VCC pin in accordance with defined thresholds.

The **UVLO** contains a hysteresis with the voltage thresholds  $V_{VCC,on}$  for enabling the **IC** and  $V_{VCC,off}$  for disabling the IC. Once the mains input voltage is applied, current flows through an external resistor into the HV pin via the integrated depletion cell and diode to the VCC pin. The **IC** is enabled once  $V_{VCC}$  exceeds the threshold  $V_{VCC,on}$  and enters normal operation if no fault condition is detected. In this phase,  $V_{VCC}$  will drop until either external supply or the self-supply via the auxiliary winding takes over the supply at the VCC pin.

In the case of output short or strong capacitive loading, the auxiliary winding cannot provide power to  $V_{VCC}$ . A timeout of  $t_{start,max}$  is available to respond to this failure condition.

*Note: The self-supply via the auxiliary winding must be in place before the output short timeout occurs or before  $V_{VCC}$  falls below the  $V_{VCC,off}$  threshold. Otherwise, the system will perform a fast restart.*

*Note: It is possible to supply VCC externally from an auxiliary power supply. In this case, the VCC also needs initially to ramp to  $V_{VCC,on}$  to enable the IC.*

### 3.3.4.3 VCC Overvoltage Protection

Overvoltage protection ensures that the voltage at the VCC pin is not exceeded.

The VCC voltage is compared to a configurable overvoltage protection threshold  $V_{VCC,OV}$ . If the threshold is exceeded for longer than the blanking time  $t_{blank,VCC,OV}$ , the protection will be triggered.

*Note: The reaction to this protection is fixed to stop mode to ensure a discharge of VCC.*

### 3.3.4.4 Other General Controller Protections

XDPL8220 includes several protections to ensure the integrity and correct flow of the firmware.

- A hardware watchdog checks correct execution of firmware. A protection is triggered in the event that the firmware does not service the watchdog within a defined period.
- A hardware **Random Access Memory (RAM)** parity check triggers a protection if a bit in the memory changes unintentionally.
- A hardware clock check watchdog checks that no clock oscillator is failing.
- A firmware **Cyclic Redundancy Check (CRC)** at each startup verifies the integrity of firmware code and its parameters.
- A firmware task execution watchdog triggers a protection if the firmware tasks are not executed as expected.

### 3.3.5 Protection Reactions

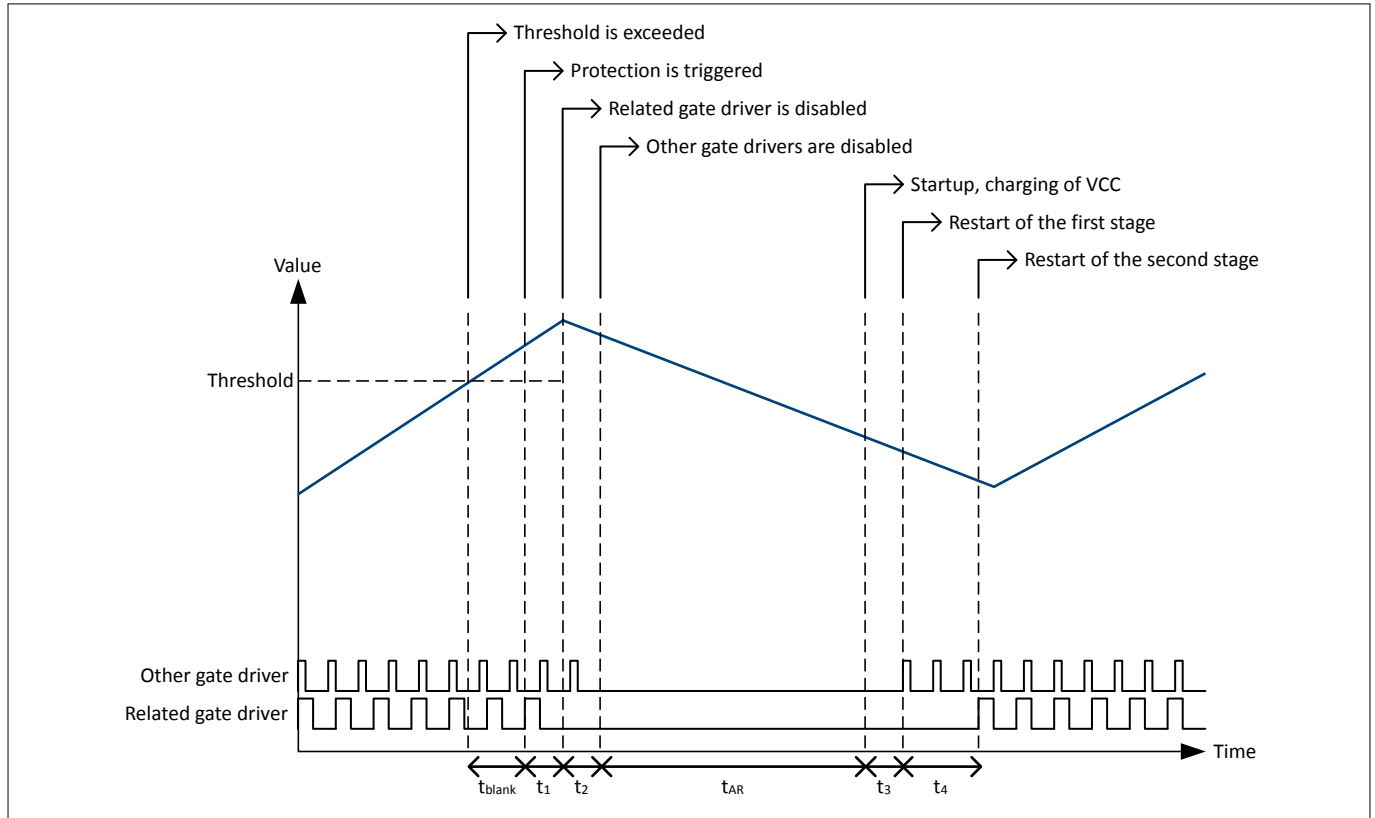
The reaction to each protection can be separately selected. Available reactions may include auto restart, fast auto restart, latch or stop mode.

**Figure 27** depicts the timing of an auto-restart reaction:

1. If a protection threshold is exceeded for longer than the related blanking time  $t_{blank}$ , the protection is triggered.
2. Within a maximum  $t_1 = 4 * 32 \mu s$ , the gate driver of the power stage related to the protection is disabled.
3. Within a maximum  $t_2 = 4 * 32 \mu s$ , the gate drivers of other stages are disabled.
4. The reaction depends on the configuration of the protection:
  - In case of latch mode, the application will enter latch mode at this time. No further steps are done, the reaction ends here.

**Functional Description**

- In case of stop mode, the application will stop and enter UART parametrization mode which allows to read out the error code. No further steps are done, the reaction ends here.
  - In case of a (fast) auto-restart reaction, the controller will enter a power saving mode for the auto-restart time  $t_{AR}$  or  $t_{AR,fast}$  respectively.
5. The auto restart may include a new VCC charging cycle. The time  $t_3$  typically depends on the input voltage.
  6. The first power stage will enable its gate driver according to its startup sequence (soft start) again.
  7. The second power stage will enable its gate driver according to its startup sequence (soft start) again. The startup of a subsequent power stage may be delayed by a time  $t_4$  depending on any startup condition for the subsequent stage.



**Figure 27 Protection Reaction for auto-restart**

**3.3.5.1 Auto restart**

When auto restart mode is activated, XDPL8220 stops switching at the GD pins. After a configurable auto restart time  $t_{AR}$ , XDPL8220 initiates a new startup with soft start.

During the time in which the gate is not switching, the internal HV startup cell is automatically enabled and disabled to keep the VCC voltage between the  $V_{UVLO}$  and  $V_{OVLO}$  thresholds for the supply of XDPL8220.

**3.3.5.2 Fast Auto Restart**

When fast auto restart mode is activated, XDPL8220 stops switching at the GD pins. After a configurable fast auto restart time  $t_{AR,fast}$ , XDPL8220 initiates a new startup with soft start.

During the time in which the gate is not switching, the internal HV startup cell is automatically enabled and disabled to keep the VCC voltage between the  $V_{UVLO}$  and  $V_{OVLO}$  thresholds for the supply of XDPL8220.

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**Functional Description**

### **3.3.5.3 Latch Mode**

When latch mode is activated, XDPL8220 stops switching at the GD pins. The device stays in this state until input voltage is completely removed and the VCC voltage drops below the  $V_{UVLO}$  threshold. Only then can XDPL8220 be restarted by applying input voltage.

To maintain this state, the internal HV startup cell is automatically enabled and disabled to keep the VCC voltage between the  $V_{UVLO}$  and  $V_{OVLO}$  thresholds for the supply of XDPL8220. The current consumption is reduced to a minimum.

### **3.3.5.4 Stop Mode**

When stop mode is activated, XDPL8220 stops switching at the GD pins. XDPL8220 enters **UART** communication mode to allow debugging of the system state.

*Note: The VCC for XDPL8220 needs to be supplied by an external source. Without an external supply, VCC will drain to  $V_{UVLO}$  and XDPL8220 performs a restart.*

**Design Support**

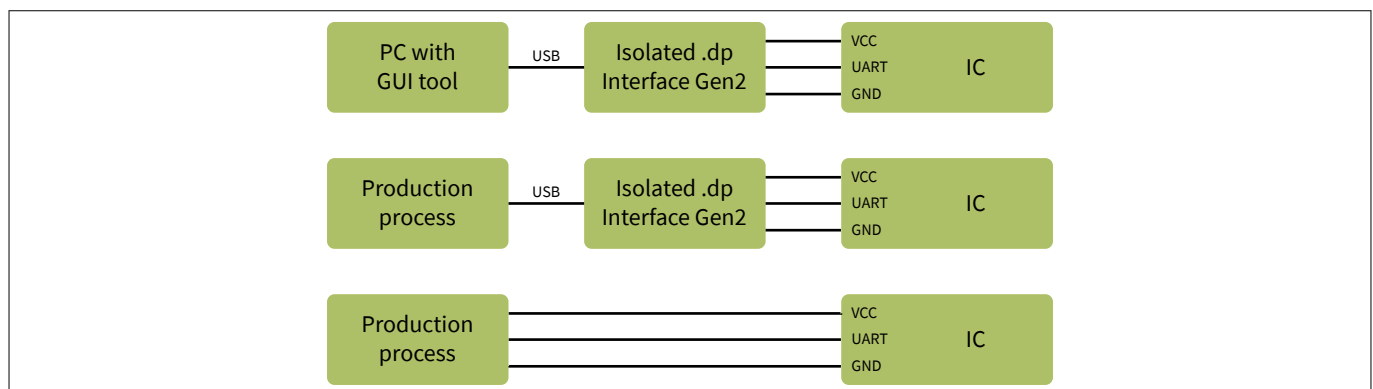
## 4 Design Support

XDPL8220 is a configurable digital platform product. It can be configured to meet a wide range of application requirements.

### 4.1 Design Procedure

Infineon provides support of the design procedure for lighting applications using Infineon's digital platform *ICs*. A lighting application is designed in a few simple steps using Infineon's digital platform *ICs* as follows:

1. The Infineon XDPL8220 reference board and the *XDPL8220 Reference Board Test Report* demonstrate the features and performance of the XDPL8220 in a typical application.
2. Parameters of the XDPL8220 reference board can easily be fitted to any application's requirements. The isolated *.dp Interface Gen2* is connected to XDPL8220 via **Universal Serial Bus (USB)**. The **GUI** tool *.dp Vision* is included with the *.dp Interface Gen2*. *.dp Vision* allows interactive changing of parameters. The usage of *.dp Vision* is explained in the *.dp Vision User Manual*.
3. To further adapt the XDPL8220 to application requirements, customers can design their own specific boards. The steps used to design a board are explained in the *XDPL8220 Design Guide*. *.dp Vision* can be used together with the *.dp Interface Gen2* to connect to customer-specific designs based on XDPL8220. This setup can be used for rapid prototyping. The tooling allows fine-tuning of parameters and development of multiple parameter sets – e.g. to reuse the same for different product variants of an application.
4. For mass production, the *XDPL8220 Programming Manual* documents the necessary interfacing and procedures to integrate the parameter configuration of XDPL8220 into the production line. **Figure 28** shows two options to easily apply the configuration of the *IC* during production tests:
  - One option is to use the isolated *.dp Interface Gen2*, which can be accessed with **USB** commands.
  - Another option is to directly use the **UART** interface of the XDPL8220. The correct VCC voltage and **UART** communication have to be controlled by the production process in this case.



**Figure 28 Setup for Parametrization using *.dp Interface Gen2* for Interactive Development (top) and Production (middle and bottom)**

### 4.2 List of Configurable Parameters

This list provides information about configurable parameters, including their permitted range and granularity. Typical example values are also provided.

**Table 2 Parameters for Hardware Configuration**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$N_a$	<b>FB</b> auxiliary winding turns	34	1	300	1
$N_p$	<b>FB</b> primary winding turns	60	1	300	1



**Design Support**

**Table 2 Parameters for Hardware Configuration (continued)**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$N_s$	<b>FB</b> secondary winding turns	44	1	300	1
$R_{CS,FB}$	<b>FB</b> current sense resistance	410/2048 $\Omega$	200/2048 $\Omega$	3 $\Omega$	1/2048 $\Omega$
$R_{ZCD,FB,1}$	<b>FB</b> ZCD upper resistor	120 k $\Omega$	50 $\Omega$	200 k $\Omega$	50 $\Omega$
$R_{ZCD,FB,2}$	<b>FB</b> ZCD shunt resistor	7.5 k $\Omega$	50 $\Omega$	100 k $\Omega$	50 $\Omega$
$R_{VS,1}$	VS upper resistor for bus voltage measurement	9.96 M $\Omega$	500 k $\Omega$	15 M $\Omega$	500 $\Omega$
$R_{VS,2}$	VS shunt resistor for bus voltage measurement	52.3 k $\Omega$	22 k $\Omega$	100 k $\Omega$	50 $\Omega$
$R_{HV}$	HV resistor	100 k $\Omega$	47 k $\Omega$	130 k $\Omega$	50 $\Omega$
$V_{out,offset}$	Output voltage offset (e.g. voltage drop from secondary diode)	-0.625 V	-4.000 V	4.000 V	0.125 V
$V_{GBFB}$	FB gate driver voltage high level	10.5 V	4.5 V	15 V <sup>1)</sup>	1.5 V
$I_{GBFB}$	FB gate driver strength	100 mA	100 mA	500 mA	Selected steps
$V_{GBPFC}$	PFC gate driver voltage high level	10.5 V	4.5 V	15 V <sup>2)</sup>	1.5 V
$I_{GBPFC}$	PFC gate driver strength	100 mA	30 mA	150 mA	Selected steps

**Table 3 Parameters for PFC Protections**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$t_{blank,Vbus,OVP2}$	Blanking time for bus overvoltage threshold, level 2	200 ns	0 s	640 ns	1 / $f_{mclk}$
$t_{blank,Vbus,OVP1}$	Blanking time for bus overvoltage threshold, level 1	400 $\mu$ s	0 s	1 ms	$t_{slot}$
$V_{bus,OVP1}$	Bus overvoltage threshold, level 1	490 V	$V_{bus,stdy,entr,OV}$	600 V <sup>3)</sup>	1/16 V
$t_{blank,Vbus,UV}$	Blanking time for bus undervoltage threshold	500 $\mu$ s	0 s	1 ms	$t_{slot}$
$V_{bus,UV}$	Bus undervoltage threshold	300 V	$V_{bus,start,PFC}$	$V_{bus,stdy,entr,U}$ V	1/16 V
$t_{start,max,PFC}$	Maximum <b>PFC</b> soft start time to settle the bus voltage at startup	200 ms	0 s	500 ms	$t_{slot}$
$t_{blank,Vin,OV}$	Blanking time for input overvoltage threshold	100 ms	0 s	200 ms	$t_{slot}$
$t_{blank,Vin,UV}$	Blanking time for input undervoltage threshold	100 ms	0 s	200 ms	$t_{slot}$

<sup>1</sup> Limited by VCC - 0.5 V

<sup>2</sup> Limited by VCC - 0.5 V

<sup>3</sup> Limited by the voltage rating of the bus capacitors

**Design Support**

**Table 3 Parameters for PFC Protections (continued)**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$V_{in,OV}$	Input overvoltage threshold	319 Vrms	$V_{in,start,max}$	424 Vrms	1/16 Vrms
$V_{in,UV}$	Input undervoltage threshold	76 Vrms	0 V	$V_{in,start,min}$	1/16 Vrms
$V_{in,start,max}$	Maximum input voltage at startup	307 Vrms	$V_{in,start,min}$	$V_{in,OV}$	1/16 Vrms
$V_{in,start,min}$	Minimum input voltage at startup	88 Vrms	$V_{in,UV}$	$V_{in,start,max}$	1/16 Vrms
$t_{blank,OCP2,PFC}$	Blanking time for the peak current limitation, level 2	200 ns	$1 / f_{mclk}$	600 ns	$1 / f_{mclk}$
$t_{blank,OCP1,PFC}$	Blanking time for the peak current limitation, level 1	200 ns	$1 / f_{mclk}$	600 ns	$1 / f_{mclk}$
$V_{CS,OCP1,PFC}$	Maximum peak current voltage	0.75 V	0.1 V	1.08 V	0.125 mV
$t_{blank,CCM,PFC}$	Blanking time for CCM protection	12 ms	0 s	30 ms	$t_{slot}$
Protection <sub>PF</sub> C <sub>EN</sub>	Bit-coded enabling per protection: If set to 1, protection is enabled.		0	65535	One-hot coded
Protection <sub>PF</sub> C <sub>conf1</sub>	Bit-coded reaction per protection: If set to 1, auto-restart is selected. If set to 0, either latch mode or stop is selected.		0	65535	One-hot coded
Protection <sub>PF</sub> C <sub>conf2</sub>	Bit-coded reaction per protection: If set to 1, fast auto restart or stop is selected. If set to 0, normal auto-restart or latch mode is enabled.		0	65535	One-hot coded
Protection <sub>PF</sub> C <sub>conf3</sub>	Bit-coded reaction per protection: If set to 1, limited number of restarts are enabled. If set to zero, unlimited restarts will be done.		0	65535	One-hot coded
Protection <sub>PF</sub> C <sub>conf4</sub>	Bit-coded reaction per protection: If set to 1, VCC charging will be enabled for auto-restarts.		0	65535	One-hot coded

**Table 4 Parameters for Flyback Protections**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$V_{out,UV}$	Output undervoltage threshold	15 V	0 V	$V_{out,start}$	0.125 V
$t_{blank,Vout,UV}$	Blanking time for output undervoltage	500 us	0 s	1 ms	$t_{slot}$
$t_{start,max,FB}$	Maximum <b>FB</b> startup time to detect an output short at startup	5 ms	0 s	200 ms	$t_{slot}$
$V_{out,OV}$	Output overvoltage threshold	55 V	$V_{out,start}$	200 V	0.125 V
$t_{blank,Vout,OV}$	Blanking time for output overvoltage	500 us	0 s	1 ms	$t_{slot}$
$t_{blank,CCM}$	Blanking time for CCM protection	500 us	0 s	1 ms	$t_{slot}$
$I_{out,OC}$	Output overcurrent threshold	3 A	$I_{out,full}$	10 A	0.5 mA
$t_{blank,Iout,OC}$	Blanking time for output overcurrent	500 us	0 s	1 ms	$t_{slot}$
$P_{out,OP}$	Output overpower threshold	120 W	$P_{out,set}$	300 W	0.5 W
$t_{blank,Pout,OP}$	Blanking time for output overpower	500 us	0 s	1 ms	$t_{slot}$

**Design Support**

**Table 4 Parameters for Flyback Protections (continued)**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$t_{blank,Vbus,FB}$	Blanking time for bus voltage plausibility check	500 us	0 s	1 ms	$t_{slot}$
$t_{blank,CSFB2GND}$	Blanking time for the CSFB-to-GND-short check	100 us	0 s	500 us	$t_{slot}$
$t_{blank,TOSC,FB}$	Blanking time for the $t_{OSC,FB}$ being overly long check	40 ms	0 ms	100 ms	20 ms
Protection <sub>FB,EN</sub>	Bit-coded enabling per protection: If set to 1, protection is enabled.		0	65535	One-hot coded
Protection <sub>FB,conf1</sub>	Bit-coded reaction per protection: If set to 1, auto-restart is selected. If set to 0, either latch mode or stop is selected.		0	65535	One-hot coded
Protection <sub>FB,conf2</sub>	Bit-coded reaction per protection: If set to 1, Fast Auto-restart or Stop is selected. If set to 0, normal Auto-restart or latch mode is enabled)		0	65535	One-hot coded
Protection <sub>FB,conf3</sub>	Bit-coded reaction per protection: If set to 1, limited number of restarts are enabled. If set to zero, unlimited restarts are enabled.		0	65535	One-hot coded
Protection <sub>FB,conf4</sub>	Bit-coded reaction per protection: If set to 1, VCC charging will be enabled for auto-restarts.		0	65535	One-hot coded

**Table 5 Parameters for General Protections**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$V_{VCC,OV}$	VCC overvoltage threshold	24.75 V	6 V	24.75 V	0.125 V
$t_{blank,VCC,OV}$	Blanking time for VCC overvoltage	5 ms	0 s	10 ms	$t_{slot}$
Protection <sub>ge,n,EN</sub>	Bit-coded enabling per protection: If set to 1, protection is enabled.		0	65535	One-hot coded
Protection <sub>ge,n,conf1</sub>	Bit-coded reaction per protection: If set to 1, auto-restart is selected. If set to 0, either latch mode or stop is selected.		0	65535	One-hot coded
Protection <sub>ge,n,conf2</sub>	Bit-coded reaction per protection: If set to 1, fast auto-restart or stop is selected. If set to 0, normal auto-restart or latch mode is enabled)		0	65535	One-hot coded
Protection <sub>ge,n,conf3</sub>	Bit-coded reaction per protection: If set to 1, limited number of restarts are enabled. If set to zero, unlimited restarts are enabled.		0	65535	One-hot coded
Protection <sub>ge,n,conf4</sub>	Bit-coded reaction per protection: If set to 1, VCC charging will be enabled for auto-restarts.		0	65535	One-hot coded

**Design Support**

**Table 5 Parameters for General Protections (continued)**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$t_{AR}$	Auto-restart time	1 s	250 ms	4 s	250 ms
$t_{AR,fast}$	Fast auto-restart time	40 ms	5 ms	4 s	5 ms
$N_{AR,max}$	Maximum number of restarts, afterwards latch	10	0	15	1

**Table 6 Parameters for Adaptive Temperature Protection**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$T_{critical}$	Shutoff temperature	110°C	$T_{hot}$	125°C	1°C
$T_{hot}$	Temperature for thermal management	100°C	60°C	$T_{critical}$	1°C
$R_{NTC,hot}$	<b>NTC</b> resistance at $T_{hot}$	1500 $\Omega$	1 $\Omega$	30000 $\Omega$	1 $\Omega$
$R_{NTC,critical}$	<b>NTC</b> resistance at $T_{critical}$	800 $\Omega$	1 $\Omega$	30000 $\Omega$	1 $\Omega$
$t_{step}$	Current reduction time step	2 s	1 s	20 s	$2^{14}t_{slot}$
$I_{out,red}$	Lowest reduced current for thermal management	200 mA	$I_{out,min}$	$I_{out,full}$	0.5 mA
$I_{out,step}$	Output current step	5 mA	0.5 mA	$I_{out,full} - I_{out,red}$	0.5 mA

**Table 7 Parameters for Startup and Shutdown**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$t_{softstart}$	Soft start time step	0.5 ms	0.1 ms	2 ms	$t_{slot}$
$V$	Maximum peak current voltage during startup CS, max, start, FB	0.9 V	$V_{CS,min,FB}$	$V_{CS,max,FB}$	0.125 mV
$V_{CS,CS,step}$	Soft start voltage limit step	0.3 V	0.1 V	$V_{CS,OC1, start}$	0.125 mV
$V_{out,start}$	Output startup voltage	10 V	$V_{out,UV}$	$V_{out,set}$	0.125 V
$t_{sw,start,FB}$	Minimum switching period during startup	1 / 20 kHz	$t_{sw,min}$	$t_{sw,max,FB}$	1 / $f_{mclk}$
$V_{bus,start,FB}$	Bus voltage <b>FB</b> startup threshold	350 V	0 V	$V_{bus,set}$	1/16 V
$V_{bus,start,PFC}$	Bus voltage <b>PFC</b> startup threshold in case of DC input	75 V	0 V	$V_{bus,UV}$	1/16 V

**Table 8 Parameters for PFC Control Loop**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$SVP_{startup}$	PIT1 proportional gain in soft start	4	0	15	1
$SVI_{startup}$	PIT1 integral gain in soft start	7	0	15	1
$SVP_{stdy}$	PIT1 proportional gain in steady state	4	0	15	1
$SVI_{stdy}$	PIT1 integral gain in steady state	7	0	15	1

**Design Support**

**Table 8 Parameters for PFC Control Loop (continued)**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
SVT	PIT1 gain of the T1 filter	6	0	15	1
ESAT	PIT1 error limitation in soft start	16384	0	32767	1
$t_{on,max,PFC}$	PIT1 maximum on-time limit	35 $\mu$ s	15 $\mu$ s	40 $\mu$ s	$1 / f_{mclk}$
$t_{on,min,PFC}$	PIT1 minimum on-time limit	200 ns	0 $\mu$ s	$t_{LEB,PFC}$	$1 / f_{mclk}$
$t_{sw,max,PFC}$	Maximum switching period	$1 / 22$ kHz	$t_{sw,min,PFC}$	$1 / 20$ kHz	$1 / f_{mclk}$
$t_{sw,min,PFC}$	Minimum switching period	$1 / 120$ kHz	$1 / 200$ kHz	$t_{sw,max,PFC}$	$1 / f_{mclk}$
$N_{valley,max,PFC}$	Upper boundary for valley number	5	1	5	1
$t_{valley,blanking,PFC}$	Blanking time for valley change	500 $\mu$ s	0 s	1 ms	$t_{slot}$
$V_{bus,set}$	Bus voltage setpoint	460 V	$V_{bus,UV}$	$V_{bus,OVP1}$	$1/16$ V
$V_{bus,stdy,entr,OV}$	Bus voltage steady state entry overvoltage threshold	472 V	$V_{bus,set}$	$V_{bus,OVP1}$	$1/16$ V
$V_{bus,stdy,entr,UV}$	Bus voltage steady state entry undervoltage threshold	448 V	$V_{bus,UV}$	$V_{bus,set}$	$1/16$ V

**Table 9 Parameters for Flyback Control Loop**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$b_{0,DCM}$	$b_0$ gain of control loop in <b>DCM</b>	$5353 / f_{mclk}/256$	0	$8192 / f_{mclk}/256$	$1 / f_{mclk}/256$
$b_{1,DCM}$	$b_1$ gain of control loop in <b>DCM</b>	$-53 / f_{mclk}/256$	$-8192 / f_{mclk}/256$	0	$1 / f_{mclk}/256$
$b_{0,QRM1}$	$b_0$ gain of control loop in <b>QRM1</b>	$6060 / 65536$ V	0 V	$16384 / 65536$ V	$1 / 65536$ V
$b_{1,QRM1}$	$b_1$ gain of control loop in <b>QRM1</b>	$-60 / 65536$ V	$-16384 / 65536$ V	0 V	$1 / 65536$ V
$K_{P,CV}$	Proportional gain for <b>CV</b> mode	1.9	0	16	0.125
$K_{D,CV}$	Derivative gain for <b>CV</b> mode		28	128	0.125
$P_{out,set}$	Output power limit	100 W	0	150 W	0.5 W
$I_{out,full}$	Non-dimmed output current	2.0 A	$I_{out,min}$	3 A	0.5 mA
$V_{out,set}$	Output voltage setpoint	48 V	$V_{out,UV}$	$V_{out,OV}$	0.125 V
$t_{on,max,FB}$	Maximum on-time limit	15 $\mu$ s	$V_{CS,max,FB} / R_{CS,FB} * L_p / V_{bus,UV}$ <sup>4)</sup>	25 $\mu$ s	$1 / f_{mclk}$
$t_{sw,max,FB}$	Maximum switching period	$1 / 20$ kHz	$t_{sw,min,FB}$	$1 / 16$ kHz	$1 / f_{mclk}$
$t_{sw,min,FB}$	Minimum switching period	$1 / 150$ kHz	$1 / 150$ kHz	$t_{sw,max,FB}$	$1 / f_{mclk}$
$V_{CS,max,FB}$	Maximum peak current voltage	1.09 V	$V_{CS,min,FB}$	$92\% * 1.214$ V	0.125 mV

<sup>4</sup> Maximum on-time occurs if maximum power is transferred at minimum bus voltage.

**Design Support**

**Table 9 Parameters for Flyback Control Loop (continued)**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$V_{CS,min,FB}$	Minimum peak current voltage	0.4 V	$t_{demag,min,FB} * N_p / N_s *$ $V_{out,OV} / L_p *$ $R_{CS,FB}$ <sup>5)</sup>	$V_{CS,max,FB}$	0.125 mV

**Table 10 Parameters for Dimming**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$D_{DIM,max}$	<b>PWM</b> duty cycle for maximum current	90%	5%	95%	0.25%
$D_{DIM,min}$	<b>PWM</b> duty cycle for minimum current	10%	5%	95%	0.25%
$D_{DIM,on}$	<b>PWM</b> duty cycle to exit dim-to-off	5%	5%	95%	0.25%
$D_{DIM,off}$	<b>PWM</b> duty cycle to enter dim-to-off	5%	5%	95%	0.25%
$t_{blank,DIM,off}$	Blanking time until when the <b>PWM</b> input has to be available before dim-to-off is triggered	1 ms	0 ms	10 ms	$t_{slot}$
$N_{DIM}$	Integer dimming curve coefficient	1	1	2	1
$I_{out,min}$	Minimum output current	20 mA	20 mA	$I_{out,full}$	0.5 mA
$n\_PWM\_hys$	PWM detection hysteresis to suppress jitter in the PWM signal	0	6	40	1

**Table 11 Parameters for Fine Tuning**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$K_{coupling}$	<b>FB</b> transformer coupling coefficient	0.98	0.5	2	0.001
$t_{LEB,FB}$	<b>FB</b> Current sense leading edge blanking	200 ns	$1 / f_{mclk}$	600 ns	$1 / f_{mclk}$
$t_{OCP2,FB}$	<b>FB</b> OCP2 blanking time	250 ns	$1 / f_{mclk}$	$63 / f_{mclk}$	$1 / f_{mclk}$
$t_{PDC}$	<b>FB</b> Propagation delay compensation	500 ns	$t_{OCP1,FB}$	2 $\mu$ s	$1 / f_{mclk}$
$t_{OCP1,FB}$	<b>FB</b> OCP1 spike suppression filter	100 ns	50 ns	500 ns	$1 / f_{mclk}$
$t_{CSFB,offset}$	<b>FB</b> sampling offset	200 ns	50 ns	500 ns	$1 / f_{mclk}$
$t_{sw,hysteresis}$	<b>FB</b> switching period hysteresis for QRM/DCM mode changes	600 ns	20 ns	1000 ns	$1 / f_{mclk}$
$t_{rsup,FB}$	<b>FB</b> ZCD ringing suppression	1.2 $\mu$ s	$1 / f_{mclk}$	2 $\mu$ s	$1 / f_{mclk}$
$t_{ZCD,PD,FB}$	<b>FB</b> Delay of zero-crossing signal	200 ns	0 s	1 $\mu$ s	$1 / f_{mclk}$
$t_{ZCD,PD,RE,FB}$	<b>FB</b> Rising edge delay of zero-crossing signal	450 ns	0 s	1 $\mu$ s	$1 / f_{mclk}$
$t_{gate,on}$	<b>FB</b> Turn-on delay of MOSFET	100 ns	0 s	1 $\mu$ s	$1 / f_{mclk}$
$t_{LEB,PFC}$	<b>PFC</b> On-time leading edge blanking	200 ns	$1 / f_{mclk}$	600 ns	$1 / f_{mclk}$

<sup>5</sup> The minimum peak current must ensure that  $t_{demag,min,FB}$  is maintained.

**Design Support**

**Table 11 Parameters for Fine Tuning (continued)**

Symbol	Description	Example	Minimum Value	Maximum Value	Granularity
$t_{zCD,PD,PFC}$	<b>PFC</b> Delay of 0.5 V crossing to real zero-crossing signal	42 ns	-1 us	1 us	$1 / f_{mclk}$
$N_{tosc,upd,PFC}$	<b>PFC</b> AC half cycle number to take oscillation measurement	0	0	255	1
$t_{osc,init,PFC}$	<b>PFC</b> Oscillation period initialization value	1.5 us	0 s	8 us	$1 / f_{mclk}$
$t_{osc,delay,PFC}$	<b>PFC</b> Delay after zero-crossing to measure oscillation period	2 ms	0 s	12 ms	$t_{slot}$
$k_{i,PFC}$	<b>PFC</b> THD optimization coefficient	0.75	0	16	0.125
$t_{src,blanking,PF C}$	Blanking time for AC/DC source change	12 ms	12 ms	30 ms	1 ms
$t_{rms,reset,PFC}$	Reset time of RMS search	20 ms	$t_{src,blanking,PF C}$	30 ms	1 ms

### 4.3 List of Fixed Parameters

This list shows the fixed parameters and their associated values – i.e. parameters whose values cannot be changed.

**Table 12 List of Fixed Parameters**

Symbol	Description	Value
$V_{CS,OCp2}$	Primary overcurrent protection	1.619 V
$t_{demag,min,FB}$	<b>FB</b> minimum demagnetizing time	2.0 us
$V_{UVOFF}$	VCC undervoltage threshold	6.07 V
$f_{mclk}$	Main clock frequency	50.0 MHz
$t_{slot}$	Firmware task scheduling interval	32 us
$V_{REF}$	Internal reference voltage	2.428 V
$k_{pkto rms}$	Constant to convert from peak to RMS values	0.707 (approx. 181/256)
$C_{IIR,PFC}$	Coefficient of the IIR LP filter for bus voltage	4

**Electrical Characteristics and Parameters**

## 5 Electrical Characteristics and Parameters

All signals are measured with respect to the ground pin, GND. The voltage levels are valid provided other ratings are not violated.

### 5.1 Package Characteristics

**Table 13 Package Characteristics**

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Thermal resistance for PG-DSO-16	$R_{thJA}$	—	119	K/W	

### 5.2 Absolute Maximum Ratings

**Attention:** *Stresses above the values listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.*

**Table 14 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Voltage externally supplied to pin VCC	$V_{VCCEXT}$	-0.5	26	V	voltage that can be applied to pin VCC by an external voltage source
Voltage at pin GDx	$V_{GDx}$	-0.5	$V_{VCC} + 0.3$	V	if gate driver is not configured for digital I/O
Junction temperature	$T_J$	-40	125	°C	max. operating frequency 66 MHz $f_{MCLK}$
Storage temperature	$T_S$	-55	150	°C	
Soldering temperature	$T_{SOLD}$	—	260	°C	Wave Soldering <sup>1)</sup>
Latch-up capability	$I_{LU}$	—	150	mA	<sup>2)</sup> Pin voltages acc. to abs. max. ratings
ESD capability HBM	$V_{HBM}$	—	2000	V	<sup>3)</sup>
ESD capability CDM	$V_{CDM}$	—	500	V	<sup>4)</sup>

<sup>1)</sup> According to JESD22-A111 Rev A.

<sup>2)</sup> Latch-up capability according to JEDEC JESD78D,  $T_A = 85^\circ\text{C}$ .

<sup>3)</sup> ESD-HBM according to ANSI/ESDA/JEDEC JS-001-2012.

<sup>4)</sup> ESD-CDM according to JESD22-C101F.



**Electrical Characteristics and Parameters**

**Table 14 Absolute Maximum Ratings (continued)**

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Input Voltage Limit	$V_{IN}$	-0.5	3.6	V	Voltage externally supplied to pins GPIO, MFIO, CS, ZCD, GPIO, VS, GDx (if GDx is configured as digital I/O). (If not stated different)
Maximum permanent negative clamping current for ZCD and CS	$-I_{CLN\_DC}$	—	2.5	mA	RMS
Maximum transient negative clamping current for ZCD and CS	$-I_{CLN\_TR}$	—	10	mA	pulse < 500ns
Maximum negative transient input voltage for ZCD	$-V_{IN\_ZCD}$	—	1.5	V	pulse < 500ns
Maximum negative transient input voltage for CS	$-V_{IN\_CS}$	—	3.0	V	pulse < 500ns
Maximum permanent positive clamping current for CS	$I_{CLP\_DC}$	—	2.5	mA	RMS
Maximum transient positive clamping current for CS	$I_{CLP\_TR}$	—	10	mA	pulse < 500ns
Maximum current into pin VIN	$I_{AC}$	—	10	mA	for charging operation
Maximum sum of input clamping high currents for digital input stages of device	$I_{CLH\_sum}$	—	300	$\mu$ A	limits for each individual digital input stage have to be respected
Voltage at HV pin	$V_{HV}$	-0.5	600	V	

### 5.3 Operating Conditions

The recommended operating conditions are shown for which the DC Electrical Characteristics are valid.

**Table 15 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Ambient temperature	$T_A$	-40	85	°C	
Junction Temperature	$T_J$	-40	125	°C	max. 66 MHz $f_{MCLK}$
Lower VCC limit	$V_{VCC}$	$V_{UVOFF}$	—	V	device is held in reset when $V_{VCC} < V_{UVOFF}$
Voltage externally supplied to VCC pin	$V_{VCCEXT}$	—	24	V	maximum voltage that can be applied to pin VCC by an external voltage source
Gate driver pin voltage	$V_{GD}$	-0.5	$V_{VCC} + 0.3$	V	

**Electrical Characteristics and Parameters**

**5.4 DC Electrical Characteristics**

The electrical characteristics provide the spread of values applicable within the specified supply voltage and junction temperature range,  $T_J$  from  $-40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$ .

Devices are tested in protection at  $T_A = 25\text{ }^\circ\text{C}$ . Values have been verified either with simulation models or by device characterization up to  $125\text{ }^\circ\text{C}$ .

Typical values represent the median values related to  $T_A = 25\text{ }^\circ\text{C}$ . All voltages refer to GND, and the assumed supply voltage is  $V_{VCC} = 18\text{ V}$  if not otherwise specified.

*Note: Not all values given in the tables are tested during production testing. Values not tested are explicitly marked.*

**Attention:** *The Vcc pin voltage must be higher than 3.4V before the voltage of any other pins (except GND and HV pins) exceeds 1.2V.*

**Table 16 Power Supply Characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC_ON threshold	$V_{VCCon}$	—	$V_{SELF}$	—	V	Self-powered startup (default)
VCC_ON_SELF threshold	$V_{SELF}$	19	20.5	22	V	$dV_{VCC}/dt = 0.2\text{ V/ms}$
VCC_ON_SELF delay	$t_{SELF}$	—	—	2.1	$\mu\text{s}$	Reaction time of $V_{VCC}$ monitor
VCC_UVOFF current	$I_{VCCUVOFF}$	5	20	40	$\mu\text{A}$	$V_{VCC} < V_{SELF}(\text{min}) - 0.3\text{ V}$ or $V_{VCC} < V_{EXT}(\text{min}) - 0.3\text{ V}^5$
UVOFF threshold	$V_{UVOFF}$	—	6.0	—	V	$\text{SYS\_CFG0.SELUVTHR} = 00_B$
UVOFF threshold tolerance	$\Delta_{UVOFF}$	—	—	$\pm 5$	%	This value defines the tolerance of $V_{UVOFF}$
UVOFF filter constant	$t_{UVOFF}$	600	—	—	ns	1V overdrive
UVLO (UVWAKE) threshold	$V_{UVLO}$	—	$V_{UVOFF} \cdot 1.25$	—	V	
UVWAKE threshold tolerance	$\Delta_{UVLO}$	—	—	$\pm 5$	%	This value defines the tolerance of $V_{UVLO}$
UVLO (UVWAKE) filter constant	$t_{UVLO}$	0.6	—	2.2	$\mu\text{s}$	1 V overdrive
OVLO (OVWAKE) threshold	$V_{OVLO}$	—	$V_{SELF}$	—	V	
OVLO (OVWAKE) filter constant	$t_{OVLO}$	0.6	—	2.4	$\mu\text{s}$	1 V overdrive

<sup>5</sup> Tested at  $V_{VCC} = 5.5\text{ V}$

**Electrical Characteristics and Parameters**

**Table 16 Power Supply Characteristics (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDDP voltage	V <sub>VDDP</sub>	3.04	3.20	3.36	V	At PMD0/PSMD1. Some internal values refer to V <sub>VDDP</sub> / V <sub>VDDA</sub> and V <sub>VDDPPS</sub> / V <sub>VDDAPS</sub> respectively.
VDDA voltage	V <sub>VDDA</sub>	3.20	3.31	3.42	V	At PMD0/PSMD1. Some internal values refer to V <sub>VDDP</sub> / V <sub>VDDA</sub> and V <sub>VDDPPS</sub> / V <sub>VDDAPS</sub> respectively.
Nominal range 0% to 100%	V <sub>ADCVCC</sub>	0	—	V <sub>REF</sub>	V	V <sub>ADCVCC</sub> = 0.09 · V <sub>VCC</sub> <sup>6)</sup>
Reduced VCC range for ADC measurement	R <sub>ADCVCC</sub>	8	—	92	%	<sup>7)8)</sup>
Maximum error for ADC measurement (8-bit result)	TET0 <sub>VCC</sub>	—	—	3.8	LSB <sub>8</sub>	
Maximum error for ADC measurement (8-bit result)	TET256 <sub>VCC</sub>	—	—	5.2	LSB <sub>8</sub>	
Gate driver current consumption excl. gate charge current	I <sub>VCCGD</sub>	—	0.26	0.35	mA	T <sub>j</sub> ≤ 125 °C
VCC quiescent current in PMD0	I <sub>VCCPMD0</sub>	—	11	13	mA	All registers have reset values, clock is active at 66 MHz, CPU is stopped, T <sub>j</sub> ≤ 85 °C
VCC quiescent current in PMD0	I <sub>VCCPMD0</sub>	—	—	14.5	mA	All registers have reset values, clock is active at 66 MHz, CPU is stopped, T <sub>j</sub> ≤ 125 °C
VCC quiescent current in power saving mode PSDM3 with standby logic active	I <sub>VCCPSMD3</sub>	—	0.25	0.45	mA	T <sub>j</sub> ≤ 125 °C WU_PWD_CFG = 28 <sub>H</sub>
VCC quiescent current in power saving mode PSDM4 with standby logic active	I <sub>VCCPSMD4</sub>	—	0.14	0.23	mA	T <sub>j</sub> ≤ 125 °C WU_PWD_CFG = 00 <sub>H</sub>

<sup>6)</sup> Theoretical minimum value, real minimum value is related to V<sub>UVOFF</sub> threshold.

<sup>7)</sup> Operational values.

<sup>8)</sup> Note that the system is turned off if V<sub>VCC</sub> < V<sub>UVOFF</sub>.

**Electrical Characteristics and Parameters**

**Table 17 Electrical Characteristics of the GDFB Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	$\mu\text{A}$	only digital input
Input clamping current, high	$I_{CLH}$	—	—	100	$\mu\text{A}$	only digital input
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	$V_{APD}$	—	—	1.6	V	$I_{GD} = 5 \text{ mA}$
$R_{PPD}$ value	$R_{PPD}$	—	600	—	k $\Omega$	Permanent pull-down resistor inside gate driver
$R_{PPD}$ tolerance	$\Delta_{PPD}$	—	—	$\pm 25$	%	Permanent pull-down resistor inside gate driver
Driver output low impedance for GD0	$R_{GDL}$	—	—	4.4	$\Omega$	$T_J \leq 125 \text{ }^\circ\text{C}$ , $I_{GD} = 0.1 \text{ A}$
Nominal output high voltage in PWM mode	$V_{GDH}$	—	10.5	—	V	$\text{GDx\_CFG.VOL} = 3$ , $I_{GDH} = -1 \text{ mA}$
Output voltage tolerance	$\Delta_{VGDH}$	—	—	$\pm 5$	%	Tolerance of programming options if $V_{GDH} > 10 \text{ V}$ , $I_{GDH} = -1 \text{ mA}$
Rail-to-rail output high voltage	$V_{GDHRR}$	$V_{VCC} - 0.5$	—	$V_{VCC}$	V	If $V_{VCC} < \text{programmed } V_{GDH}$ and output at high state
Output high current in PWM mode for GD0	$-I_{GDH}$	—	100	—	mA	$\text{GDx\_CFG.CUR} = 8$
Output high current tolerance in PWM mode	$\Delta_{IGDH}$	—	—	$\pm 15$	%	Calibrated <sup>9)</sup>
Discharge current for GD0	$I_{GDDIS}$	800	—	—	mA	$V_{GD} = 4 \text{ V}$ and driver at low state
Output low reverse current	$-I_{GDREVL}$	—	—	100	mA	Applies if $V_{GD} < 0 \text{ V}$ and driver at low state
Output high reverse current in PWM mode	$I_{GDREVLH}$	—	1/6 of $I_{GDH}$	—		Applies if $V_{GD} > V_{GDH} + 0.5 \text{ V (typ)}$ and driver at high state

<sup>9</sup> referred to  $\text{GDx\_CFG.CUR} = 16$

**Electrical Characteristics and Parameters**

**Table 18 Electrical Characteristics of the CSFB Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	$V_{INP}$	-0.5	—	3.0	V	
OCP2 comparator reference voltage, derived from $V_{VDPA}$ , given values assuming $V_{VDPA} = V_{VDPA,typ}$	$V_{OCP2}$	—	1.6	—	V	SYS_CFG0.OCP2 = 00 <sub>B</sub>
Threshold voltage tolerance	$\Delta_{VOCP2}$	—	—	±5	%	Voltage divider tolerance
Comparator propagation delay	$t_{OCP2PD}$	15	—	35	ns	
Minimum comparator input pulse width	$t_{OCP2PW}$	—	—	30	ns	
OCP2F comparator propagation delay	$t_{OCP2FPD}$	70	—	170	ns	$dV_{CS}/dt = 100 \text{ V}/\mu\text{s}$
Delay from $V_{CS}$ crossing $V_{CSOCP2}$ to begin of GDx turn-off ( $I_{GD0} > 2\text{mA}$ )	$t_{CSGDxOCP2}$	125	135	190	ns	$dV_{CS}/dt = 100 \text{ V}/\mu\text{s}$ ; $f_{MCLK} = 66 \text{ MHz}$ . GDx driven by QR_GATE FIL_OCP2.STABLE = 3
OCP1 operating range	$V_{OCP1}$	0	—	$V_{REF}/2$	V	RANGE = 00 <sub>B</sub>
OCP1 threshold at full scale setting (CS_OCP1LVL=FF <sub>H</sub> ) for CS0	$V_{OCP1FS}$	1192	1229	1266	mV	RANGE = 00 <sub>B</sub>
Delay from $V_{CS}$ crossing $V_{CSOCP1}$ to CS_OCP1 rising edge, 1.2 V range	$t_{CSOCP1}$	90	170	250	ns	Input signal slope $dV_{CS}/dt = 150 \text{ mV}/\mu\text{s}$ . This slope represents a use case of a switch-mode power supply with minimum input voltage.
Delay from CS_OCP1 rising edge to QR_GATE falling edge	$t_{OCP1GATE}$	—	—	12	ns	STB_RET31. OCP_ASM_SEL=0
Delay from QR_GATE falling edge to start of GDx turn-off	$t_{GATEGDx}$	1	3	5	ns	GDx driven by QR_GATE. Measured up to $I_{GDx} > 2 \text{ mA}$
OCP1 comparator input single pulse width filter	$t_{OCP1PW}$	60	—	95	ns	Shorter pulses than min. are suppressed, longer pulses than max. are passed

**Electrical Characteristics and Parameters**

**Table 18 Electrical Characteristics of the CSFB Pin (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Nominal S&H operating range 0% to 100%	$V_{CSH}$	0	—	$V_{REF}/2$	V	CS_ICR.RANGE =00 <sub>B</sub>
Reduced S&H operating range	RR <sub>CVSH</sub>	8	—	92	%	CS_ICR.RANGE =00 <sub>B</sub> Operational values
Maximum error of CS0 S&H for corrected measurement (8-bit result)	TET0 <sub>CS0S</sub>	—	—	4.7	LSB	CS_ICR.RANGE =00 <sub>B</sub>
Maximum error of CS0 S&H for corrected measurement (8-bit result)	TET256 <sub>CS0S</sub>	—	—	6.0	LSB	CS_ICR.RANGE =00 <sub>B</sub>
Nominal S&H operating range 0% to 100%	$V_{CSH}$	0	—	$V_{REF}/6$	V	CS_ICR.RANGE =11 <sub>B</sub>
Reduced S&H operating range	RR <sub>CVSH</sub>	20	—	80	%	CS_ICR.RANGE =11 <sub>B</sub> Operational values
Maximum error of CS0 S&H for corrected measurement (8-bit result)	TET0 <sub>CS0S</sub>	—	—	8.0	LSB	CS_ICR.RANGE =11 <sub>B</sub>
Maximum error of CS0 S&H for corrected measurement (8-bit result)	TET256 <sub>CS0S</sub>	—	—	8.7	LSB	CS_ICR.RANGE =11 <sub>B</sub>
S&H delay of input buffer	$t_{CSHST}$	—	—	510	ns	Referring to jump in input voltage. Limits the minimum gate driver T <sub>on</sub> time.

**Table 19 Electrical Characteristics of the ZCD Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	$V_{INP}$	-0.5	—	3.3	V	
Input clamping current, high	$I_{CLH}$	—	—	100	μA	
Zero-crossing threshold	$V_{ZCTHR}$	15	40	70	mV	
Comparator propagation delay	$t_{ZCPD}$	30	50	70	ns	$dV_{ZCD}/dt = 4 V/\mu s$

**Electrical Characteristics and Parameters**

**Table 19 Electrical Characteristics of the ZCD Pin (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage negative clamping level	$-V_{INPCLN}$	140	180	220	mV	Analog clamp activated
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	4	mA	CRNG = 00 <sub>B</sub> Gain = 600 mV/mA
Reduced I/V-conversion operating range	RR <sub>IV</sub>	5	—	80	%	
Maximum error for corrected ADC measurement (8-bit result)	TET0 <sub>IV</sub>	—	—	4.1	LSB <sub>8</sub>	CRNG = 00 <sub>B</sub>
Maximum error for corrected ADC measurement (8-bit result)	TET256 <sub>IV</sub>	—	—	9.7	LSB <sub>8</sub>	CRNG = 00 <sub>B</sub>
Maximum deviation between ZCD clamp voltage and trim result stored in OTP	E <sub>ZCDClp</sub>	—	—	±5	%	$-I_{IV} > 0.25$ mA
IV-conversion delay of input buffer	t <sub>IVST</sub>	—	—	900	ns	Refers to jump in input current <sup>10)</sup>
Nominal S&H input voltage range 0% to 100%	V <sub>ZSH</sub>	0	—	$2/3 \cdot V_{REF}$	V	SHRNG = 0 <sub>B</sub>
Nominal S&H input voltage range 0% to 100%	V <sub>ZSH</sub>	$V_{REF} / 2$	—	$7/6 \cdot V_{REF}$	V	SHRNG = 1 <sub>B</sub>
Reduced S&H input voltage range	RR <sub>ZVSH</sub>	4	—	95	%	
Maximum error for corrected ADC measurement (8-bit result)	TET0 <sub>ZVS0</sub>	—	—	3.7	LSB <sub>8</sub>	SHRNG = 0 <sub>B</sub>
Maximum error for corrected ADC measurement (8-bit result)	TET256 <sub>ZVS0</sub>	—	—	4.9	LSB <sub>8</sub>	SHRNG = 0 <sub>B</sub>

<sup>10</sup> Limits the minimum gate driver T<sub>on</sub> time.

**Electrical Characteristics and Parameters**

**Table 19 Electrical Characteristics of the ZCD Pin (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum error for corrected ADC measurement (8-bit result)	TET0 <sub>ZVS1</sub>	—	—	4.2	LSB <sub>8</sub>	SHRNG = 1 <sub>B</sub>
Maximum error for corrected ADC measurement (8-bit result)	TET256 <sub>ZVS1</sub>	—	—	5.8	LSB <sub>8</sub>	SHRNG = 1 <sub>B</sub>
S&H delay of input buffer referring to jump of input voltage	t <sub>ZSHST</sub>	—	—	1.0	μs	SHRNG = 0 <sub>B</sub> T <sub>J</sub> ≤ 125 °C
S&H delay of input buffer referring to jump of input voltage	t <sub>ZSHST</sub>	—	—	1.6	μs	SHRNG = 1 <sub>B</sub> T <sub>J</sub> ≤ 125 °C

**Table 20 Electrical Characteristics of the VS Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Nominal measurement range 0% to 100%	V <sub>VS</sub>	0	—	V <sub>REF</sub>	V	Gain 1, no offset
Nominal measurement range 0% to 100%	V <sub>VS</sub>	5/6·V <sub>REF</sub>	—	7/6·V <sub>REF</sub>	V	Gain 3, with offset
Reduced operating range	RR <sub>VVS</sub>	5	—	95	%	Gain 1, no offset
Reduced operating range	RR <sub>VVS</sub>	10	—	90	%	Gain 3, with offset
Maximum error for corrected measurement (8-bit result)	TET0 <sub>VS</sub>	—	—	4.1	LSB <sub>8</sub>	Range 1, no offset
Maximum error for corrected measurement (8-bit result)	TET256 <sub>VS</sub>	—	—	5.6	LSB <sub>8</sub>	Range 1, no offset
Maximum error for corrected measurement (8-bit result)	TET0 <sub>VS</sub>	—	—	12.0	LSB <sub>8</sub>	Range 2, with offset
Maximum error for corrected measurement (8-bit result)	TET256 <sub>VS</sub>	—	—	12.9	LSB <sub>8</sub>	Range 2, with offset
Overvoltage comparator threshold	THR <sub>OV</sub>	2.70	2.8	2.90	V	
Overvoltage comparator propagation delay	t <sub>PDOV</sub>	—	—	300	μs	Step at input



**Electrical Characteristics and Parameters**

**Table 21 Electrical Characteristics of the HV Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Leakage current at HV pin	$I_{HVleak}$	—	—	10	$\mu A$	$V_{HV} = 600 V$ HV startup cell disabled
Nominal current for measurement path 0% to 100%	$I_{MEAS}$	0	—	4.8	mA	CURRNG = 10 <sub>B</sub>
Reduced measurement range for current path	RR <sub>IMEAS</sub>	5	—	80	%	CURRNG = 10 <sub>B</sub> . Operational values.
Maximum error for corrected ADC measurement (8-bit result, temperature gain correction applied)	TET0 <sub>DP</sub>	—	—	3.7	LSB <sub>8</sub>	CURRNG = 10 <sub>B</sub>
Maximum error for corrected ADC measurement (8-bit result, temperature gain correction applied)	TET256 <sub>DP</sub>	—	—	7.9	LSB <sub>8</sub>	CURRNG = 10 <sub>B</sub>
Comparator threshold (in % of full range of $I_{MEAS}$ )	THR <sub>COMP</sub>	15	20	25	%	COMPTHR= 00 <sub>B</sub>
Comparator threshold (in % of full range of $I_{MEAS}$ )	THR <sub>COMP</sub>	25	30	35	%	COMPTHR= 01 <sub>B</sub>
Comparator threshold (in % of full range of $I_{MEAS}$ )	THR <sub>COMP</sub>	35	40	45	%	COMPTHR= 10 <sub>B</sub>
Comparator threshold (in % of full range of $I_{MEAS}$ )	THR <sub>COMP</sub>	45	50	55	%	COMPTHR= 11 <sub>B</sub>

**Table 22 Electrical Characteristics of the PWM Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{INPUT}$	—	—	10	pF	
Input low voltage	$V_{IL}$	—	—	1.0	V	
Input high voltage	$V_{IH}$	2.0	—	—	V	
Input leakage current, no pull device	$I_{LK}$	-5	—	+1	$\mu A$	$V_{MFIO} = 0 V / 3 V$
Input low current with active weak pull-up WPU	- $I_{LPU}$	30	—	90	$\mu A$	Measured at max. $V_{IL}$
Input high current with active weak pull-down WPD	$I_{HPD}$	90	—	300	$\mu A$	Measured at min. $V_{IH}$

**Electrical Characteristics and Parameters**

**Table 22 Electrical Characteristics of the PWM Pin (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Max. input frequency	$f_{\text{INPUT}}$	15	—	—	MHz	
Pull-up resistor value	$R_{\text{PU}}$	—	2.25	—	k $\Omega$	$R_{\text{PU}}=1111_{\text{B}}$
Pull-up resistor tolerance	$\Delta_{\text{RPU}}$	—	—	$\pm 20$	%	Overall tolerance
PWM input frequency	$f_{\text{PWM}}$	500	—	2000	Hz	
PWM duty cycle	$D_{\text{PWM}}$	5	—	95	%	

**Table 23 Electrical Characteristics of the TEMP Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
MFIO reference voltage	$V_{\text{MFIOREF}}$	—	$V_{\text{REF}}$	—	V	Selection = $V_{\text{REF}}$
Nominal range 0% to 100%	$V_{\text{MFIO}}$	0	—	$V_{\text{REF}}$	V	Gain = 1
Reduced operating range	$RR_{\text{VMFIO}}$	4	—	96	%	Gain = 1. Operational values.
Maximum error for corrected measurement (8-bit result)	$TET0_{\text{MFIO}}$	—	—	4.0	LSB <sub>8</sub>	Gain = 1
Maximum error for corrected measurement (8-bit result)	$TET256_{\text{MFIO}}$	—	—	4.8	LSB <sub>8</sub>	Gain = 1
Offset calibration voltage	$V_{\text{CAL}}$	—	$V_{\text{MFIOREF}}/8$	—	V	
Offset calibration voltage absolute tolerance	$\Delta_{\text{VCAL}}$	—	—	$\pm 3$	LSB	Ref. to $V_{\text{MFIOREF}}=V_{\text{REF}}$ , Gain = 1
Offset calibration voltage variation over temperature	$\Delta_{\text{VCAL\_TMP}}$	—	—	$\pm 1$	LSB	Ref. to $V_{\text{MFIOREF}}=V_{\text{REF}}$ , Gain = 1
Pull-up resistor value	$R_{\text{PU}}$	—	11	—	k $\Omega$	$R_{\text{PU}}=0110_{\text{B}}$
Pull-up resistor tolerance	$\Delta_{\text{RPU}}$	—	—	$\pm 20$	%	Overall tolerance

**Table 24 Electrical Characteristics of the CSPFC Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	$V_{\text{INP}}$	-0.5	—	3.0	V	
OCP1 operating range	$V_{\text{OCP1}}$	0	—	$V_{\text{REF}}/2$	V	$\text{RANGE}=00_{\text{B}}$

**Electrical Characteristics and Parameters**

**Table 24 Electrical Characteristics of the CSPFC Pin (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OCP2 comparator reference voltage, derived from $V_{VDDA}$ , given values assuming $V_{VDDA} = V_{VDDA,typ}$	$V_{OCP2}$	—	1.6	—	V	SYS_CFG0.OCP2 = 00 <sub>B</sub>
Threshold voltage tolerance	$\Delta V_{OCP2}$	—	—	±5	%	Voltage divider tolerance
Comparator propagation delay	$t_{OCP2PD}$	15	—	35	ns	
Minimum comparator input pulse width	$t_{OCP2PW}$	—	—	30	ns	
OCP2F comparator propagation delay	$t_{OCP2FPD}$	70	—	170	ns	$dV_{CS}/dt = 100 \text{ V}/\mu\text{s}$
Delay from $V_{CS}$ crossing $V_{CSOCP2}$ to begin of GDx turn-off ( $I_{GD0} > 2\text{mA}$ )	$t_{CSGDxOCP2}$	125	135	190	ns	$dV_{CS}/dt = 100 \text{ V}/\mu\text{s}$ ; $f_{MCLK} = 66 \text{ MHz}$ . GDx driven by QR_GATE FIL_OCP2.STABLE = 3
Nominal S&H operating range 0% to 100%	$V_{CSH}$	0	—	$V_{REF}/2$	V	CS_ICR.RANGE = 00 <sub>B</sub>
Reduced S&H operating range	$RR_{CVSH}$	4	—	90	%	Operational values
Hysteretic comparator threshold	$THR_{HYS}$	—	0.54	—	V	1 → 0 transition
Hysteretic comparator threshold	$THR_{HYS}$	—	1.53	—	V	0 → 1 transition
Hysteretic comparator threshold tolerance	$\Delta THR_{HYS}$	—	—	±120	mV	
Hysteretic comparator propagation delay	$t_{PDHYS}$	—	90	—	ns	Rising edge
Hysteretic comparator propagation delay	$t_{PDHYS}$	—	40	—	ns	Falling edge
Hysteretic comparator minimum input pulse width	$t_{PWHYS}$	—	—	300	ns	

**Electrical Characteristics and Parameters**

**Table 25 Electrical Characteristics of the UART Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	$\mu\text{A}$	only digital input
Input clamping current, high	$I_{CLH}$	—	—	100	$\mu\text{A}$	only digital input
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	$V_{APD}$	—	—	1.6	V	$I_{GD} = 5 \text{ mA}$
Input capacitance	$C_{INPUT}$	—	—	25	pF	
Input low voltage	$V_{IL}$	—	—	1.0	V	
Input high voltage	$V_{IH}$	2.1	—	—	V	
Input low current with active weak pull-up WPU	$-I_{LPU}$	30	—	90	$\mu\text{A}$	Measured at max. $V_{IL}$
Max. input frequency	$f_{INPUT}$	15	—	—	MHz	
Output low voltage	$V_{OL}$	—	—	0.8	V	$I_{OL} = 2 \text{ mA}$
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -2 \text{ mA}$
Output sink current	$I_{OL}$	—	—	2	mA	
Output source current	$-I_{OH}$	—	—	2	mA	
Output rise time (0 → 1)	$t_{RISE}$	—	—	50	ns	20 pF load, push/pull output
Output fall time (1 → 0)	$t_{FALL}$	—	—	50	ns	20 pF load, push/pull or open-drain output
Max. output switching frequency	$f_{SWITCH}$	10	—	—	MHz	
UART baudrate	$f_{UART}$	9600		105000	baud	

**Table 26 Electrical Characteristics of the GDPFC Pin**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	$\mu\text{A}$	only digital input
Input clamping current, high	$I_{CLH}$	—	—	100	$\mu\text{A}$	only digital input
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	$V_{APD}$	—	—	1.6	V	$I_{GD} = 5 \text{ mA}$

**Electrical Characteristics and Parameters**

**Table 26 Electrical Characteristics of the GDPFC Pin (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
R <sub>PPD</sub> value	R <sub>PPD</sub>	—	600	—	kΩ	Permanent pull-down resistor inside gate driver
R <sub>PPD</sub> tolerance	Δ <sub>PPD</sub>	—	—	±25	%	Permanent pull-down resistor inside gate driver
Driver output low impedance for GD1/2	R <sub>GD<sub>L</sub></sub>	—	—	7.0	Ω	T <sub>J</sub> ≤ 125 °C, I <sub>GD</sub> = 0.1 A
Nominal output high voltage in PWM mode	V <sub>GDH</sub>	—	10.5	—	V	GDx_CFG.VOL = 3, I <sub>GDH</sub> = -1 mA
Output voltage tolerance	Δ <sub>VG<sub>DH</sub></sub>	—	—	±5	%	Tolerance of programming options if V <sub>GDH</sub> > 10 V, I <sub>GDH</sub> = -1 mA
Rail-to-rail output high voltage	V <sub>GDHRR</sub>	V <sub>VCC</sub> - 0.5	—	V <sub>VCC</sub>	V	If V <sub>VCC</sub> < programmed V <sub>GDH</sub> and output at high state
Output high current in PWM mode for GD1/2	-I <sub>GDH</sub>	—	104	—	mA	GDx_CFG.CUR = 24
Output high current tolerance in PWM mode	Δ <sub>I<sub>GDH</sub></sub>	—	—	±15	%	Calibrated <sup>11)</sup>
Discharge current for GD1/2	I <sub>GDDIS</sub>	500	—	—	mA	V <sub>GD</sub> = 4 V and driver at low state
Output low reverse current	-I <sub>GDREVL</sub>	—	—	100	mA	Applies if V <sub>GD</sub> < 0 V and driver at low state
Output high reverse current in PWM mode	I <sub>GDREVL</sub>	—	1/6 of I <sub>GDH</sub>	—	—	Applies if V <sub>GD</sub> > V <sub>GDH</sub> + 0.5 V (typ) and driver at high state

**Table 27 Electrical Characteristics of the A/D Converter**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Integral non-linearity	INL	—	—	1	LSB <sub>8</sub>	<sup>12)</sup>

<sup>11</sup> referred to GDx\_CFG.CUR = 16

<sup>12</sup> ADC capability measured via channel MFIO without errors due to switching of neighbouring pins, e.g. gate drivers, measured with STC = 5. MFIO buffer non-linearity masked out by taking ADC output values ≥ 30 only.

**Electrical Characteristics and Parameters**

**Table 28 Electrical Characteristics of the Reference Voltage**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Reference voltage	$V_{REF}$	—	2.428	—	V	
VREF overall tolerance	$\Delta V_{REF}$	—	—	$\pm 1.5$	%	Trimmed, $T_j \leq 125^\circ\text{C}$ and aging

**Table 29 Electrical Characteristics of the OTP Programming**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OTP programming voltage at the VCC pin for range C000 <sub>H</sub> to CFFF <sub>H</sub>	$V_{PP}$	7.35	7.5	7.65	V	Operational values
OTP programming voltage at the VCC pin for range D000 <sub>H</sub> to DFFF <sub>H</sub>	$V_{PP}$	9.0	—	$V_{VCC}$	V	Operational values
OTP programming current	$I_{PP}$	—	1.6	—	mA	Programming of 4 bits in parallel

**Table 30 Electrical Characteristics of the Clock Oscillators**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Master clock oscillation period including all variations	$t_{MCLK}$	19.2	20.0	21.1	ns	In reference to 50 MHz $f_{MCLK}$
Main clock oscillator frequency variation of stored DPARAM frequency	$\Delta_{MCLK}$	-3.2	—	+2.0	%	Temperature drift and aging only, 50 MHz $f_{MCLK}$
Standby clock oscillator frequency	$f_{STBCLK}$	96	100	104	kHz	Trimming tolerance at $T_A = 25^\circ\text{C}$
Standby clock oscillator frequency	$f_{STBCLK}$	90	100	110	kHz	Overall tolerance

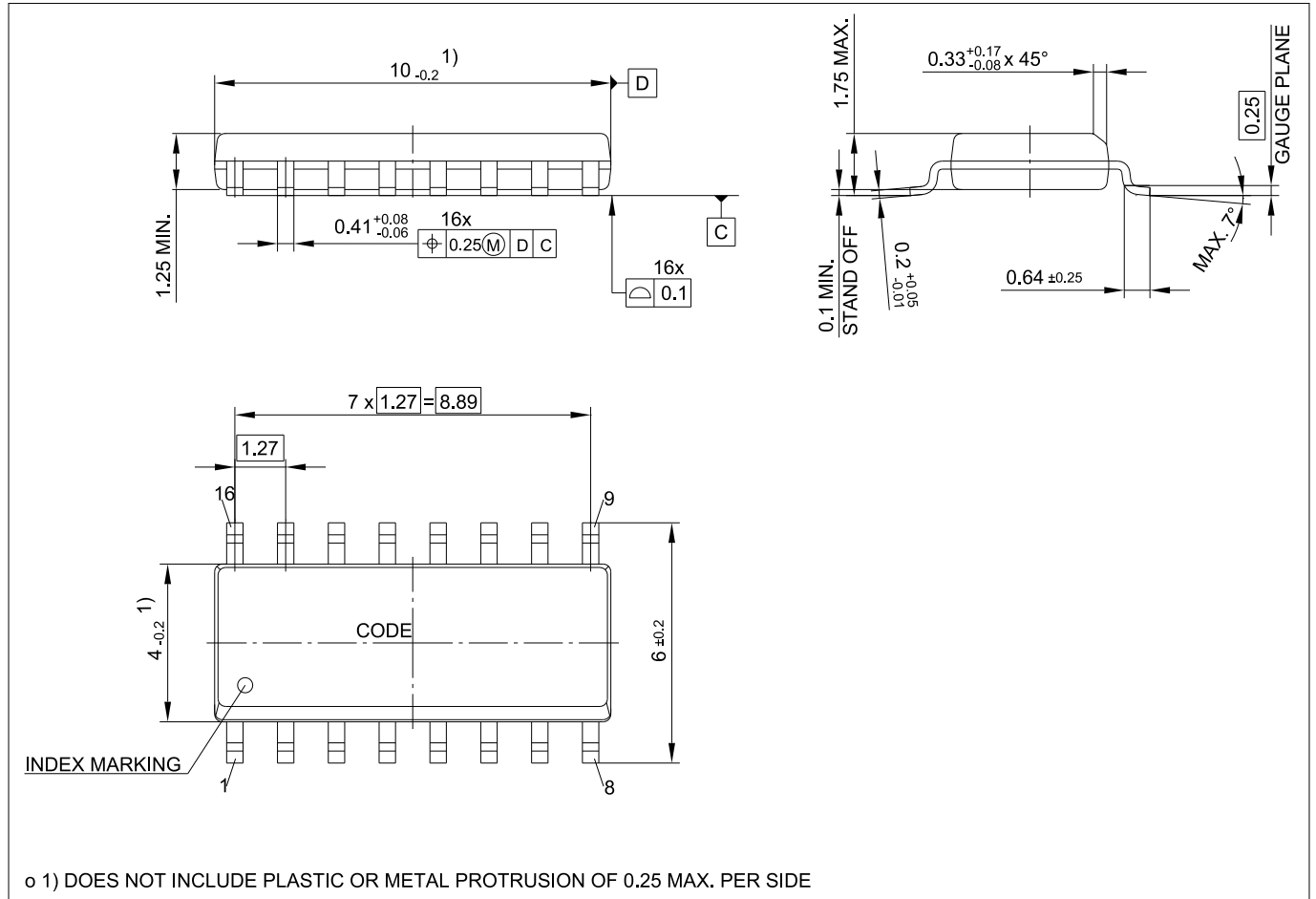
**Table 31 Electrical Characteristics of the Temperature Sensor**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Temperature sensor ADC output operating range	$ADC_{TEMP}$	0	—	190	LSB	$ADC_{TEMP} = 40 + \text{temperature} / ^\circ\text{C}$
Temperature sensor tolerance	$\Delta_{TEMP}$	—	—	$\pm 6$	K	Incl. ADC conversion accuracy at $3\sigma$

**Package Dimensions**

**6 Package Dimensions**

The package dimensions of PG-DSO-16 are provided.



**Figure 29 Package Dimensions for PG-DSO-16**

*Note: Dimensions in mm.*

*Note: You can find all of our packages, packing types and other package information on our Infineon Internet page “Products”: <http://www.infineon.com/products>.*

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## References

## 7 References

1. Infineon Technologies AG: *XDPL8220 Reference Board Test Report*
2. Infineon Technologies AG: *.dp Interface Gen2*: Can be ordered at <http://ehitex.com/programmer/486/.dp-interface-board-gen2>
3. Infineon Technologies AG: *.dp Vision User Manual*
4. Infineon Technologies AG: *.dp Interface Gen2 User Manual*
5. Infineon Technologies AG: *XDPL8220 Design Guide*
6. Infineon Technologies AG: *XDPL8220 Programming Manual*

## Abbreviations

### AC

*Alternating Current (AC)*

An Alternating Current is a form of power supply in which the flow of electric charge periodically reverses direction.

### ADC

*Analog-to-Digital Converter (ADC)*

An analog-to-digital converter is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

### BOM

*Bill of Materials (BOM)*

A bill of materials is a list of the raw materials, sub-assemblies, intermediate assemblies, sub-components, parts and the quantities of each needed to manufacture an end product.

### CC

*Constant Current (CC)*

Constant Current is a mode of a power supply in which the output current is kept constant regardless of the load.

### CCM

*Continuous Conduction Mode (CCM)*

Continuous Conduction Mode is an operational mode of a switching power supply in which the current is continuously flowing and does not return to zero.

### CRC

*Cyclic Redundancy Check (CRC)*

A cyclic redundancy check is an error-detecting code commonly used to detect accidental changes to raw data.

### CV

*Constant Voltage (CV)*

Constant Voltage is a mode of a power supply in which the output voltage is kept constant regardless of the load.

### DAC

*Digital-to-Analog Converter (DAC)*

A digital-to-analog converter is a device that converts digital data into an analog signal (typically voltage).

### DC

*Direct Current (DC)*

A Direct Current is a form of power supply in which the flow of electric charge is only into one direction.



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## Abbreviations

### **DCM**

*Discontinuous Conduction Mode (DCM)*

Discontinuous Conduction Mode is an operational mode of a switching power supply in which the current starts and returns to zero.

### **ECG**

*Electronic Control Gear (ECG)*

An electronic control gear is a power supply which provides one or more light module(s) with the appropriate voltage or current.

### **FB**

*Flyback (FB)*

A flyback converter is a power converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of galvanic isolation between the input and any outputs.

### **FW**

*Firmware (FW)*

A proprietary software exploiting a set of functions.

### **GUI**

*Graphic User Interface (GUI)*

A graphical user interface is a type of interface that allows users to interact with electronic devices through graphical icons and visual indicators.

### **HW**

*Hardware (HW)*

The collection of physical elements that comprise a computer system.

### **IC**

*Integrated Circuit (IC)*

A miniaturized electronic circuit that has been manufactured in the surface of a thin substrate of semiconductor material. An IC may also be referred to as micro-circuit, microchip, silicon chip, or chip.

### **IIR**

*Infinite Impulse Response (IIR)*

Infinite impulse response is a property applying to many linear time-invariant systems. Common examples of linear time-invariant systems are most electronic and digital filters. Systems with this property have an impulse response which does not become exactly zero past a certain point, but continues indefinitely.

### **LED**

*Light Emitting Diode (LED)*

A light-emitting diode is a two-lead semiconductor light source which emits light when activated.

### **LP**

*Limited Power (LP)*

Limited Power is a mode of a power supply in which the output power is limited regardless of the load.

### **NTC**

*Negative Temperature Coefficient Thermistor (NTC)*

A negative temperature coefficient thermistor is a type of resistor whose resistance declines over temperature.

### **OCP1**

*Overcurrent Protection Level 1 (OCP1)*

The Overcurrent Protection Level 1 is limiting the current in a switched-mode power supply to limit the power delivered to the output of the power supply.

---

## Abbreviations

### **OCP2**

*Overcurrent Protection Level 2 (OCP2)*

The Overcurrent Protection Level 2 is protecting the current in a switched-mode power supply from exceeding a maximum threshold.

### **OTP**

*One Time Programmable Memory (OTP)*

A One-Time Programmable memory is a form of memory to which data can be written once. After writing, the data is stored permanently and cannot be further changed.

### **PF**

*Power Factor (PF)*

Power factor is the ratio between the real power and the apparent power.

### **PFC**

*Power Factor Correction (PFC)*

Power factor correction increases the power factor of an AC power circuit closer to 1 which corresponds to minimizing the reactive power of the power circuit.

### **PSR**

*Primary Side Regulated (PSR)*

A Primary Side Regulated power supply is controlling its operation based on a property sensed on primary side of an isolated power supply.

### **PWM**

*Pulse Width Modulation (PWM)*

Pulse-width modulation is a technique to encode an analog value into the duty cycle of a pulsing signal with arbitrary amplitude.

### **QRM**

*Quasi-Resonant Mode (QRM)*

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by only switching at preferred times when switching losses are low.

### **QRM1**

*Quasi-Resonant Mode, switching in valley 1 (QRM1)*

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by switching at the occurrence of the first valley of a signal which corresponds to a time when switching losses are low.

### **QRMn**

*Quasi-Resonant Mode, switching in valley n (QRMn)*

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by switching at the occurrence of an nth valley of a signal which corresponds to a time when switching losses are low.

### **RAM**

*Random Access Memory (RAM)*

Random-access memory is a form of computer data storage which allows data items to be read and written regardless of the order in which data items are accessed.

### **THD**

*Total Harmonic Distortion (THD)*

The total harmonic distortion of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

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## Revision History

### UART

*Universal Asynchronous Receiver Transmitter (UART)*

A universal asynchronous receiver transmitter is used for serial communications over a peripheral device serial port by translating data between parallel and serial forms.

### USB

*Universal Serial Bus (USB)*

Universal Serial Bus is an industry standard that defines cables, connectors and communications protocols used in a bus for connection, communication, and power supply between computers and electronic devices.

### UVLO

*Undervoltage Lockout (UVLO)*

The Undervoltage-Lockout is an electronic circuit used to turn off the power of an electronic device in the event of the voltage dropping below the operational value.

## Revision History

Major changes since previous revision

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### Revision History

Revision	Description
1.0	<ul style="list-style-type: none"><li>Added the attention that the Vcc must be higher than 3.4V before any other pins exceeds 1.2V</li></ul>
0.7	<ul style="list-style-type: none"><li>Added a description of the input filter for the PWM sensing</li></ul>
0.6	<ul style="list-style-type: none"><li>Corrected for English language</li><li>Minor update of the PFC and FB content</li><li>Updated electrical characteristics</li></ul>

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## Edition 2016-11-4

**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

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**Email:** [erratum@infineon.com](mailto:erratum@infineon.com)

**Document reference**  
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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

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