

2:1 Active HDMI 1.3 Compatible Mux with Advanced Equalization for Enhanced Signal Integrity

Description

Features

- Supply voltage, $V_{DD} = 3.3V \pm 5\%$
- Compatible w/ DVI, HDMI 1.1, 1.2, and 1.3 signals
- HDMI revision 1.3 support up to 12-bits of color/channel (2.5Gbps)
- Supports both AC-coupled and DC-coupled inputs
- 2:1 Mux
- Configurable output swing control (500mV, 750mV, 1000mV)
- Configurable Pre-Emphasis levels (0dB, 1.5dB, 3.5dB, & 6.0dB)
- Configurable De-Emphasis (0dB, -1.5dB, -3.5dB, -6.0dB)
- Configurable Equalization (1dB, 3.5dB, 6dB, or optimal setting)
- Auto-Flex™ Equalization allws single setting for all cable length support, 1meter to 20meters
- Max Data Rate = 2.5Gbps
- ESD protection = 6kV (typical)
- Inputs w/ built in termination
- Proagation delay = < 2ns input
- Uni-Directional
- Packaging (Pb-free & Green): 56-pad TQFN (ZB56)

Pericom Semiconductor's PI3HDMI421AR 2:1 active mux circuit is targeted for high-resolution video networks that are based on DVI/HDMI standards, and TMDS signal processing. The PI3HDMI421AR is an active 2 TMDS to 1 TMDS mux receiver switch with Hi-Z outputs. The device receives differential signals from selected video components and drives the video display unit. It provides three controllable output swings that can be controlled through a single bit. The allowable output swings are 500mV, 750mV and 1000mV. This solution also provides a unique advanced pre-emphasis technique to increase rise and fall times which are reduced during transmission across long distances.

The maximum DVI/HDMI Bandwidth of 2.5Gbps provides 1920x1080 resolution with 12-bit/channel color depths required by the next Gen HDTV and PC graphics. For consumer video networks, the device sits at the receiver's side to switch between multiple video components. PI3HDMI421AR is the industry's first active DVI/HDMI switch compatible with HDMI rev. 1.3, which ensures transmitting high bandwidth video streams from video components to the display unit.

The Optimized Equalization provides the user a single optimal setting that can provide HDMI compliance for all cable lengths: 2meter, 10meter, 15meter, and 20 meter. Pericom also offers the ability to fine tune the equalization settings in situations where cable length is known.

Switch Block Diagram



Pin Configuration



Function Block Description



BYTE 1 (Address Assignment)

| Address | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---------|----|----|----|----|----|----|----|---------|
| Value | 1 | 1 | 0 | A3 | A2 | A1 | A0 | R=1/W=0 |

BYTE 2 (1st Data byte - Port A control and output control)

| Port A and Output Control | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | Result | | |
|---------------------------|----|----|----|----|----|----|----|----|------------------------|-------------------|------------------|
| | | | | | | | | | Swing (mV) | Pre-emphasis (dB) | De-emphasis (dB) |
| Swing Control | 0 | 0 | 0 | 0 | x | x | x | x | 500 | 0 | 0 |
| | 0 | 0 | 0 | 1 | x | x | x | x | 750 | 0 | 0 |
| | 0 | 0 | 1 | 0 | x | x | x | x | 1000 | 0 | 0 |
| | 0 | 0 | 1 | 1 | x | x | x | x | N/A | N/A | N/A |
| Pre-Emphasis | 0 | 1 | 0 | 0 | x | x | x | x | 500 | 0 | 0 |
| | 0 | 1 | 0 | 1 | x | x | x | x | 500 | 1.5 | 0 |
| | 0 | 1 | 1 | 0 | x | x | x | x | 500 | 3.5 | 0 |
| | 0 | 1 | 1 | 1 | x | x | x | x | 750 | 6.0 | 0 |
| De-Emphasis | 1 | 0 | 0 | 0 | x | x | x | x | 750 | 0 | 0 |
| | 1 | 0 | 0 | 1 | x | x | x | x | 750 | 0 | -1.5 |
| | 1 | 0 | 1 | 0 | x | x | x | x | 750 | 0 | -3.5 |
| | 1 | 0 | 1 | 1 | x | x | x | x | 750 | 0 | -6.0 |
| Output Port Select | x | x | x | x | x | x | 0 | 1 | Port A is active | | |
| | x | x | x | x | x | x | 1 | 1 | Port B is active | | |
| | x | x | x | x | x | x | x | 0 | I/O's = Hi-Z | | |
| Equalization (dB) | x | x | x | x | 0 | 0 | x | x | 1 | | |
| | x | x | x | x | 0 | 1 | x | x | 3.5 | | |
| | x | x | x | x | 1 | 0 | x | x | Optimized Equalization | | |
| | x | x | x | x | 1 | 1 | x | x | 8 | | |

BYTE 3 (2nd Data byte - Port B control)

| Port B Control | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | Result |
|-------------------|----|----|----|----|----|----|----|----|----------------------|
| Equalization (dB) | x | x | x | x | 0 | 0 | x | x | 1 |
| | x | x | x | x | 0 | 1 | x | x | 3.5 |
| | x | x | x | x | 1 | 0 | x | x | Optimized EQ Setting |
| | x | x | x | x | 1 | 1 | x | x | 8 |

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|---|--------------------------|
| Storage Temperature | -65°C to +150°C |
| Supply Voltage to Ground Potential..... | -0.5V to +5V |
| DC Input Voltage | -0.5V to V _{DD} |
| DC Output Current..... | 120mA |
| Power Dissipation | 1.0W |

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Description

| Pin # | Pin Name | Type | Description |
|--|------------------------------------|-------|---|
| 4, 10, 16, 29, 36, 42, 45, 54 | VDD | Power | 3.3V power supply |
| 1, 7, 13, 24, 32, 35, 39, 43, 44, 51 | GND | Power | 0V power supply |
| 22 | SCL | I | I ² C Clock input Signal if and only if, MS = 'HIGH' |
| 23 | SDA | I/O | I ² C Date Input/Output Signal if and only if, MS = 'HIGH' |
| 22, 23 | S3, S2 (PortB) | I | If MS = 'LOW', then pins 22 and 23 are control bits S2 and S3 for Port B only, as shown in the truth table on page 3. |
| 48 | SEL_IN | I | Control pin used to choose which input signal is active, Port A or Port B. If 'LOW', then Port A is active, if 'HIGH', then Port B is active. |
| 25, 26, 27, 28 | A0 - A3 | I | I ² C address inputs if and only if MS = 'HIGH'. |
| 25, 26, 27, 28 | S7, S6, S5, S4 | I | If MS = 'LOW', then pins 25-28 are control bits S7-S4, as shown in truth table on page 3 of datasheet |
| 50 | MS | I | Mode Select Pin. If MS = 'HIGH', then I2C control is active. Pins 25-28 are I ² C address and pin 22 is SCL and pin 23 is SDA. If MS = 'LOW', then I2C control is inactive and pin programmability is active. Pins 25-28 are control pins S7-S4 and pin 23 is S2 and pin 22 is S3. |
| 20, 21 | NC | N/A | No Connect. |
| 19 | SEL_OUT | O | Output bit, that provides information to user as to which port is active, if SEL_OUT = 'LOW', then Port A is active, if SEL_OUT = 'HIGH', then Port B is active. Only used when MS pin is 'HIGH' |
| 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18, 52, 53, 55, 56 | Dx ^y , CLK ^y | I | High Speed TMDS input signals |
| 30, 31, 33, 34, 37, 38, 40, 41 | Dx, CLK | O | High Speed TMDS output signals |
| 46, 47 | S2, S3 (Port A) | I | If MS = 'LOW', then pins 22 and 23 are control bits S2 and S3 for Port A only, as shown in the truth table on page 3. |
| 49 | OE | I | Output is enabled and normal when OE = 'HIGH'. If OE = 'LOW', output is disabled and at Hi-Z |

TMDS Compliance Test Results

| Item | HDMI 1.3 Spec | Pericom TMDS Product Spec |
|--|---|---|
| Operating Conditions | | |
| Termination Supply Voltage, A_{VDD} | $3.3V \leq 5\%$ | $3.30 \pm 5\%$ |
| Terminal Resistance | $50\text{-ohm} \pm 10\%$ | 45 to 55-ohm |
| Source DC Characteristics at TP1 | | |
| Single-ended high level output voltage, V_H | $A_{VDD} \pm 10mV$ | $A_{VDD} \pm 10mV$ |
| Single-ended low level output voltage, V_L | $(A_{VDD} - 600mV) \leq V_L \leq (A_{VDD} - 400mV)$ | $(A_{VDD} - 600mV) \leq V_L \leq (A_{VDD} - 400mV)$ |
| Single-ended output swing voltage, V_{swing} | $400mV \leq V_{swing} \leq 600mV$ | $400mV \leq V_{swing} \leq 600mV$ |
| Single-ended standby (off) output voltage, V_{off} | $A_{VDD} \pm 10mV$ | $A_{VDD} \pm 10mV$ |
| Single-ended standby (off) output current, I_{off} | $ I_{OFF} < 10\mu A$ | $ I_{OFF} < 10\mu A$ |
| Transmitter AC Characteristics at TP1 | | |
| Risetime/Falltime (20%-80%) | $75ps \leq \text{Risetime/Falltime} \leq 0.4 \text{ Tbit}$ ($75ps \leq tr/ft \leq 242ps$) @ 1.65Gbps | 240ps |
| Intra-Pair Skew at Transmitter Connector, max | 0.15 Tbit (90.9ps @ 1.65Gbps) | 60ps max |
| Inter-Pair Skew at Transmitter Connector, max | 0.2 Tpixel (1.2ns @ 1.65Gbps) | 100ps max |
| Clock Jitter, max | 0.25 Tbit (151.5ps @ 1.65Gbps) | 82ps max |
| Sink Operating DC Characteristics at TP2 | | |
| Input Differential Voltage Level, V_{diff} | $150 \leq V_{diff} \leq 1200mV$ | $150mV \leq V_{DIFF} \leq 1200mV$ |
| Input Common Mode Voltage Level, V_{ICM} | $(A_{VDD} - 300mV) \leq V_{icm} \leq (A_{VDD} - 37.5mV)$ Or $A_{VDD} \pm 10\%$ | $(A_{VDD} - 300mV) \leq V_{icm} \leq (A_{VDD} - 37.5mV)$ Or $A_{VDD} \pm 10\%$ |
| Sink DC Characteristics When Source Disabled or Disconnected at TP2 | | |
| Differential Voltage Level | $A_{VDD} \pm 10mV$ | $A_{VDD} \pm 10mV$ |

DC Electrical Characteristics^(2,3) ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted. $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

| Symbol | Parameter | Test Condition ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units |
|--------------------|----------------------------------|-------------------------------|------------------------|---------------------|-------------------------|-------|
| V_{idiff} | Input Differential Voltage Level | | 150 | | 1200 | mVp-p |
| V_{icm} | Input Common Mode Voltage | | 1.8 | | $V_{DD} + 10\%$ | V |
| V_{diff} | Differential Voltage Level | | $V_{DD} - 10\text{mV}$ | V_{DD} | $V_{DD} + 10\text{mV}$ | V |
| V_{OS} | Offset Voltage | | | | $V_{DD} - 250\text{mV}$ | V |
| V_{IH} | Minimum Input High Voltage | | 1.8 | | | V |
| V_{IL} | Minimum Input Low Voltage | | | | 0.8 | V |
| I_{CC} | Power Supply Current | | | | 282 | mA |

AC Electrical Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units |
|-------------------|---|--------------------------------|------|---------------------|------|---------------|
| V_{SEN} | Differential Sensitivity (peak-to-peak) | | 150 | | | mVp-p |
| V_{IN} | Differential Input (peak-to-peak) | | | | 1560 | mVp-p |
| | Allowable Intra-Pair Skew at Sink Connector | | | | 50 | ps |
| | Allowable Inter-Pair Skew at Sink Connector | | | | 100 | ps |
| | TMDS Clock Jitter | | | 50 | | ps |
| T_{20-80} | TDR Rise Time | | | | 200 | ps |
| | Through connection impedance | | 85 | 100 | 115 | Ω |
| | At Termination Impedance | | 90 | 100 | 110 | Ω |
| t_{PHLD} | Differential Propagation Delay High to Low | | | 1 | | ns |
| t_{PLHD} | Differential Propagation Delay Low to High | | | 1 | | ns |
| t_{SKD} | Differential Skew $t_{\text{PHLD}} - t_{\text{PLHD}}$ | | | 25 | | ps |
| t_{PHZ} | Disable Time High to Z | | | 5 | | ns |
| t_{PLZ} | Disable Time Low to Z | | | 5 | | |
| t_{PZH} | Enable Time Z to High | | | 1 | | μs |
| t_{PZL} | Enable Time Z to Low | | | 1 | | |

Power Supply Characteristics

| Parameters | Description | Test Conditions ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units |
|------------------|--------------------------------|--|------|---------------------|------|-------|
| I_{CCQ} | Quiescent Power Supply Current | $V_{DD} = \text{Max.}, V_{\text{IN}} = V_{DD}, \text{OE} = \text{'LOW'}$ | | 1 | | mA |

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{DD} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$ ambient and maximum loading.

Normalized Eye Diagram Mask at TP1 for Source Requirements

Absolute Eye Diagram Mask at TP2 for Sink Requirements


Application Information - Recommended layout for 2 HDMI Input System


Application Information

PI3HDMI421AR can be used to re-drive HDMI or DVI signals across internal cables or long FR4 trace lengths.

If a DTV is designed with a side/front HDMI connector, a separate daughter card is needed for the side/front HDMI connector and Pericom re-driver.

ATC compliance **MUST** only be maintained from the front/side connector to the PI3HDMI421AR IC. After the PI3HDMI421AR signal integrity will be taken care of through the powerful pre-emphasis technique of the Pericom solution.

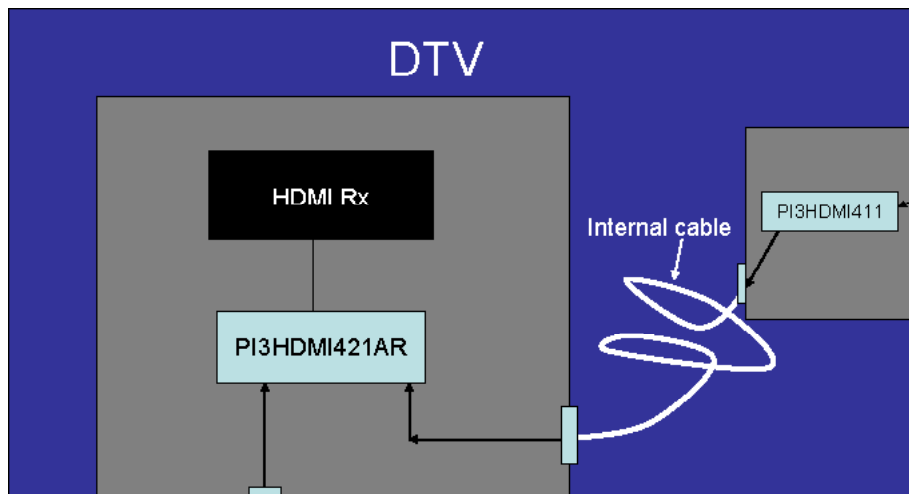


Figure 1: DTV with 2 HDMI connectors (1 HDMI in back & 1 HDMI on the side)



Figure 2: Signal integrity analysis test setup



Figure 3: 8bit deep color DVI/HDMI TX eye tested with 2 meter. 30 AWG HDMI cable. Setting: Optimized equalization, 0dB output pre-emphasis and de-emphasis, and Swing 500mV.



Figure 4: 8bit deep color DVI/HDMI TX eye tested with 10 meter. 24 AWG HDMI cable. Setting: Optimized equalization, 0dB output pre-emphasis and de-emphasis, and Swing 500mV.



Figure 5: 8bit deep color DVI/HDMI TX eye tested with 20 meter. 24 AWG HDMI cable. Setting: Optimized equalization, 0dB output pre-emphasis and de-emphasis, and Swing 500mV.

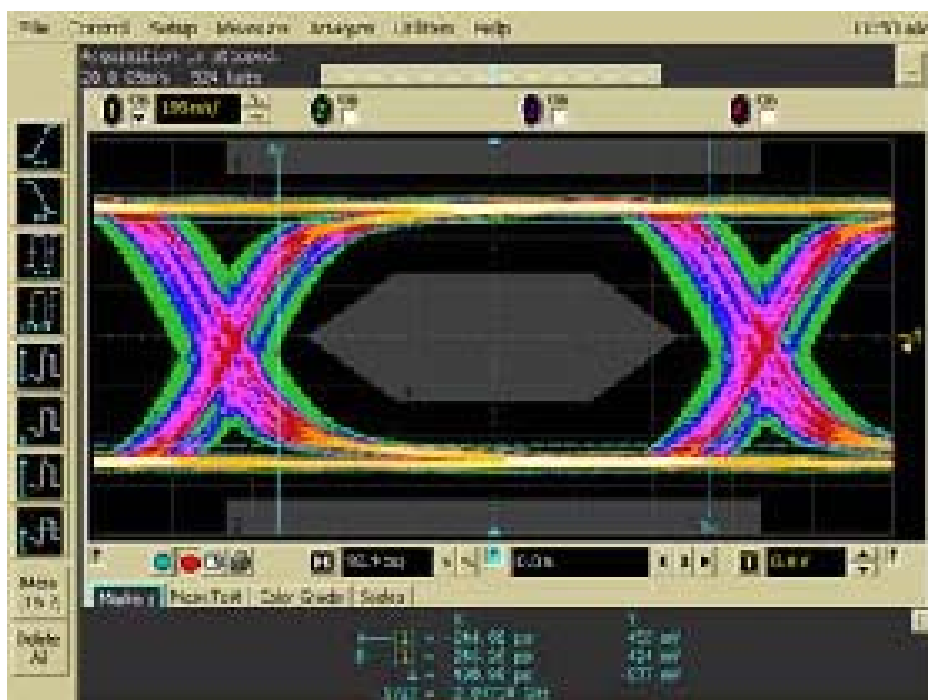


Figure 6: 8bit deep color DVI/HDMI TX eye tested with 25 meter. 24 AWG HDMI cable. Setting: Optimized equalization, 0dB output pre-emphasis and de-emphasis, and Swing 500mV.



Figure 7: 12bit deep color DVI/HDMI TX eye tested with 1 meter. 30 AWG HDMI cable. Setting: Optimized equalization, 0dB output pre-emphasis and de-emphasis, and Swing 500mV.



Figure 8: 12bit deep color DVI/HDMI TX eye tested with 20 meter. 24 AWG HDMI cable. Setting: Optimized equalization, 0dB output pre-emphasis and de-emphasis, and Swing 500mV.



Ordering Information

| Ordering Code | Package Code | Package Description |
|-----------------|--------------|------------------------------|
| PI3HDMI421ARZBE | ZB | 56-pin, Pb-free & Green TQFN |

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel

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