

LM5114 Single 7.6A Peak Current Low-Side Gate Driver

Check for Samples: [LM5114](#)

FEATURES

- Independent Source and Sink Outputs for Controllable Rise and Fall Times
- +4V to +12.6V Single Power Supply
- 7.6A/1.3A Peak Sink/Source Drive Current
- 0.23Ω Open-drain Pull-down Sink Output
- 2Ω Open-drain Pull-up Source Output
- 12ns (Typical) Propagation Delay
- Matching Delay Time Between Inverting and Non-inverting Inputs
- TTL/CMOS Logic Inputs
- 0.68V Input Hysteresis
- Up to +14V Logic Inputs (Regardless of VDD Voltage)
- Low Input Capacitance: 2.5pF (Typical)
- -40°C to +125°C Operating Temperature Range
- Pin-to-Pin Compatible with MAX5048

APPLICATIONS

- Boost Converters
- Flyback and Forward Converters
- Secondary Synchronous FETs Drive in Isolated Topologies
- Motor Control

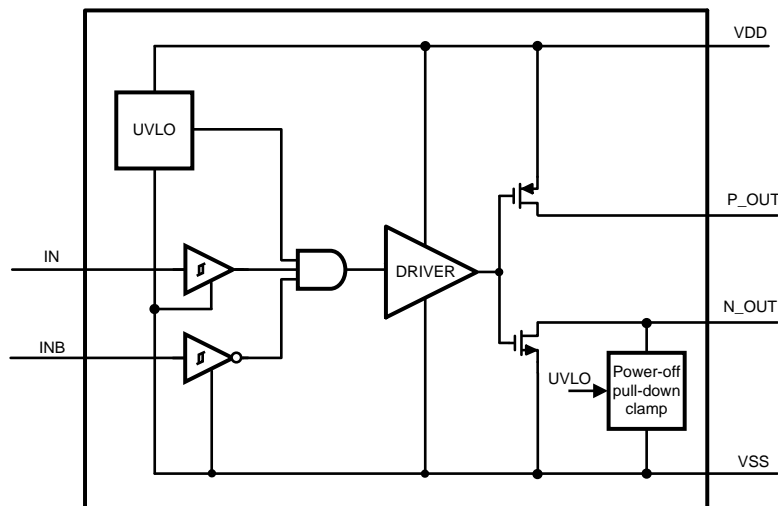
DESCRIPTION

The LM5114 is designed to drive low-side MOSFETs in boost type configurations or to drive secondary synchronous MOSFETs in isolated topologies. With strong sink current capability, the LM5114 can drive multiple FETs in parallel. The LM5114 also has the features necessary to drive low-side enhancement mode Gallium Nitride (GaN) FETs. The LM5114 provides inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive in a single device type. The inputs of the LM5114 are TTL/CMOS Logic compatible and withstand the input voltages up to 14V regardless of the VDD voltage. The LM5114 has split gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently. The LM5114 has fast switching speed and minimized propagation delays, facilitating high-frequency operation. The LM5114 is available in SOT-23 6-pin package and WQFN-6 package with an exposed pad to aid thermal dissipation.

PACKAGES

- SOT-23-6
- WQFN-6 (3mm x 3mm)

Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012–2013, Texas Instruments Incorporated

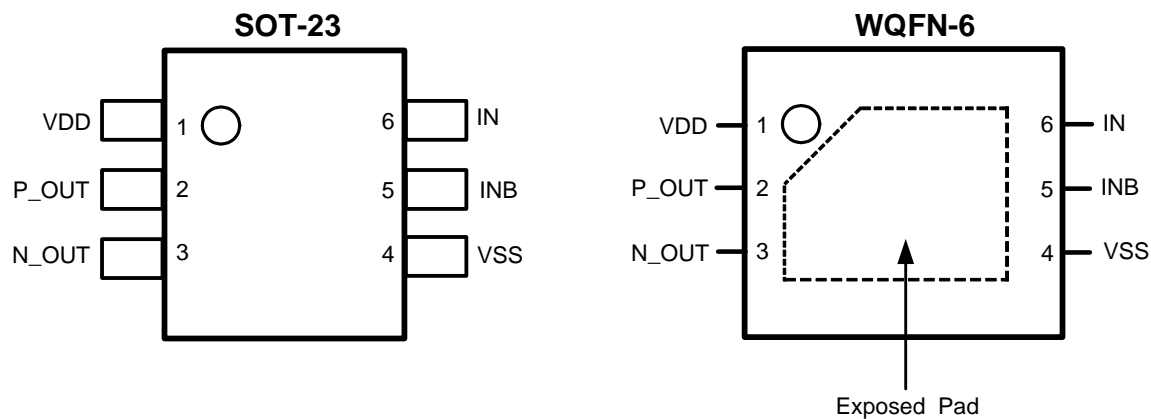
Input Options

Base Part Number	Input Thresholds
LM5114A	CMOS
LM5114B	TTL

Truth Table

IN	INB	P_OUT	N_OUT
L	L	OPEN	L
L	H	OPEN	L
H	L	H	OPEN
H	H	OPEN	L

Connection Diagram



PIN DESCRIPTIONS

Pin No.		Name	Description	Applications Information
SOT-23-6	WQFN-6			
1	1	VDD	Gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor located as close as possible to the IC.
2	2	P_OUT	Source-current output	Connect to the gate of the MOSFET with a short, low inductance path. A gate resistor can be used to adjust the turn-on speed.
3	3	N_OUT	Sink-current output	Connect to the gate of the MOSFET with a short, low inductance path. A gate resistor can be used to adjust the turn-off speed.
4	4	VSS	Ground	All signals are referenced to this ground.
5	5	INB	Inverting logic input	Connect to VSS when not used.
6	6	IN	Non-inverting logic input	Connect to VDD when not used.
	EP	It is recommended that the exposed pad on the bottom of the package is soldered to ground plane on the PC board to aid thermal dissipation.		



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

VDD to VSS	–0.3 to 14V
IN, INB to VSS	–0.3 to 14V
N_OUT to VSS	–0.3 to VDD +0.3V
P_OUT to VSS	–0.3 to VDD +0.3V
Junction Temperature	+150°C
Storage Temperature Range	–55 to +150°C
ESD Rating HBM	2kV

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the [Electrical Characteristics](#).

Recommended Operating Conditions

VDD	+4.0 to 12.6V
Junction Temperature	–40 to +125°C

Electrical Characteristics

Limits in standard type are for $T_J = 25^\circ\text{C}$ only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to $+125^\circ\text{C}$. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise specified, $V_{DD} = +12\text{V}$ ⁽¹⁾.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{DD}	VDD Operating Voltage		4.0		12.6	V
UVLO	VDD Undervoltage Lockout	VDD Rising	3.25	3.6	4.00	V
	VDD Undervoltage Lockout Hysteresis			0.4		V
	VDD Undervoltage lockout to Output delay time	VDD Rising		300		ns
I_{DD}	VDD Quiescent Current	IN = INB = VDD		0.95	1.9	mA

- (1) Min and Max limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Limits in standard type are for $T_J = 25^\circ\text{C}$ only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to $+125^\circ\text{C}$. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise specified, $V_{DD} = +12\text{V}$ ⁽¹⁾.

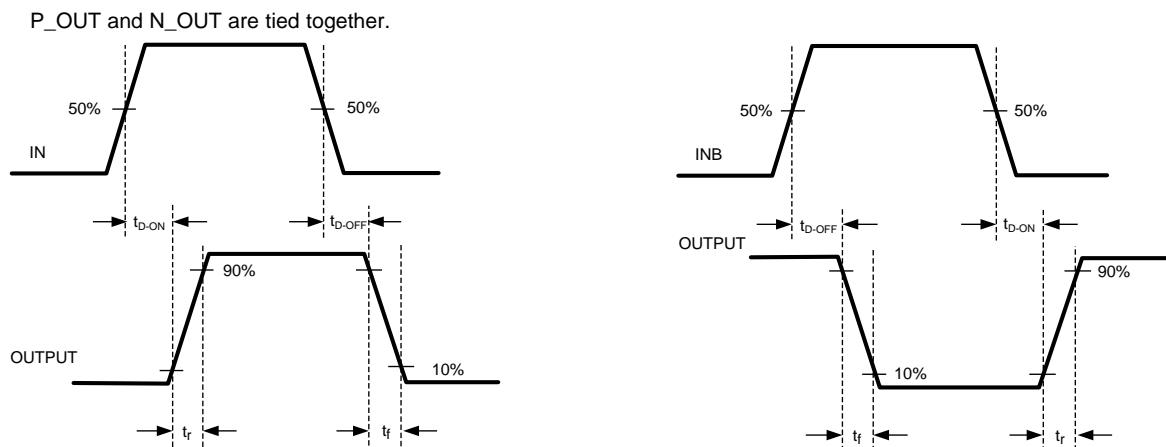
Symbol	Parameter	Conditions		Min	Typ	Max	Units
N-CHANNEL OUTPUT							
R _{ON-N} (SOT-23-6)	Driver Output Resistance – Pulling Down	VDD = 10V, I _{N-OUT} = -100mA	T _J = +25°C		0.23	0.26	Ω
			T _J = +125°C		0.38	0.43	Ω
		VDD = 4.5V, I _{N-OUT} = -100mA	T _J = +25°C		0.24	0.28	Ω
			T _J = +125°C		0.40	0.47	Ω
R _{ON-N} (WQFN-6)	Driver Output Resistance – Pulling Down	VDD = 10V, I _{N-OUT} = -100mA	T _J = +25°C		0.31	0.34	Ω
			T _J = +125°C		0.46	0.51	Ω
		VDD = 4.5V, I _{N-OUT} = -100mA	T _J = +25°C		0.32	0.36	Ω
			T _J = +125°C		0.48	0.55	Ω
	Power-off Pull Down Resistance	VDD = 0V, I _{N-OUT} = -10mA			3.3	10	Ω
	Power-off Pull Down Clamp Voltage	VDD = 0V, I _{N-OUT} = -10mA			0.85	1.0	V
I _{LK-N}	Output Leakage Current	N_OUT = VDD			6.85	20	μA
I _{PK-N}	Peak Sink Current	C _L = 10,000pF			7.6		A
P-CHANNEL OUTPUT							
R _{ON-P} (SOT-23-6)	Driver Output Resistance – Pulling Up	VDD = 10V, I _{P-OUT} = 50mA	T _J = +25°C		2.00	3.00	Ω
			T _J = +125°C		2.85	4.30	Ω
		VDD = 4.5V, I _{P-OUT} = 50mA	T _J = +25°C		2.20	3.30	Ω
			T _J = +125°C		3.10	4.70	Ω
R _{ON-P} (WQFN-6)	Driver Output Resistance – Pulling Up	VDD = 10V, I _{P-OUT} = 50mA	T _J = +25°C		2.08	3.08	Ω
			T _J = +125°C		2.93	4.38	Ω
		VDD = 4.5V, I _{P-OUT} = 50mA	T _J = +25°C		2.28	3.38	Ω
			T _J = +125°C		3.18	4.78	Ω
I _{LK-P}	Output Leakage Current	P_OUT = 0			0.001	10	uA
I _{PK-P}	Peak Source Current	CL = 10,000pF			1.3		A
LOGIC INPUT							
V _{IH}	Logic 1 Input Voltage	LM5114A		0.67X VDD			V
		LM5114B		2.4			V
V _{IL}	Logic 0 Input Voltage	LM5114A				0.33X VDD	V
		LM5114B				0.8	V
V _{HYS}	Logic-Input Hysteresis	LM5114A			1.6		V
		LM5114B			0.68		V
	Logic-Input Current	INB = VDD or 0			0.001	10	uA
C _{IN}	Input Capacitance				2.5		pF
THERMAL RESISTANCE							
θ _{JA}	Junction to Ambient	SOT-23-6			90		°C/W
		WQFN-6			60		°C/W
SWITCHING CHARACTERISTICS FOR VDD = +10V							
t _R	Rise Time	C _L = 1000pF			8		ns
		C _L = 5000pF			45		ns
		C _L = 10,000pF			82		ns

Electrical Characteristics (continued)

Limits in standard type are for $T_J = 25^\circ\text{C}$ only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to $+125^\circ\text{C}$. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise specified, $V_{DD} = +12\text{V}$ ⁽¹⁾.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t _F	Fall Time	C _L = 1000pF			3.2		ns
		C _L = 5000pF			7.5		ns
		C _L = 10,000pF			12.5		ns
t _{D-ON}	Turn-On Propagation Delay	C _L = 1000pF	LM5114A	5	12	30	ns
			LM5114B	6	12	25	ns
t _{D-OFF}	Turn-Off Propagation Delay	C _L = 1000pF	LM5114A	5	12	30	ns
			LM5114B	6	12	25	ns
	Break-before-make Time					2.5	
SWITCHING CHARACTERISTICS FOR VDD = +4.5V							
t _R	Rise Time	C _L = 1000pF			12		ns
		C _L = 5000pF			41		ns
		C _L = 10,000pF			74		ns
t _F	Fall Time	C _L = 1000pF			3.0		ns
		C _L = 5000pF			7.0		ns
		C _L = 10,000pF			11.3		ns
t _{D-ON}	Turn-On Propagation Delay	C _L = 1000pF	LM5114A	5	17	36	ns
			LM5114B	8	14	27	ns
t _{D-OFF}	Turn-Off Propagation Delay	C _L = 1000pF	LM5114A	5	17	36	ns
			LM5114B	8	14	27	ns
	Break-Before-Make Time					4.2	

TIMING DIAGRAM



Typical Performance Characteristics

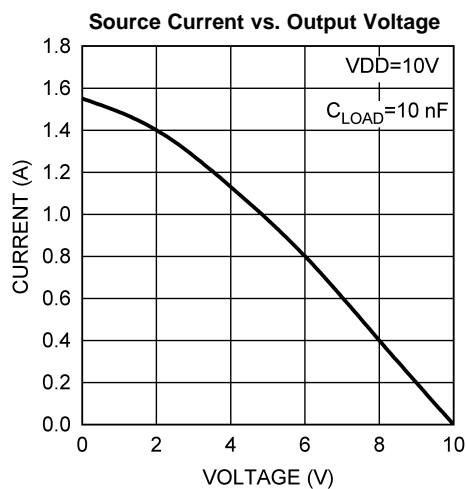


Figure 1.

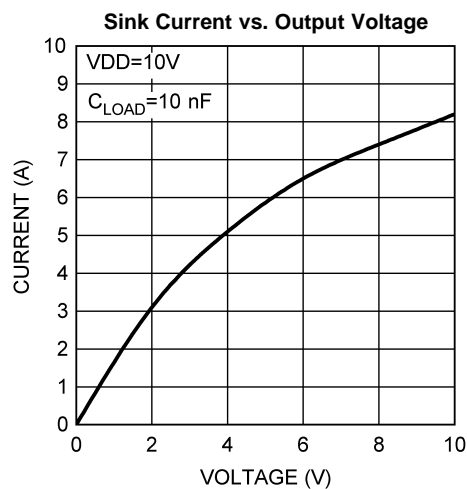


Figure 2.

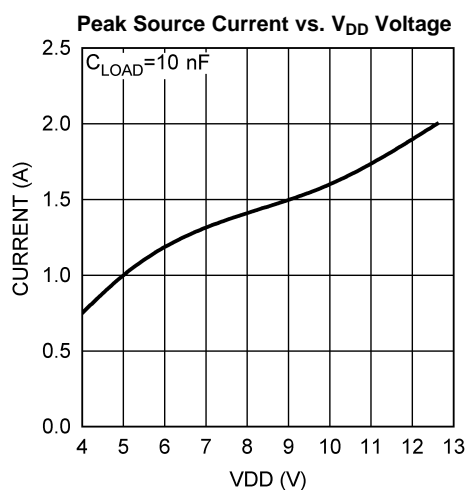


Figure 3.

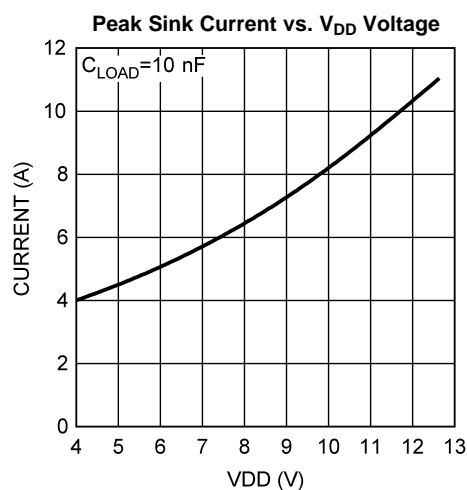


Figure 4.

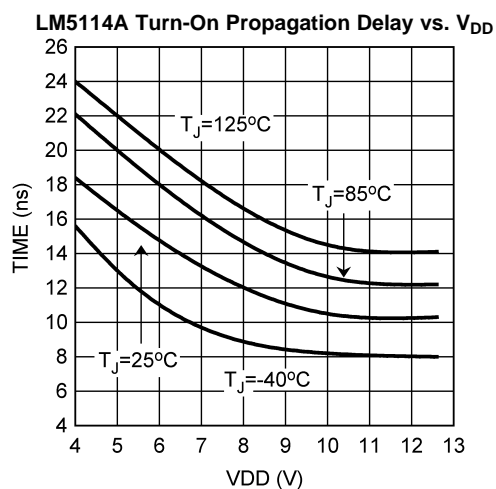


Figure 5.

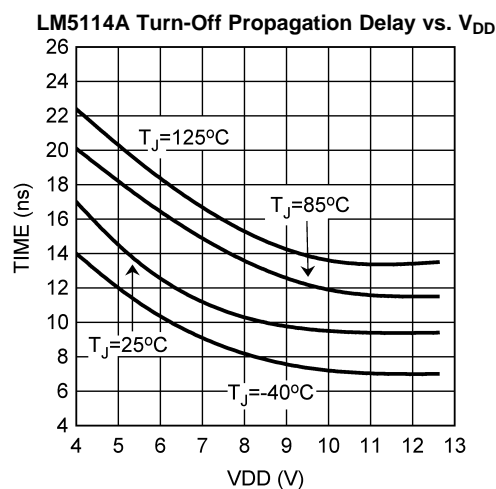


Figure 6.

Typical Performance Characteristics (continued)

LM5114B Turn-On Propagation Delay vs. V_{DD}

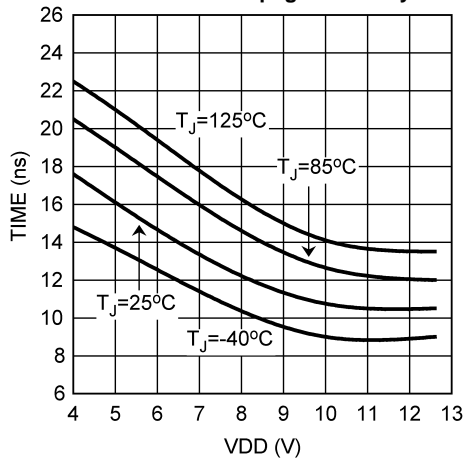


Figure 7.

LM5114B Turn-Off Propagation Delay vs. V_{DD}

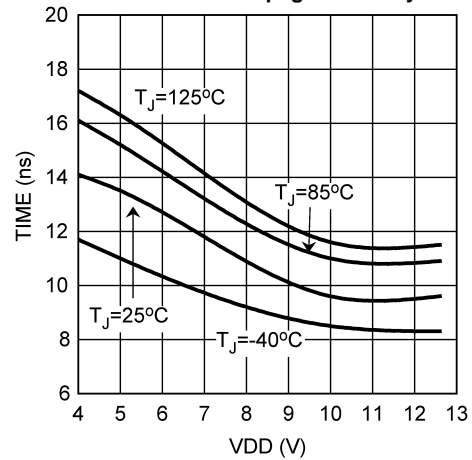


Figure 8.

UVLO Threshold vs. Temperature

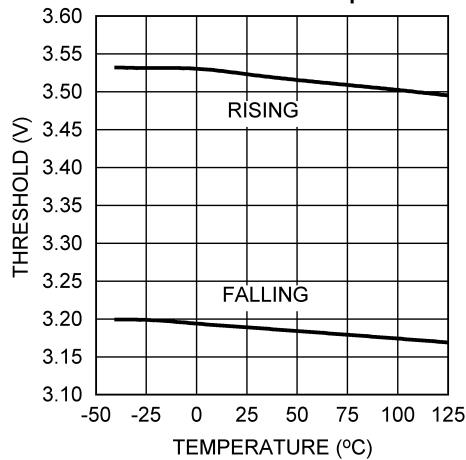


Figure 9.

Quiescent Current vs. Temperature

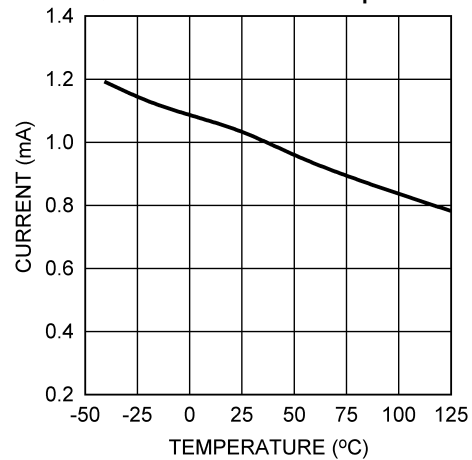


Figure 10.

Supply Current vs. Frequency

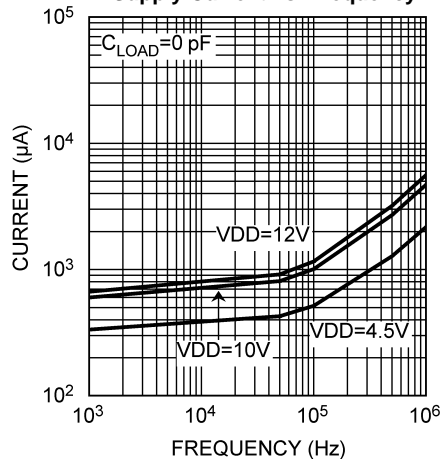


Figure 11.

Supply Current vs. Capacitive Load

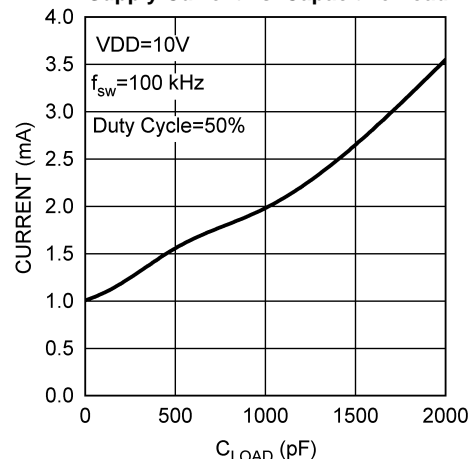


Figure 12.

Typical Performance Characteristics (continued)

Input Voltage vs. Output Voltage ($V_{DD} = 4V$, $C_L = 5000pF$)

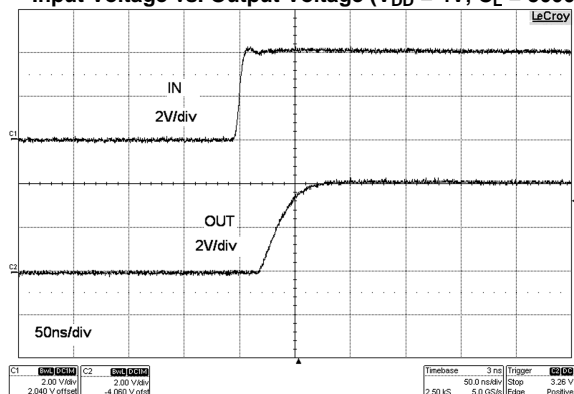


Figure 13.

Input Voltage
vs.
Output Voltage
($V_{DD} = 4V$, $C_L = 5000pF$)

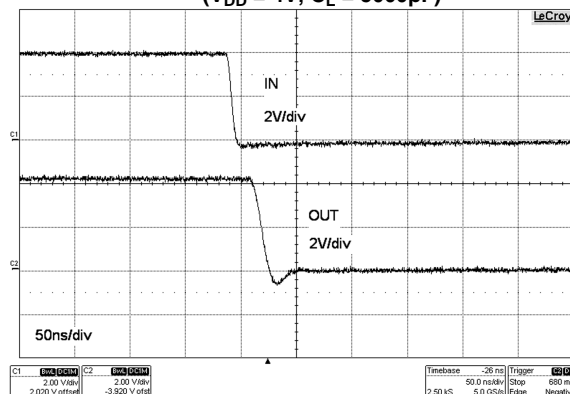


Figure 14.

Input Voltage
vs.
Output Voltage
($V_{DD} = 12V$, $C_L = 5000pF$)

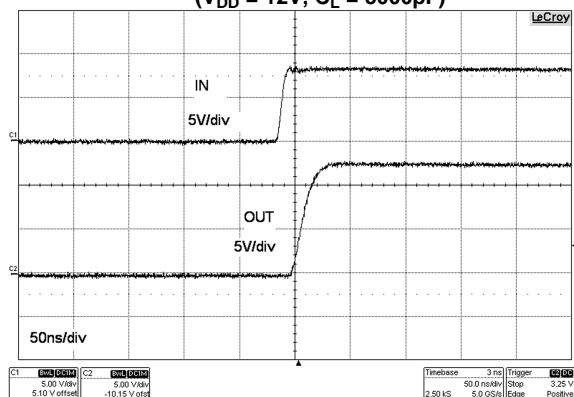


Figure 15.

Input Voltage
vs.
Output Voltage
($V_{DD} = 12V$, $C_L = 5000pF$)

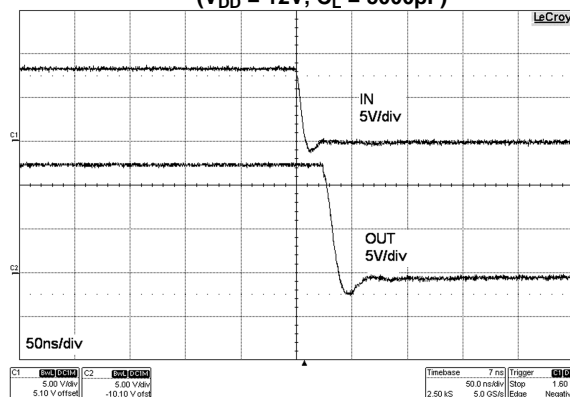


Figure 16.

Input Voltage
vs.
Output Voltage
($V_{DD} = 4V$, $C_L = 10000pF$)

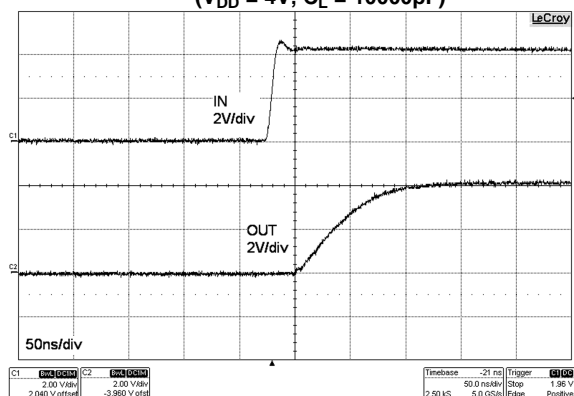


Figure 17.

Input Voltage
vs.
Output Voltage
($V_{DD} = 4V$, $C_L = 10000pF$)

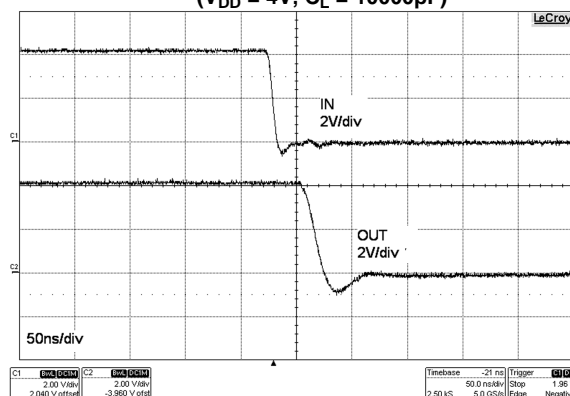


Figure 18.

Typical Performance Characteristics (continued)

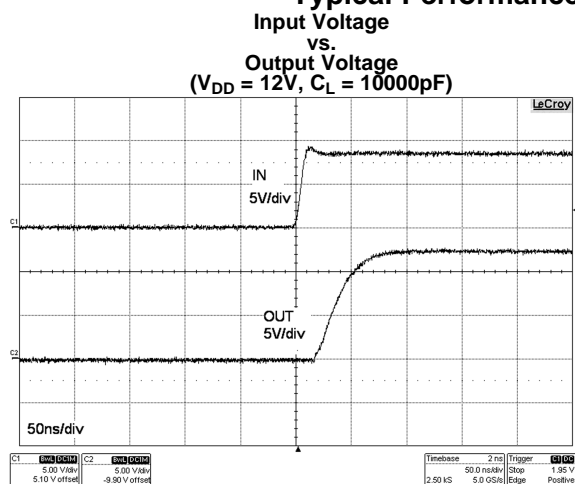


Figure 19.

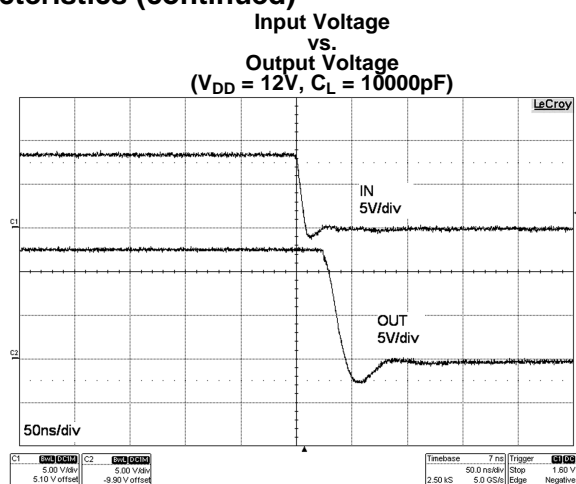


Figure 20.

TYPICAL APPLICATIONS

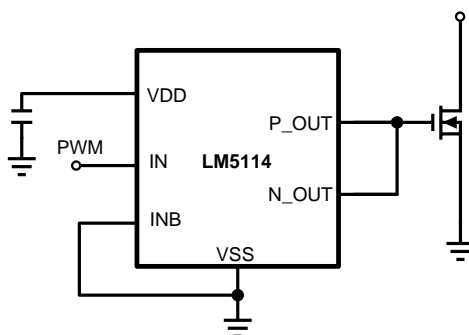


Figure 21. Non-inverting Application

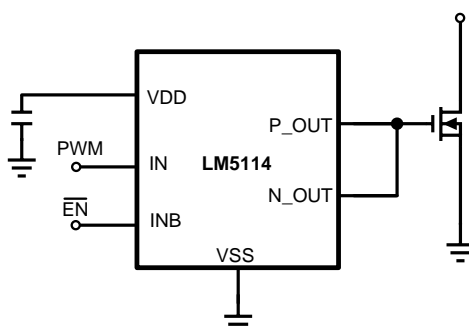


Figure 22. Non-Inverting Application with Enable Pin

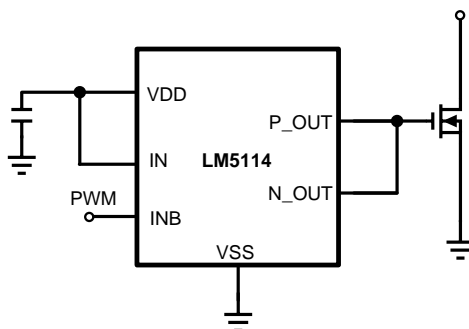


Figure 23. Inverting Application

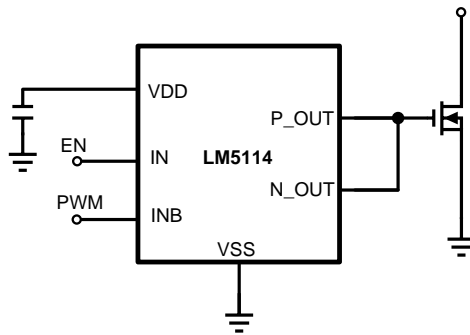


Figure 24. Inverting Application with Enable Pin

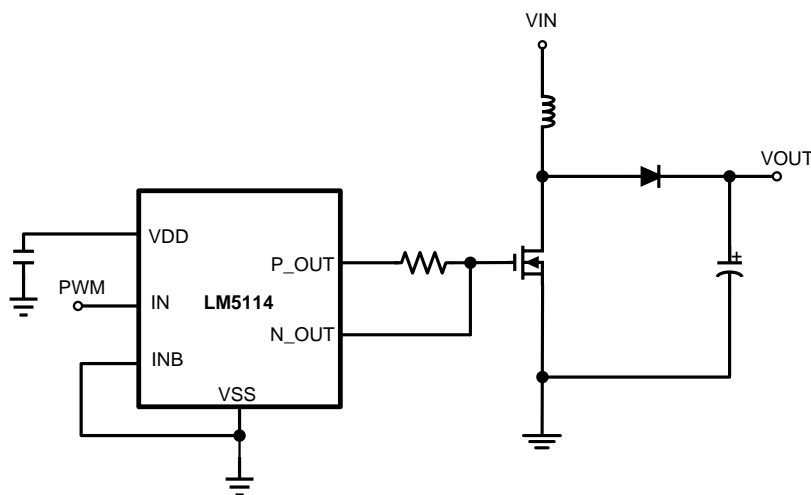


Figure 25. A Simplified Boost Converter

Detailed Operating Description

The LM5114 is designed to drive low-side MOSFETs in boost type configurations or to drive secondary synchronous MOSFETs in isolated topologies. The LM5114 offers both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive in a single device type. Inputs of the LM5114 are TTL Logic compatible and can withstand the input voltages up to 14V regardless of the VDD voltage. This allows inputs of the LM5114 to be connected directly to most PWM controllers. The split outputs of the LM5114 offer flexibility to adjust the turn-on and turn-off speed independently by adding additional impedance in either the turn-on path and/or the turn-off path.

The LM5114 includes an under-voltage lockout (UVLO) circuit. When the VDD voltage is below the UVLO threshold voltage, the IN and INB inputs are ignored, and if there is sufficient VDD voltage, the output NMOS is turned on to pull the N_OUT low. In addition, the LM5114 has an internal PNP transistor in parallel with the output NMOS. Under the UVLO condition, the PNP transistor will be on and clamp the N_OUT voltage below 1V. This feature ensures the N_OUT remaining low when VDD voltage is not sufficient to enhance the output NMOS.

The LM5114 has the features necessary to drive low-side enhancement mode GaN FETs. Due to the fast switching speed and relatively low gate voltage of enhancement mode GaN FETs, PCB layout is crucial to achieve reliable operation. Refer to [Layout Considerations](#) for details.

Power Dissipation

It is important to keep the power consumption of the driver below the maximum power dissipation limit of the package at the operating temperature. The total power dissipation of the LM5114 is the sum of the gate charge losses and the losses in the driver due to the internal CMOS stages used to buffer the output as well as the power losses associated with the quiescent current.

The gate charge losses can be calculated with the total input gate charge as follows.

$$P_g = Q_g \times V_{DD} \times F_{sw} \quad (1)$$

Or

$$P_g = C_{LOAD} \times V_{DD}^2 \times F_{sw} \quad (2)$$

Where F_{sw} is switching frequency.

The power dissipation associated with the internal circuit operation of the driver can be estimated with the characterization curves of the LM5114. For a given ambient temperature, the maximum allowable power loss of the IC can be defined as

$$P = \frac{(T_J - T_A)}{\theta_{JA}} \quad (3)$$

Where P is the total power dissipation of the driver.

Layout Considerations

Attention must be given to board layout when using LM5114. Some important considerations include:

1. The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the FETs gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate.
2. To reduce the loop inductance, the driver should be placed as close as possible to the FETs. The gate trace to and from the FETs are recommended to be placed closely side by side, or directly on top of one another.
3. A low ESR/ESL ceramic capacitor must be connected close to the IC, between VDD and VSS pins to support the high peak current being drawn from VDD during turn-on of the FETs. It is most desirable to place the VDD decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.
4. The parasitic source inductance, along with the gate capacitor and the driver pull-down path, can form a LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5114AMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SL2A	Samples
LM5114AMF/S7003109	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SL2A	Samples
LM5114AMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SL2A	Samples
LM5114AMFX/S7003103	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SL2A	Samples
LM5114ASD/NOPB	ACTIVE	WSO	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5114A	Samples
LM5114ASDX/NOPB	ACTIVE	WSO	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5114A	Samples
LM5114BMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SJ4B	Samples
LM5114BMF/S7003094	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SJ4B	Samples
LM5114BMF/S7003110	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SJ4B	Samples
LM5114BMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SJ4B	Samples
LM5114BMFX/S7003094	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SJ4B	Samples
LM5114BSD/NOPB	ACTIVE	WSO	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5114B	Samples
LM5114BSDX/NOPB	ACTIVE	WSO	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5114B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5114AMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5114AMF/S7003109	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q2
LM5114AMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5114AMFX/S7003103	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q2
LM5114ASD/NOPB	WSO	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5114ASDX/NOPB	WSO	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5114BMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5114BMF/S7003110	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q2
LM5114BMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5114BMFX/S7003094	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q2
LM5114BSD/NOPB	WSO	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5114BSDX/NOPB	WSO	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

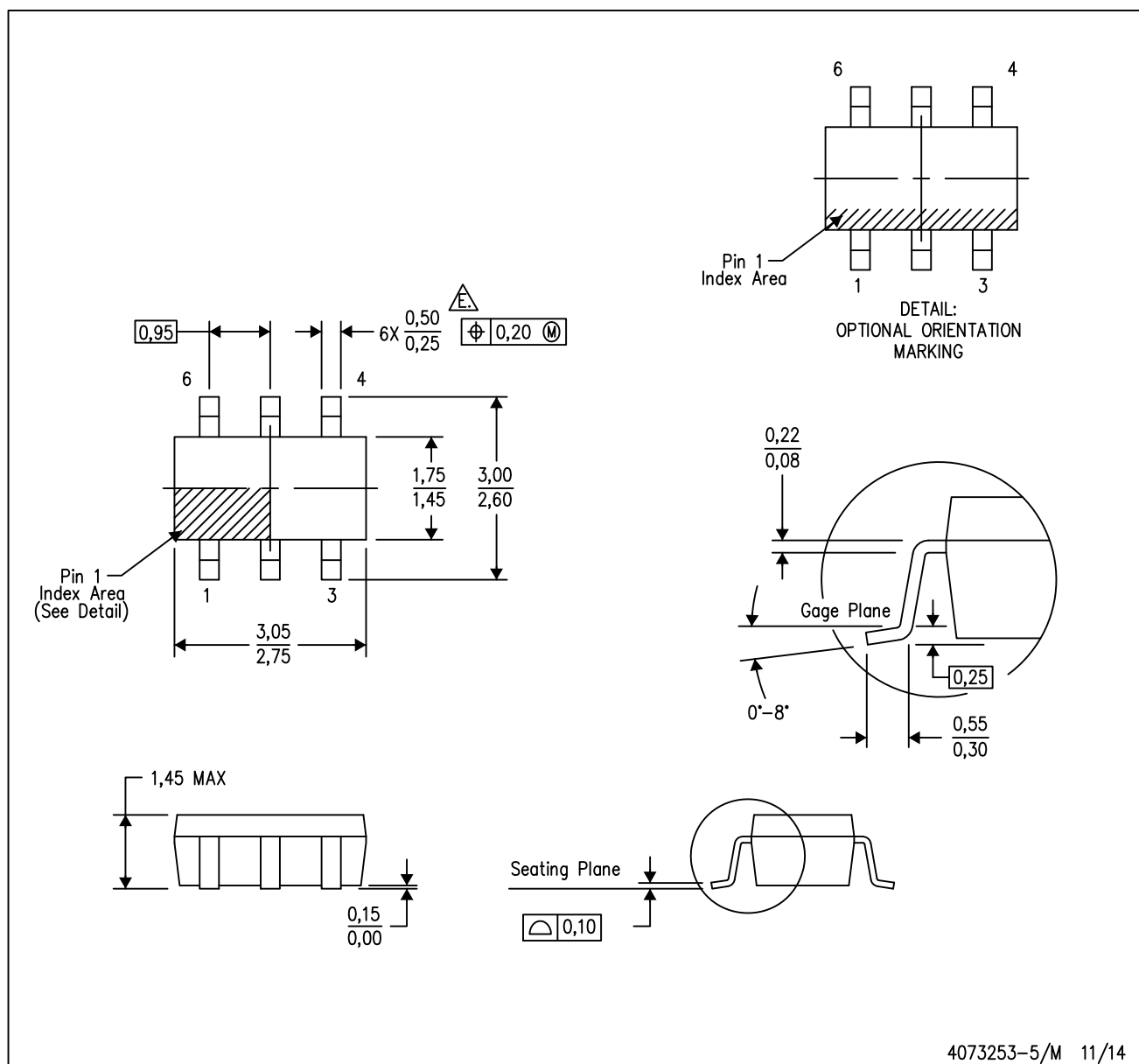


*All dimensions are nominal

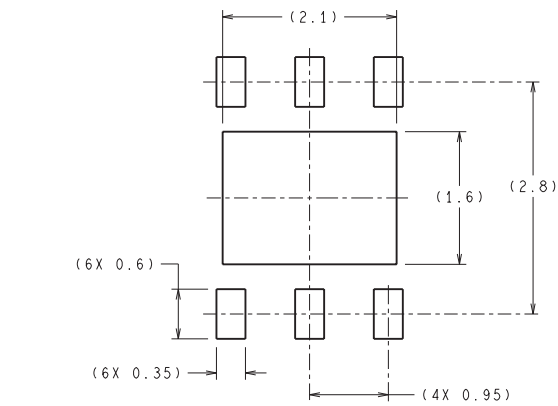
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5114AMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM5114AMF/S7003109	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM5114AMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM5114AMFX/S7003103	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM5114ASD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM5114ASDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LM5114BMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM5114BMF/S7003110	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM5114BMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM5114BMFX/S7003094	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM5114BSD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM5114BSDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

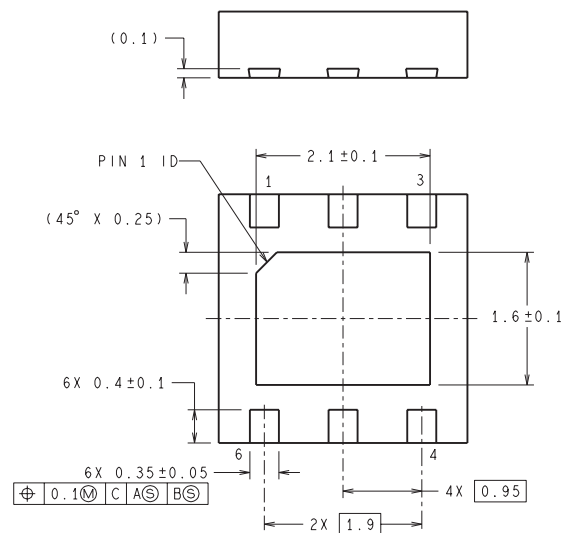
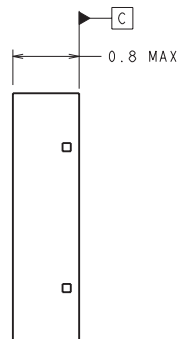
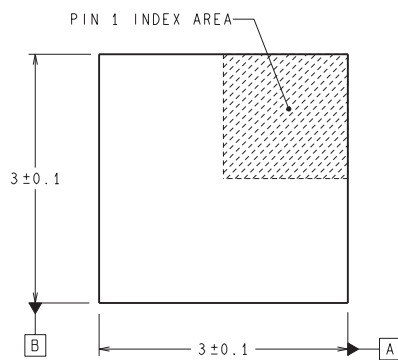


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 - Δ Falls within JEDEC MO-178 Variation AB, except minimum lead width.



DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN () FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN



SDE06A (Rev A)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9