# HCPL-270L/070L/273L/073L

## Low Input Current, High Gain, LVTTL/LVCMOS Compatible Optocouplers

AVAGO TECHNOLOGIES

## Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

### Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in LVTTL compatible saturation voltages and high speed operation. Where desired, the $V_{CC}$ and $V_O$ terminals may be tied together to achieve conventional photo-darlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

These optocouplers are for use in LVTTL/LVCMOS or other low power applications. A 400% minimum current transfer ratio is guaranteed over 0 to +70˚C operating range for only 0.5 mA of LED current.

The HCPL-070L and HCPL-073L are surface mount devices packaged in an industry standard SOIC-8 footprint.

The SOIC-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

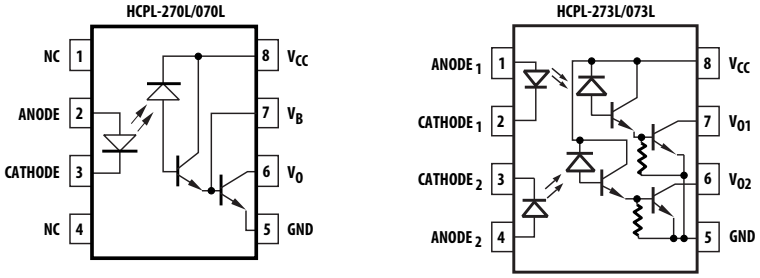
### Features

- 3.3V/5V Dual Supply Voltages
- Low power consumption
- High current transfer ratio
- Low input current requirements – 0.5 mA
- LVTTL/LVCMOS compatible output
- Performance guaranteed over temperature 0°C to +70°C
- Base access allows gain bandwidth adjustment
- High output current – 60 mA
- Safety approval, UL, IEC/EN/DIN EN 60747-5-2, CSA

### Applications

- Ground isolate most logic families – LVTTL/LVCMOS
- Low input current line receiver
- High voltage insulation
- EIA RS-232C line receiver
- Telephone ring detector
- V AC line voltage status indicator – low input power dissipation
- Low power systems – ground isolation

### Functional Diagram




TRUTH TABLE

| LED | $V_O$ |
|---|---|
| ON | LOW |
| OFF | HIGH |

**A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.**

***CAUTION:*** *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

## Ordering Information

HCPL-270L, HCPL-273L, HCPL-070L and HCPL-073L are UL Recognized with 3750 Vrms for 1 minute per UL1577 and are approved under CSA Component Acceptance Notice #5, File CA 88324.

| Part Number | Option | | Package | Surface Mount | Gull Wing | Tape & Reel | UL 5000 Vrms/ 1 Minute rating | IEC/EN/DIN EN 60747-5-2 | Quantity |
|---|---|---|---|---|---|---|---|---|---|
| | RoHS Compliant | non RoHS Compliant | | | | | | | |
| | -000E | no option | 300 mil DIP-8 | | | | | | 50 per tube |
| HCPL-270L | -300E | -300 | | X | X | | | | 50 per tube |
| HCPL-273L | -500E | -500 | | X | X | X | | | 1000 per reel |
| | -060E | -060 | | | | | | X | 100 per tube |
| | -560E | -560 | | X | X | X | | X | 1500 per reel |
| | -000E | no option | SO-8 | X | | | | | 100 per tube |
| HCPL-070L | -500E | -500 | | X | | X | | | 1500 per reel |
| HCPL-073L | -060E | -060 | | X | | | | X | 100 per tube |
| | -560E | -560 | | X | | X | | X | 1500 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:
HCPL-273L-500E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval and RoHS compliant.

Example 2:
HCPL-273L to order product of 300 mil DIP package in Tube packaging and non RoHS compliant.

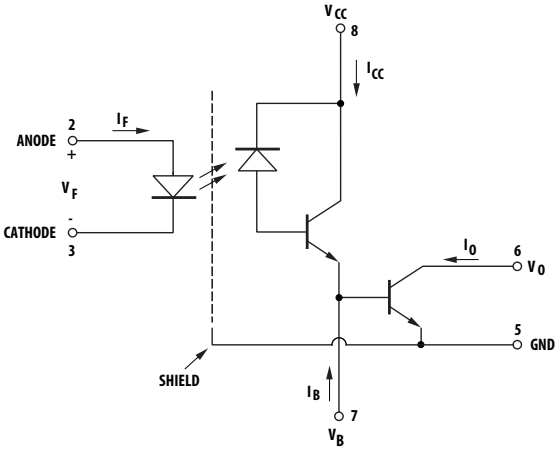
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use '–XXXE.'

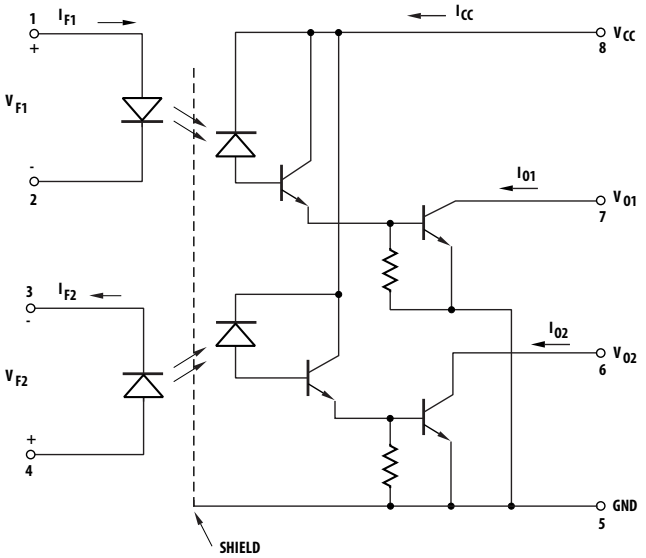
## Selection Guide

| 8-Pin DIP (300 Mil) | | Small Outline SO-8 | | | |
|---|---|---|---|---|---|
| Single Channel Package HCPL- | Dual Channel Package HCPL- | Single Channel Package HCPL- | Dual Channel Package HCPL- | Minimum Input ON Current ($I_F$) | Minimum CTR |
| 270L | 273L | 070L | 073L | 0.5 mA | 400% |

## Schematic




HCPL-270L/HCPL-070L

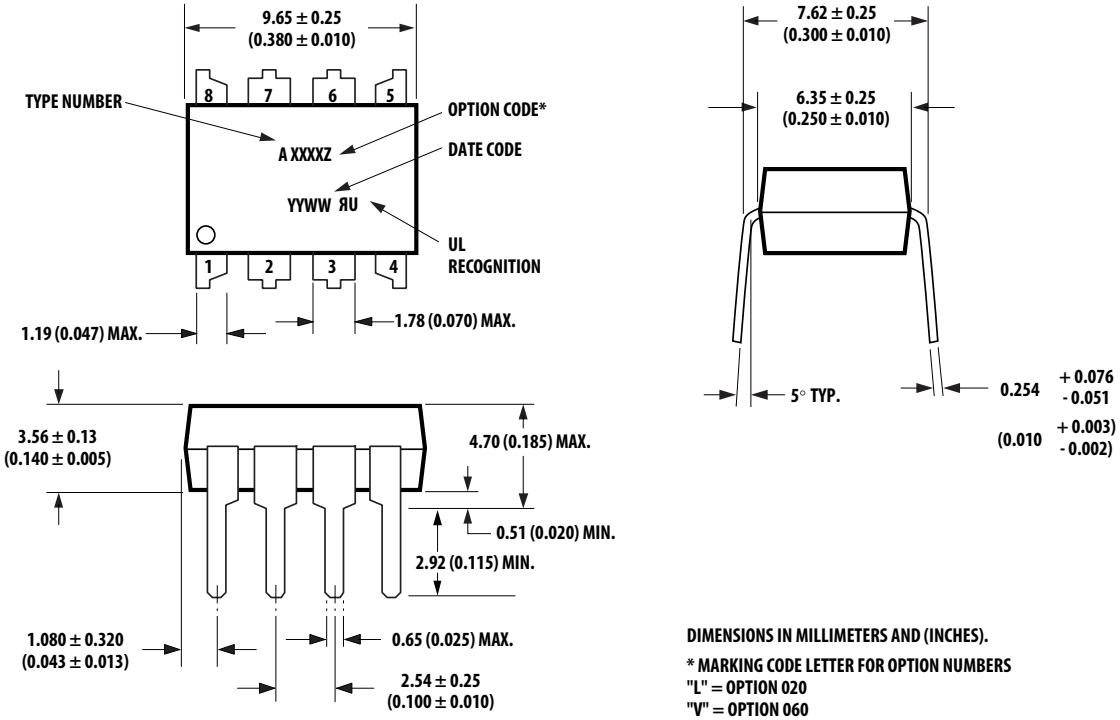



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED

HCPL-273L/HCPL-073L

## Package Outline Drawings

### 8-Pin DIP Package

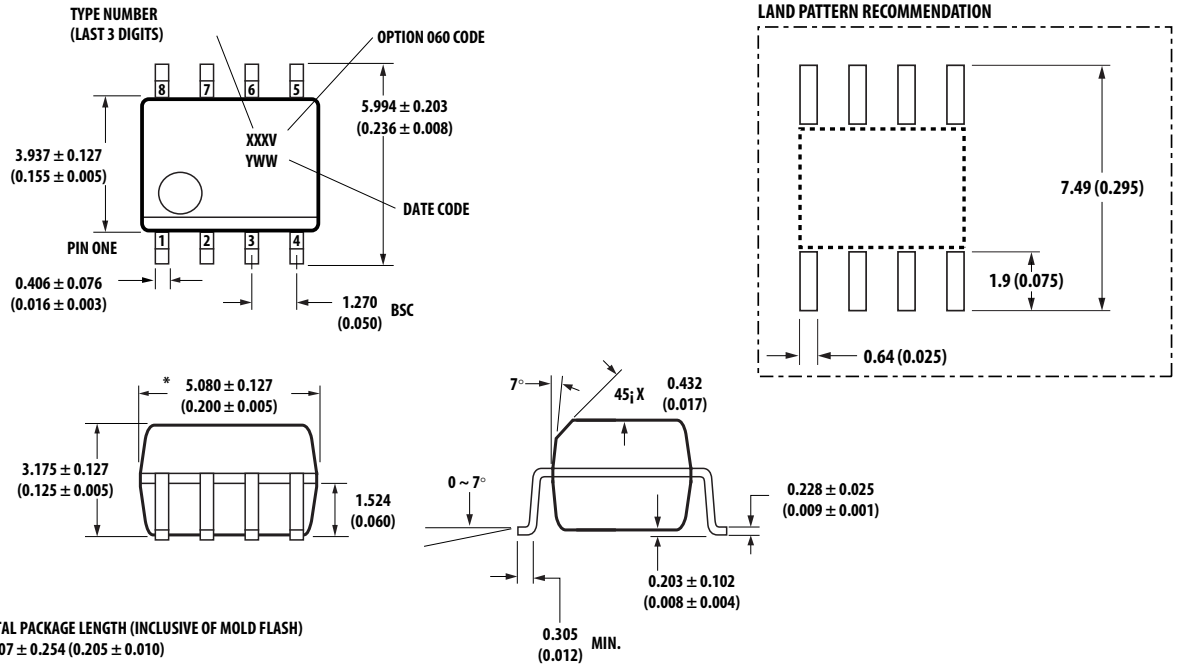



DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

### Small Outline SO-8 Package

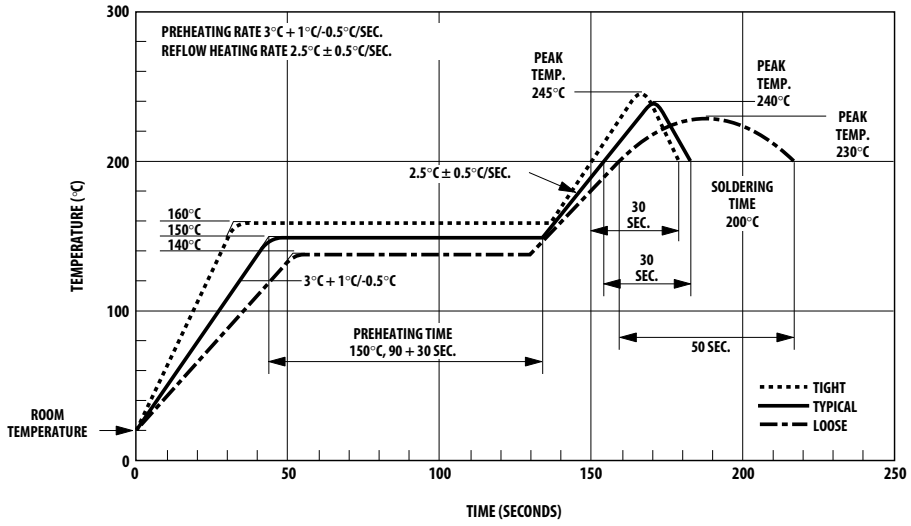



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.
OPTION NUMBER 500 NOT MARKED.

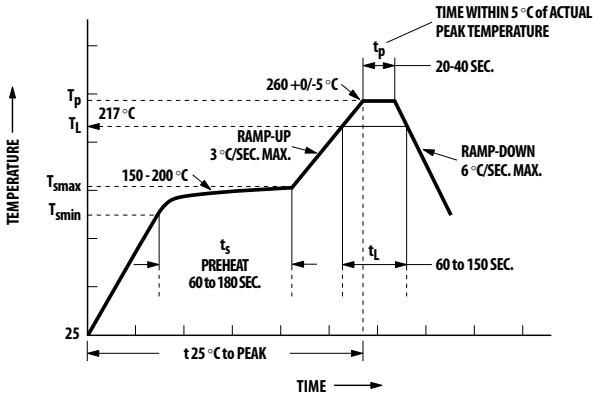
NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

## Solder Reflow Temperature Profile




**Note: Non-halide flux should be used.**

## Recommended Pb-Free IR Profile




**NOTES:**
**THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.**
**$T_{smax}$ = 200 °C, $T_{smin}$ = 150 °C**

**Note: Non-halide flux should be used.**

## Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL Approval under UL 1577, Component Recognition Program, File E55361.

CSA Approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2

Approved under

IEC 60747-5-2:1997 + A1:2002

EN 60747-5-2:2001 + A1:2002

DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01 (Option 060 only)

## Insulation and Safety Related Specifications

| Parameter | Symbol | 8-Pin DIP (300 Mil) Value | SO-8 Value | Units | Conditions |
|---|---|---|---|---|---|
| Minimum External Air Gap (External Clearance) | L (101) | 7.1 | 4.9 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L (102) | 7.4 | 4.8 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | 0.08 | mm | Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity. |
| Tracking Resistance (Comparative Tracking Index) | CTI | 200 | 200 | Volts | DIN IEC 112/VDE 0303 Part 1. |
| Isolation Group | | IIIa | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1). |

## IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics

| Description | Symbol | 8-pin DIP (300 mil) | SO-8 | Units |
|---|---|---|---|---|
| Installation classification per DIN VDE 0110/1.89, Table 1 | | | | |
| for rated mains voltage ≤ 150 V rms | | | I-IV | |
| for rated mains voltage ≤ 300 V rms | | I-IV | I-III | |
| for rated mains voltage ≤ 600 V rms | | I-III | I-II | |
| Climatic Classification | | 55/100/21 | 55/100/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 630 | 566 | $V_{peak}$ |
| Input to Output Test Voltage, Method b* $V_{PR}$ = 1.875 x $V_{IORM}$, 100% Production Test with $t_P$ = 1 sec, Partial Discharge < 5 pC | $V_{PR}$ | 1181 | 1063 | $V_{peak}$ |
| Input to Output Test Voltage, Method a* $V_{PR}$ = 1.5 x $V_{IORM}$, Type and Sample Test, $t_P$ = 60 sec, Partial Discharge < 5 pC | $V_{PR}$ | 945 | 849 | $V_{peak}$ |
| Highest Allowable Overvoltage* (Transient Overvoltage, $t_{ini}$ = 10 sec) | $V_{IOTM}$ | 6000 | 4000 | $V_{peak}$ |
| Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 11, Thermal Derating curve.) | | | | |
| Case Temperature | $T_S$ | 175 | 150 | ˚C |
| Current (Input Current $I_F$, $P_S$ = 0) | $I_{S,INPUT}$ | 400 | 150 | mA |
| Output Power | $P_{S,OUTPUT}$ | 600 | 600 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | ≥ $10^9$ | ≥ $10^9$ | Ω |

***Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-2, for a detailed description.**
**Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.**

## Absolute Maximum Ratings (No Derating Required up to +85˚C)

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Storage Temperature | $T_S$ | –55 | 125 | ˚C |
| Operating Temperature | $T_A$ | –40 | 85 | ˚C |
| Average Forward Input Current | $I_{F(AVG)}$ | | 20 | mA |
| Peak Forward Input Current (50% Duty Cycle, 1 ms Pulse Width) | $I_{F(PEAK)}$ | | 40 | mA |
| Peak Transient Input Current (< 1 µs Pulse Width, 300 pps) | $I_{F(TRAN)}$ | | 1.0 | A |
| Reverse Input Voltage | $V_R$ | | 5 | V |
| Input Power Dissipation | $P_I$ | | 35 | mW |
| Output Current (Pin 6) | $I_O$ | | 60 | mA |
| Emitter Base Reverse Voltage (Pin 5-7) | $V_{EB}$ | | 0.5 | V |
| Supply Voltage and Output Voltage | $V_{CC}$ | –0.5 | 7 | V |
| Output Power Dissipation | $P_O$ | | 100 | mW |
| Total Power Dissipation | $P_T$ | | 135 | mW |
| Lead Solder Temperature (for Through Hole Devices) | | 260˚C for 10 sec., 1.6 mm below seating plane. | | |
| Reflow Temperature Profile (for SOIC-8 and Option #300) | | See Package Outline Drawings section. | | |

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 2.7 | 7.0 | V |
| Forward Input Current (ON) | $I_{F(ON)}$ | 0.5 | 12.0 | mA |
| Forward Input Voltage (OFF) | $V_{F(OFF)}$ | 0 | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | 70 | ˚C |

## Electrical Specifications

0˚C ≤ $T_A$ ≤ +70˚C, 2.7 V ≤ $V_{CC}$ ≤ 3.3 V, 0.5 mA ≤ $I_{F(ON)}$ ≤ 12 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified.
All typicals at $T_A$ = 25˚C. (See Note 8.)

| Parameter | Sym. | Device HCPL- | Min. | Typ.* | Max. | Units | Test Conditions | | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| Current Transfer Ratio | CTR | | 400 | 1300 | 5000 | % | $I_F$ = 0.5 mA | $V_{CC}$ = 3.3 V<br>$V_O$ = 0.4 V | 1, 2 | 2 |
| Logic Low Output Voltage | $V_{OL}$ | | | 0.05 | 0.3 | V | $I_F$ = 1.6 mA,<br>$I_O$ = 8 mA | $V_{CC}$ = 3.3 V | | |
| | | | | 0.05 | 0.4 | V | $I_F$ = 5.0 mA,<br>$I_O$ = 15 mA | | | |
| Logic High Output Current | $I_{OH}$ | | | 5 | 25 | µA | $V_O$ = $V_{CC}$ = 3.3 V | $I_F$ = 0 mA | | 2 |
| Logic Low Supply Current | $I_{CCL}$ | 270L/070L | | 0.4 | 1.3 | mA | $V_{CC}$ = 3.3 V | $I_{F1}$ = $I_{F2}$ = 1.6 mA<br>$V_{O1}$ = $V_{O2}$ = Open | | |
| | | 273L/073L | | 0.8 | 2.7 | mA | | | | |
| Logic High Supply Current | $I_{CCH}$ | 270L/070L | | 0.002 | 1 | µA | $V_{CC}$ = 3.3 V | $I_{F1}$ = $I_{F2}$ = 0 mA<br>$V_{O1}$ = $V_{O2}$ = Open | | |
| | | 273L/073L | | 0.002 | 2 | µA | | | | |
| Input Forward Voltage | $V_F$ | | | 1.5 | 1.7 | V | $T_A$ = 25˚C | $I_F$ = 1.6 mA | 3, 4 | |
| Input Reverse Breakdown Voltage | $BV_R$ | | 5.0 | | | V | $I_R$ = 10 µA,<br>$T_A$ = 25˚C | | | 2 |
| Temperature Coefficient of Forward Voltage | ΔVF/<br>ΔTA | | | -1.8 | | mV/°C | $I_F$ = 1.6 mA | | | |
| Input Capacitance | $C_{IN}$ | | | 60 | | pF | f = 1 MHz, $V_F$ = 0 | | | 2 |

***All typical values at $T_A$ = 25˚C and $V_{CC}$ = 3.3 V, unless otherwise noted.**

## Electrical Specifications

0°C ≤ $T_A$ ≤ 70°C, 4.5 V ≤ $V_{CC}$ ≤ 7 V, 0.5 mA ≤ $I_{F(ON)}$ ≤ 12 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified.
All Typicals at $T_A$ = 25°C. (See note 8.)

| Parameter | Sym. | Device | Min. | Typ.* | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|
| Current Transfer Ratio | CTR | | 300 | 1600 | 2600 | % | $I_F$ = 1.6 mA, $V_{CC}$ = 4.5V, $V_O$ = 0.5V | 2, 3 | 2 |
| Logic Low Output Voltage | $V_{OL}$ | | | 0.1 | 0.4 | V | $I_F$ = 1.6 mA, $I_O$ = 4.8 mA, $V_{CC}$ = 4.5V | 1 | |
| Logic High Output Current | $I_{OH}$ | | | 0.1 | 250 | µA | $V_O$ = $V_{CC}$ = 7 V, $I_F$ = 0 mA | | 2 |
| Logic Low Supply Current | $I_{CCL}$ | | | 0.9 | 3 | mA | $V_{CC}$ = 7 V, $I_{F1}$ = $I_{F2}$ = 1.6 mA<br>$V_{01}$ = $V_{02}$ = Open | 5 | |
| Logic High Supply Current | $I_{CCH}$ | | | 0.004 | 20 | µA | $V_{CC}$ = 7 V, $I_{F1}$ = $I_{F2}$ = 0 mA,<br>$V_{01}$ = $V_{02}$ = Open | 5 | |
| Input Forward Voltage | $V_F$ | | | 1.4 | 1.7 | V | $T_A$ = 25°C | 4 | |
| | | | | | 1.75 | V | $I_F$ = 1.6 mA | | |
| Input Reverse Breakdown Voltage | $BV_R$ | | 5 | | | V | $I_R$ = 10 µA, $T_A$ = 25°C | | 2 |
| Temperature Coefficient of Forward Voltage | ΔVF/<br>ΔTA | | | -1.8 | | mV/°C | $I_F$ = 1.6 mA | | |
| Input Capacitance | $C_{IN}$ | | | 60 | | pF | f = 1 MHz, $V_F$ = 0 | | 2 |

***All typical values at $T_A$ = 25°C and $V_{CC}$ = 5 V, unless otherwise noted.**

## Switching Specifications (AC)

Over Recommended Operating Conditions ($T_A$ = 0˚C to +70˚C), $V_{CC}$ = 3.3 V, unless otherwise specified. (See Note 8.)

| Parameter | Sym. | Min. | Typ.* | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low at Output | $t_{PHL}$ | | | 30 | µs | $I_F$ = 0.5 mA, Rl = 4.7 kΩ | 5 | 2 |
| Propagation Delay Time to Logic High at Output | $t_{PLH}$ | | | 90 | µs | $I_F$ = 0.5 mA, $R_L$ = 4.7 kΩ | 5 | 2 |
| Common Mode Transient Immunity at Logic High Level Output | $\|CM_H\|$ | 1000 | 10000 | | V/µs | $I_F$ = 0 mA, $T_A$ = 25˚C, Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 $V_{p-p}$ | 6 | 2, 6, 7 |
| Common Mode Transient Immunity at Logic Low Level Output | $\|CM_L\|$ | 1000 | 10000 | | V/µs | $I_F$ = 1.6 mA, $T_A$ = 25˚C, Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 $V_{p-p}$ | 6 | 2, 6, 7 |

***All typical values at $T_A$ = 25˚C and $V_{CC}$ = 3.3 V, unless otherwise noted.**

## Switching Specifications (AC)

Over recommended operating conditions ($T_A$ = 0°C to 70°C), $V_{CC}$ = 5 V, unless otherwise specified. (See note 8.)

| Parameter | Sym. | Min. | Typ.* | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to LogicLow at Output | $t_{PHL}$ | | | 25 | | $I_F$ = 1.6 mA, $R_L$ = 2.2 kΩ | 6, 7, 8, 9 | 2 |
| Propagation Delay Time to Logic High at Output | $t_{PLH}$ | | | 50 | | $I_F$ = 1.6 mA, $R_L$ = 2.2 kΩ | 7, 8, 9 | 2 |
| Common Mode Transient Immunity at Logic High Output | $\|CM_H\|$ | 1000 | 10000 | | V/µs | $I_F$ = 0 mA, $T_A$ = 25°C, $R_L$ = 2.2 kΩ $\|V_{CM}\|$ = 10 Vp-p | 10 | 2, 6, 7 |
| Common Mode Transient Immunity at Logic Low Output | $\|CM_H\|$ | 1000 | 10000 | | V/µs | $I_F$ = 1.6 mA, $T_A$ = 25°C, $R_L$ = 2.2 kΩ $\|V_{CM}\|$ = 10 Vp-p | 10 | 2, 6, 7 |

***All typical values at $T_A$ = 25˚C and $V_{CC}$ = 5 V, unless otherwise noted.**

## Package Characteristics

| Parameter | Sym. | Device HCPL- | Min. | Typ.* | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage** | $V_{ISO}$ | | 3750 | | | V rms | RH ≤ 50%, t = 1 min., $T_A$ = 25°C | | 4, 9 |
| Resistance (Input-Output) | $R_{I-O}$ | | | $10^{12}$ | | Ω | $V_{I-O}$ = 500 Vdc RH ≤ 45% | | 4 |
| Capacitance (Input-Output) | $C_{I-O}$ | | | 0.6 | | pF | f = 1 MHz | | 11 |
| Input-Input Insulation Leakage Current | $I_{I-I}$ | | 0.005 | | | µA | RH ≤ 45% $V_{I-I}$ = 500 Vdc | | 5 |
| Input-Input Insulation Leakage Current | $R_{I-I}$ | | | $10^{11}$ | | Ω | | | 5 |
| Capacitance (Input-Input) | $C_{I-I}$ | 270L 273L | | 0.03 | | pF | | | 5 |
| | | 070L 073L | | 0.25 | | | | | |

*All typical values at TA = 25°C, unless otherwise noted.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

**Notes:**

1. Pin 5 should be the most negative voltage at the detector side.
2. Each channel.
3. DC CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, $I_O$, to the forward LED input current, $I_F$, times 100%.
4. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
6. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) $dV_{CM}/dt$ of the common mode pulse, $V_{CM}$, to assure that the output will remain in a Logic High state (i.e., $V_O$ > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) $dV_{CM}/dt$ of the common mode pulse, $V_{CM}$, to assure that the output will remain in a Logic Low state (i.e., $V_O$ < 0.8 V).
7. In applications where dV/dt may exceed 50,000 V/µs (such as static discharge) a series resistor, $R_{CC}$, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC}$ = 110 Ω.
8. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 adjacent to the device is recommended.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 4500 V rms for 1 second (leakage detection current limit, $I_{I-O}$ < 5 µA).
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 V rms for 1 second (leakage detection current limit, $I_{I-O}$ < 5 µA).
11. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
12. Derate linearly above 65°C free-air temperature at a rate of 2.3 mW/°C for the SO-8 package.

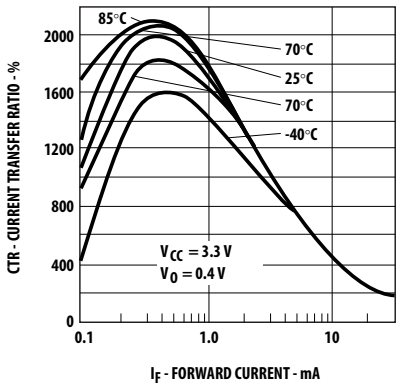



Figure 1. Current transfer ratio vs. forward current

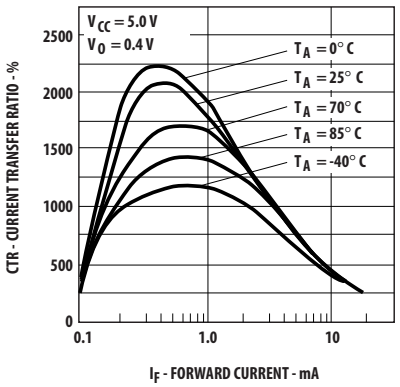



Figure 2. Current transfer ratio vs. forward current

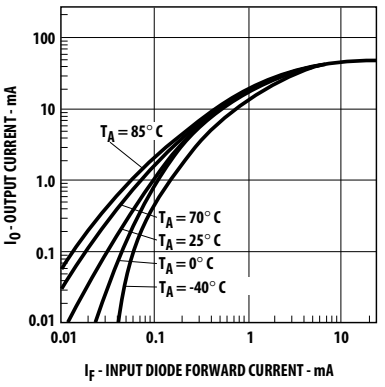



Figure 3. Output current vs. input diode forward current

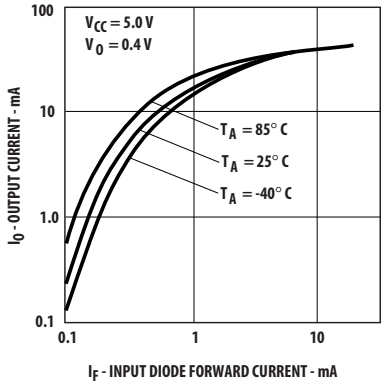



Figure 4. Output current vs. input diode forward current

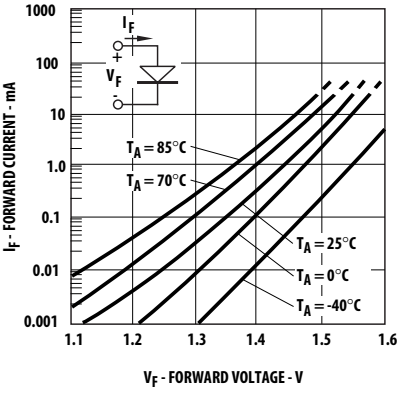



Figure 5. Input diode forward current vs. forward voltage

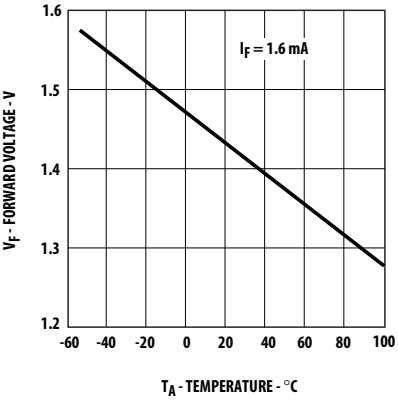



Figure 6. Forward voltage vs. temperature

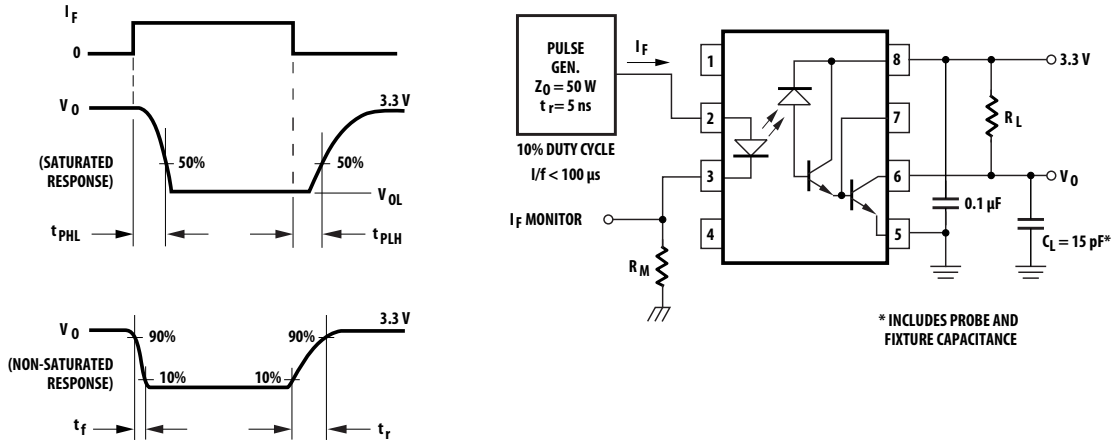



Figure 7. Switching test circuit

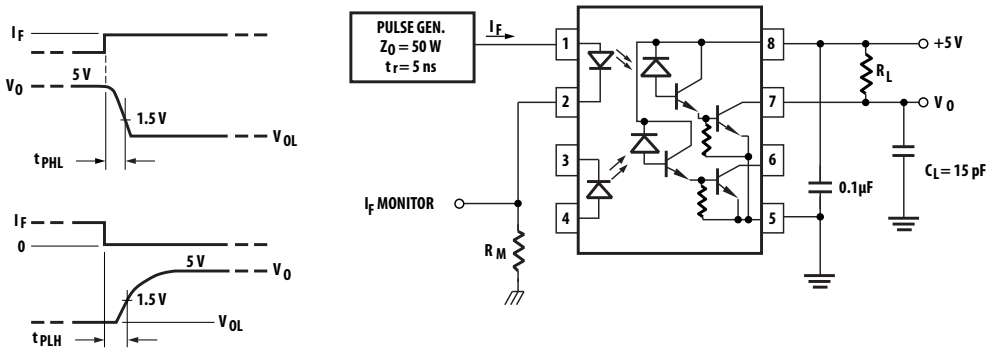



**Figure 8. Switching test circuit**

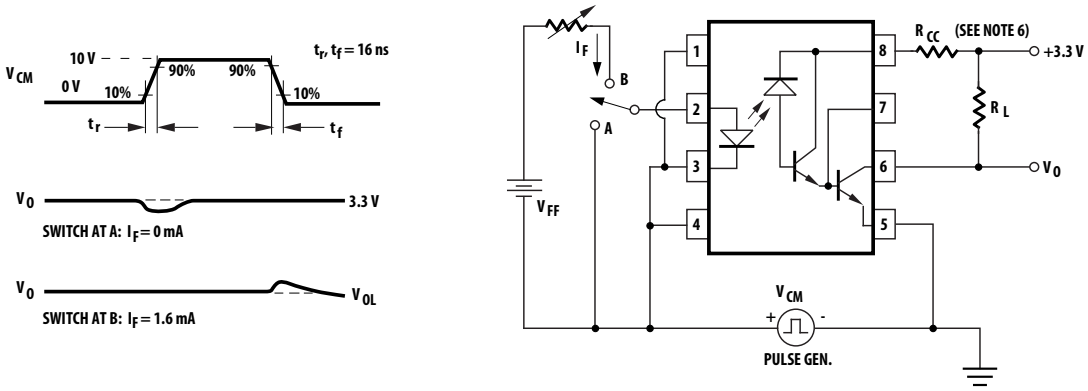



**Figure 9. Test circuit for transient immunity and typical waveforms**

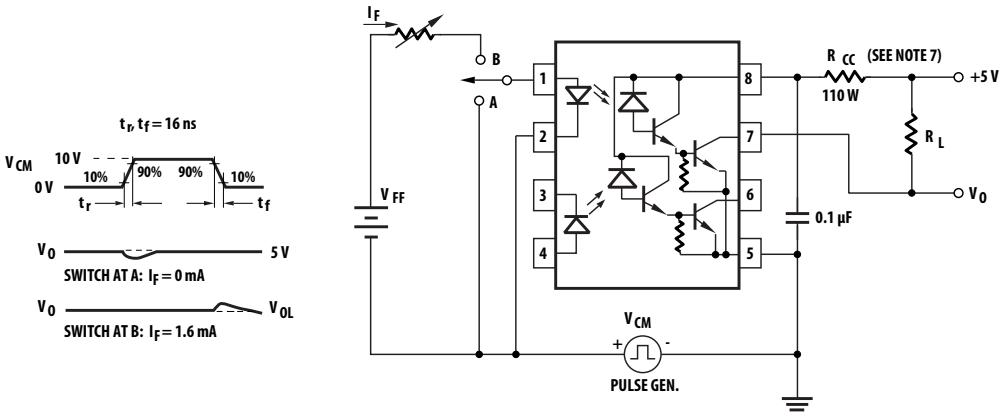



**Figure 10. Test circuit for transient immunity and typical waveforms**

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**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
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