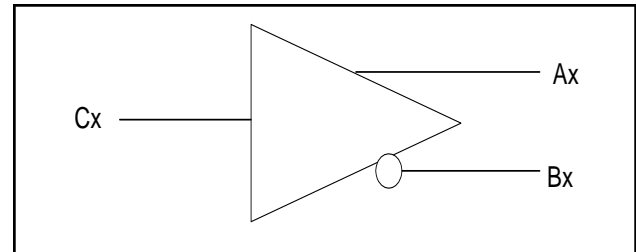


Features

- High Speed CMOS Technology
- Complementary Outputs
- Positive Voltage Control
- Low Power Dissipation
- Plastic SOIC Package for SMT Applications
- Tape and Reel Packaging Available
- Lead-Free SOIC-16 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free "Green" Mold Compound
- 260°C Reflow Compatible
- RoHS* Compliant Version of DR65-0001

Logic Diagram



Description

M/A-COM's MADRCC0004 is a Quad channel driver used to translate TTL control inputs into gate voltages for GaAs FET microwave switches and attenuators. High speed analog CMOS technology is utilized to achieve low power dissipation at moderate to high speeds, encompassing most microwave switching applications.

Ordering Information

Part Number	Package
MADRCC0004	Bulk Packaging
MADRCC0004TR	1000 piece reel

Note: Reference Application Note M513 for reel size information.

Pin Configuration

Pin No.	Function	Pin No.	Function
1	A3	9	C2
2	B3	10	C1
3	A4	11	GND
4	B4	12	GND
5	V _{EE}	13	A1
6	V _{CC}	14	B1
7	C4	15	A2
8	C3	16	B2

Guaranteed Operating Ranges

Symbol	Parameter ¹	Unit	Min	Typical	Max
V _{CC}	Positive DC Supply Voltage	V	4.5	5.0	5.5
V _{EE}	Negative DC Supply Voltage	V	-5.5	-5.0	-4.5
T _A	Operating Ambient Temperature	°C	-40	+25	+85
I _{OH}	DC Output Current - HIGH	mA	—	—	-1.0
I _{OL}	DC Output Current - LOW	mA	—	—	1.0
T _{rise} , T _{fall}	Maximum Input Rise or Fall Time	nS	—	—	500

1. All voltages are relative to GND.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

ADVANCED: Data Sheets contain information regarding a product M/A-COM Technology Solutions is considering for development. Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.
PRELIMINARY: Data Sheets contain information regarding a product M/A-COM Technology Solutions has under development. Performance is based on engineering tests. Specifications are typical. Mechanical outline has been fixed. Engineering samples and/or test data may be available. Commitment to produce in volume is not guaranteed.

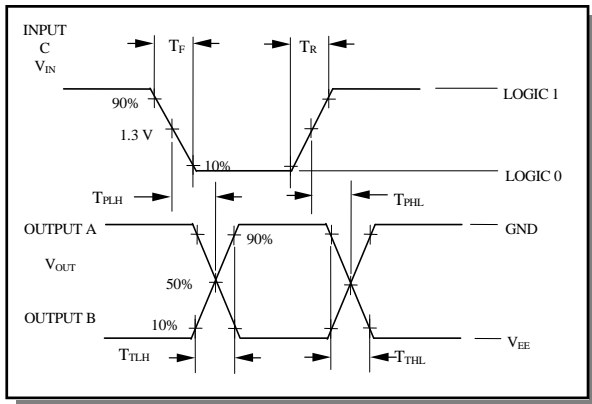
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AC & DC Characteristics Over Guaranteed Operating Range

Symbol	Parameter	Test Conditions	Units	Min	Typ	Max
V_{IH}	Input HIGH Voltage	Guaranteed HIGH Input Voltage	V	2.0	—	-
V_{IL}	Input LOW Voltage	Guaranteed LOW Input Voltage	V	-	—	0.8
V_{OH}	Output HIGH Voltage	$I_{OH} = -1 \text{ mA}$ $V_{EE} = \text{Max}$	V	-0.1	—	-
V_{OL}	Output LOW Voltage	$I_{OL} = 1 \text{ mA}$ $V_{EE} = \text{Max}$	V	—	—	$V_{EE} + 0.1$
I_{IN}	Input Current	$V_{IN} = V_{CC}$ or GND $V_{EE} = \text{Min}$	μA	-10	0	10
I_{CC}	Quiescent Supply Current	$V_{CC} = \text{Max}$ $V_{EE} = \text{Min}$ $V_{IN} = V_{CC}$ or GND	μA	—	—	400
ΔI_{CC}	Additional Supply Current, per TTL Input pin	$V_{CC} = \text{Max}$ $V_{IN} = V_{CC} - 2.1 \text{ V}$	mA	—	—	1.0
T_{PHL}, T_{PLH}	Propagation Delay	Guaranteed -40° C to $+85^\circ \text{ C}$	nS	—	—	50
T_{THL}, T_{TLH}	Output Transition Time	Guaranteed -40° C to $+85^\circ \text{ C}$	nS	—	—	25
	Delay Skew, Output A to Output B	Guaranteed -40° C to $+85^\circ \text{ C}$	nS	—	—	8

Switching Waveforms



Note: See Switching Wave Forms for the definition of the switching terms. Supplies must be by-passed with .01 μF Capacitors.

Note: Unused inputs must be tied to Ground

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Absolute Maximum Ratings^{2,3}

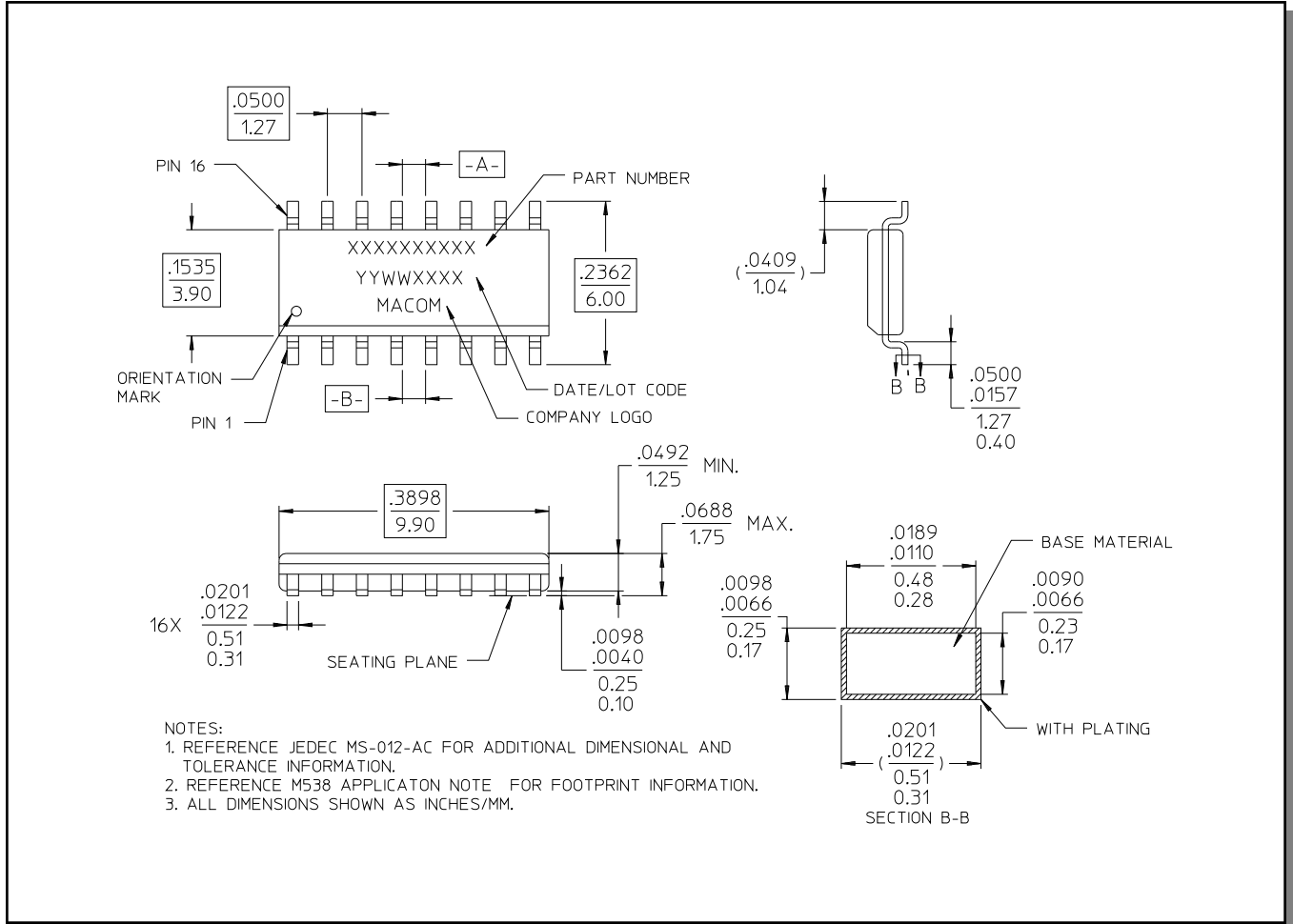
Parameter	Absolute Maximum
V_{CC}	- .5V to + 6.0 V
V_{EE}	- 6.0 V to - .5 V
$V_{CC} - V_{EE}$	12 V
V_{IN}^4	$V_{CC} + .5 \text{ V}$
V_{OUT}	$V_{EE} - .5 \text{ V}$
Storage Temperature	-65° C to $+150^\circ \text{ C}$
Operating Temperature	-40° C to $+85^\circ \text{ C}$

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Truth Table

Input	Outputs	
C_X	A_X	B_X
0	V_{EE}	GND
1	GND	V_{EE}

Lead-Free, SOIC-16[†]



[†] Reference Application Note M538 for lead-free solder reflow recommendations.

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