

2Mx8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
 - 30 mW (typical) operating
 - 12 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
 - 1.65V–1.98V V_{DD} (62/65WV20488EALL)
 - 2.2V–3.6V V_{DD} (62/65WV20488EBLL)
- Fully static operation: no clock or refresh required
- Industrial (-40°C to +85°C) and Automotive (-40°C to +125°C) temperature support

DESCRIPTION

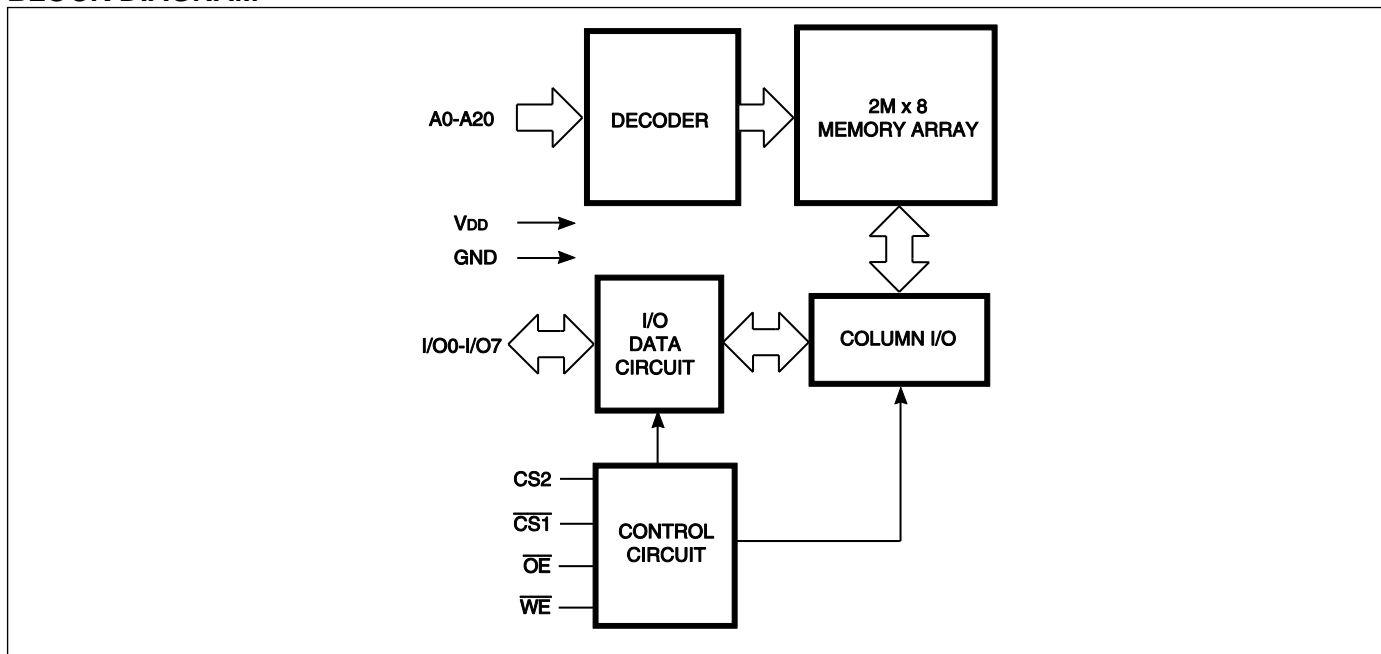
The ISSI IS62WV20488EALL/BLL and IS65WV20488EALL/BLL are high-speed, 16M bit static RAMs organized as 2M words by 8 bits. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS62WV20488EALL/BLL and IS65WV20488EALL/BLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm).

BLOCK DIAGRAM



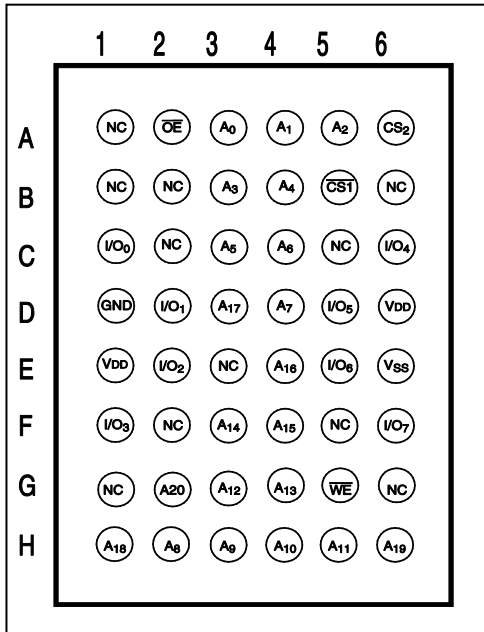
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PIN CONFIGURATION (2M x 8 Low Power)

48-pin mini BGA (B) (6mm x 8mm)



PIN DESCRIPTIONS

| | |
|------------------|---------------------|
| A0-A20 | Address Inputs |
| $\overline{CS1}$ | Chip Enable 1 Input |
| CS2 | Chip Enable 2 Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| NC | No Connection |
| VDD | Power |
| GND | Ground |

TRUTH TABLE

| Mode | \overline{WE} | $\overline{CS1}$ | CS2 | \overline{OE} | I/O Operation | VDD Current |
|-----------------|-----------------|------------------|-----|-----------------|---------------|-----------------|
| Not Selected | X | H | X | X | High-Z | ISB1, ISB2 |
| (Power-down) | X | X | L | X | High-Z | ISB1, ISB2 |
| Output Disabled | H | L | H | H | High-Z | I _{cc} |
| Read | H | L | H | L | Dout | I _{cc} |
| Write | L | L | H | X | Din | I _{cc} |

OPERATING RANGE (VDD)

| Range | Ambient Temperature | 1.65V – 1.98V | 2.2V - 3.6V |
|------------|---------------------|------------------------|----------------------------|
| Commercial | 0°C to +70°C | IS62WV20488EALL (55ns) | IS62WV20488EBLL (45, 55ns) |
| Industrial | -40°C to +85°C | IS62WV20488EALL (55ns) | IS62WV20488EBLL (45, 55ns) |
| Automotive | -40°C to +125°C | IS65WV20488EALL (55ns) | IS65WV20488EBLL (55ns) |

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|-------------------------------------|------|
| V _{term} | Terminal Voltage with Respect to GND | -0.2 to +3.9(V _{DD} +0.3V) | V |
| t _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| V _{DD} | V _{DD} Related to GND | -0.2 to +3.9(V _{DD} +0.3V) | V |
| t _{Stg} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current (LOW) | 20 | mA |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE⁽¹⁾

| Range | Device Marking | Ambient Temperature | V _{DD} (min) | V _{DD} (typ) | V _{DD} (max) |
|------------|-----------------|---------------------|-----------------------|-----------------------|-----------------------|
| Commercial | IS62WV20488EALL | 0°C to +70°C | 1.65V | 1.8V | 1.98V |
| Industrial | IS62WV20488EALL | -40°C to +85°C | 1.65V | 1.8V | 1.98V |
| Automotive | IS65WV20488EALL | -40°C to +125°C | 1.65V | 1.8V | 1.98V |
| Commercial | IS62WV20488EBLL | 0°C to +70°C | 2.2V | 3.3V | 3.6V |
| Industrial | IS62WV20488EBLL | -40°C to +85°C | 2.2V | 3.3V | 3.6V |
| Automotive | IS65WV20488EBLL | -40°C to +125°C | 2.2V | 3.3V | 3.6V |

Note:

1. Full device AC operation assumes a 100 μs ramp time from 0 to V_{cc}(min) and 200 μs wait time after V_{cc} stabilization.

PIN CAPACITANCE⁽¹⁾

| Parameter | Symbol | Test Condition | Max | Units |
|--------------------------|------------------|---|-----|-------|
| Input capacitance | C _{IN} | T _A = 25°C, f = 1 MHz, V _{DD} = V _{DD} (typ) | 10 | pF |
| DQ capacitance (IO0–IO7) | C _{I/O} | | 10 | pF |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS⁽¹⁾

| Parameter | Symbol | Rating | Units |
|--|------------------|--------|-------|
| Thermal resistance from junction to ambient (airflow = 1m/s) | R _{θJA} | 38.3 | °C/W |
| Thermal resistance from junction to case | R _{θJC} | 6.86 | °C/W |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

ELECTRICAL CHARACTERISTICS

IS62(5)WV20488EALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------------|---------------------|---|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $I_{OH} = -0.1 \text{ mA}$ | 1.4 | — | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 0.1 \text{ mA}$ | — | 0.2 | V |
| $V_{IH}^{(1)}$ | Input HIGH Voltage | | 1.4 | $V_{DD} + 0.2$ | V |
| $V_{IL}^{(1)}$ | Input LOW Voltage | | -0.2 | 0.4 | V |
| I_{LI} | Input Leakage | $GND < V_{IN} < V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND < V_{IN} < V_{DD}$, Output Disabled | -1 | 1 | μA |

Notes:

- $V_{ILL}(\text{min}) = -1.0\text{V AC}$ (pulse width < 10ns). Not 100% tested.
 $V_{IHH}(\text{max}) = V_{DD} + 1.0\text{V AC}$ (pulse width < 10ns). Not 100% tested.

IS62(5)WV20488EBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------------|---------------------|---|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $2.2 \leq V_{DD} < 2.7$, $I_{OH} = -0.1 \text{ mA}$ | 2.0 | — | V |
| | | $2.7 \leq V_{DD} \leq 3.6$, $I_{OH} = -1.0 \text{ mA}$ | 2.4 | — | V |
| V_{OL} | Output LOW Voltage | $2.2 \leq V_{DD} < 2.7$, $I_{OL} = 0.1 \text{ mA}$ | — | 0.4 | V |
| | | $2.7 \leq V_{DD} \leq 3.6$, $I_{OL} = 2.1 \text{ mA}$ | — | 0.4 | V |
| $V_{IH}^{(1)}$ | Input HIGH Voltage | $2.2 \leq V_{DD} < 2.7$ | 1.8 | $V_{DD} + 0.3$ | V |
| | | $2.7 \leq V_{DD} \leq 3.6$ | 2.2 | $V_{DD} + 0.3$ | V |
| $V_{IL}^{(1)}$ | Input LOW Voltage | $2.2 \leq V_{DD} < 2.7$ | -0.3 | 0.6 | V |
| | | $2.7 \leq V_{DD} \leq 3.6$ | -0.3 | 0.8 | V |
| I_{LI} | Input Leakage | $GND < V_{IN} < V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND < V_{IN} < V_{DD}$, Output Disabled | -1 | 1 | μA |

Notes:

- $V_{ILL}(\text{min}) = -2.0\text{V AC}$ (pulse width < 10ns). Not 100% tested.
 $V_{IHH}(\text{max}) = V_{DD} + 2.0\text{V AC}$ (pulse width < 10ns). Not 100% tested.

**IS62(5)WV20488EALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER
(OVER THE OPERATING RANGE)**

| Symbol | Parameter | Test Conditions | Grade | Typ. | Max. | Unit |
|--------|--|--|-------|------|------|------|
| ICC | V _{DD} Dynamic Operating Supply Current | V _{DD} =V _{DD} (max), I _{OUT} =0mA, f=f _{MAX} | Com. | 6 | 12 | mA |
| | | | Ind. | - | 12 | |
| | | | Auto. | - | 12 | |
| ICC1 | V _{DD} Static Operating Supply Current | V _{DD} =V _{DD} (max), I _{OUT} = 0mA, f=0Hz | Com. | 3 | 6 | mA |
| | | | Ind. | - | 6 | |
| | | | Auto. | - | 6 | |
| ISB1 | CMOS Standby Current (CMOS Inputs) | V _{DD} =V _{DD} (max), (1) 0V ≤ CS2 ≤ 0.2V or (2) $\overline{CS1} \geq V_{DD} - 0.2V$, CS2 ≥ V _{DD} - 0.2V | Com. | 30 | 50 | μA |
| | | | Ind. | - | 65 | μA |
| | | | Auto. | - | 165 | μA |

Note:

Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25°C

**IS62(5)WV20488EBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER
(OVER THE OPERATING RANGE)**

| Symbol | Parameter | Test Conditions | Grade | Typ. | Max. | Unit |
|--------|--|--|-------|------|------|------|
| ICC | V _{DD} Dynamic Operating Supply Current | V _{DD} =V _{DD} (max), I _{OUT} =0mA, f=f _{MAX} | Com. | 6 | 12 | mA |
| | | | Ind. | - | 12 | |
| | | | Auto. | - | 12 | |
| ICC1 | V _{DD} Static Operating Supply Current | V _{DD} =V _{DD} (max), I _{OUT} = 0mA, f=0Hz | Com. | 3 | 6 | mA |
| | | | Ind. | - | 6 | |
| | | | Auto. | - | 6 | |
| ISB1 | CMOS Standby Current (CMOS Inputs) | V _{DD} =V _{DD} (max), (1) 0V ≤ CS2 ≤ 0.2V or (2) $\overline{CS1} \geq V_{DD} - 0.2V$, CS2 ≥ V _{DD} - 0.2V | Com. | 30 | 50 | μA |
| | | | Ind. | - | 65 | μA |
| | | | Auto. | - | 165 | μA |

Note:

Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25°C

AC CHARACTERISTICS⁽⁶⁾ (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|---|---------------|------|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Read Cycle Time | tRC | 45 | - | 55 | - | ns | 1,5 |
| Address Access Time | tAA | - | 45 | - | 55 | ns | 1 |
| Output Hold Time | tOHA | 8 | - | 8 | - | ns | 1 |
| $\overline{CS1}$, CS2 Access Time | tACS1/tACS2 | - | 45 | - | 55 | ns | 1 |
| \overline{OE} Access Time | tDOE | - | 22 | - | 25 | ns | 1 |
| \overline{OE} to High-Z Output | tHZOE | - | 18 | - | 18 | ns | 2 |
| \overline{OE} to Low-Z Output | tLZOE | 5 | - | 5 | - | ns | 2 |
| $\overline{CS1}$, CS2 to High-Z Output | tHZCS//tHZCS2 | - | 18 | - | 18 | ns | 2 |
| $\overline{CS1}$, CS2 to Low-Z Output | tLZCS/tLZCS2 | 10 | - | 10 | - | ns | 2 |

WRITE CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|--------------------------------------|-------------|------|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Write Cycle Time | tWC | 45 | - | 55 | - | ns | 1,3,5 |
| $\overline{CS1}$, CS2 to Write End | tSCS1/tSCS2 | 35 | - | 40 | - | ns | 1,3 |
| Address Setup Time to Write End | tAW | 35 | - | 40 | - | ns | 1,3 |
| Address Hold from Write End | tHA | 0 | - | 0 | - | ns | 1,3 |
| Address Setup Time | tSA | 0 | - | 0 | - | ns | 1,3 |
| \overline{WE} Pulse Width | tPWE | 35 | - | 40 | - | ns | 1,3,4 |
| Data Setup to Write End | tSD | 28 | - | 28 | - | ns | 1,3 |
| Data Hold from Write End | tHD | 0 | - | 0 | - | ns | 1,3 |
| \overline{WE} LOW to High-Z Output | tHZWE | - | 18 | - | 18 | ns | 2,3 |
| \overline{WE} HIGH to Low-Z Output | tLZWE | 10 | - | 10 | - | ns | 2,3 |

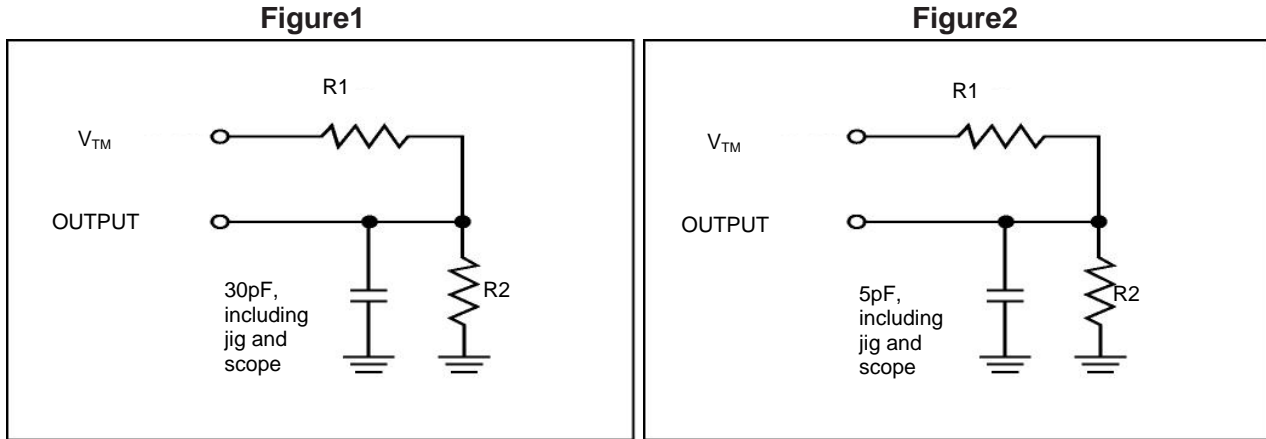
Notes:

1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CS1}$ =LOW, CS2=HIGH, (\overline{UB} or \overline{LB})=LOW, and \overline{WE} =LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

| Parameter | Symbol | Conditions | Units |
|-------------------------------|-------------------------|----------------------|-------|
| Input Rise Time | T_R | 1.0 | V/ns |
| Input Fall Time | T_F | 1.0 | V/ns |
| Output Timing Reference Level | V_{REF} | $\frac{1}{2} V_{TM}$ | V |
| Output Load Conditions | Refer to Figure 1 and 2 | | |

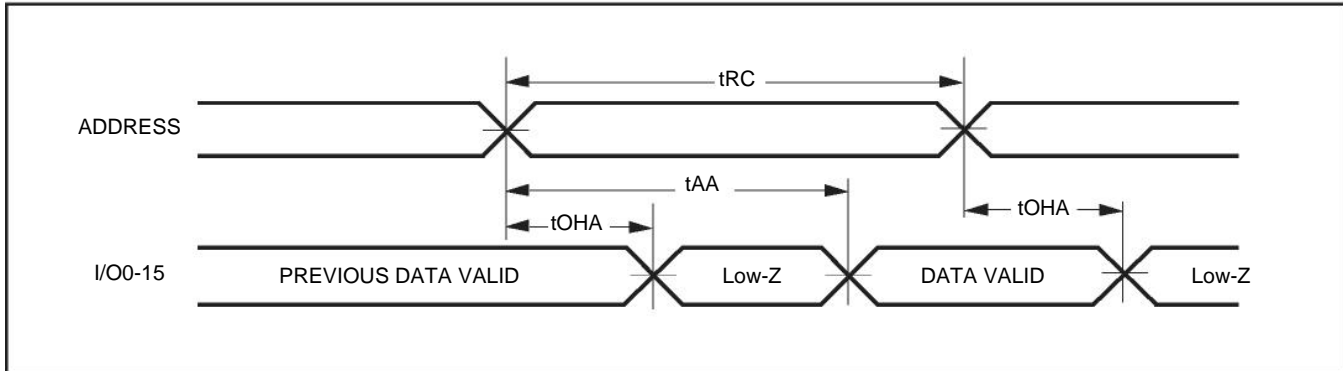
OUTPUT LOAD CONDITIONS FIGURES



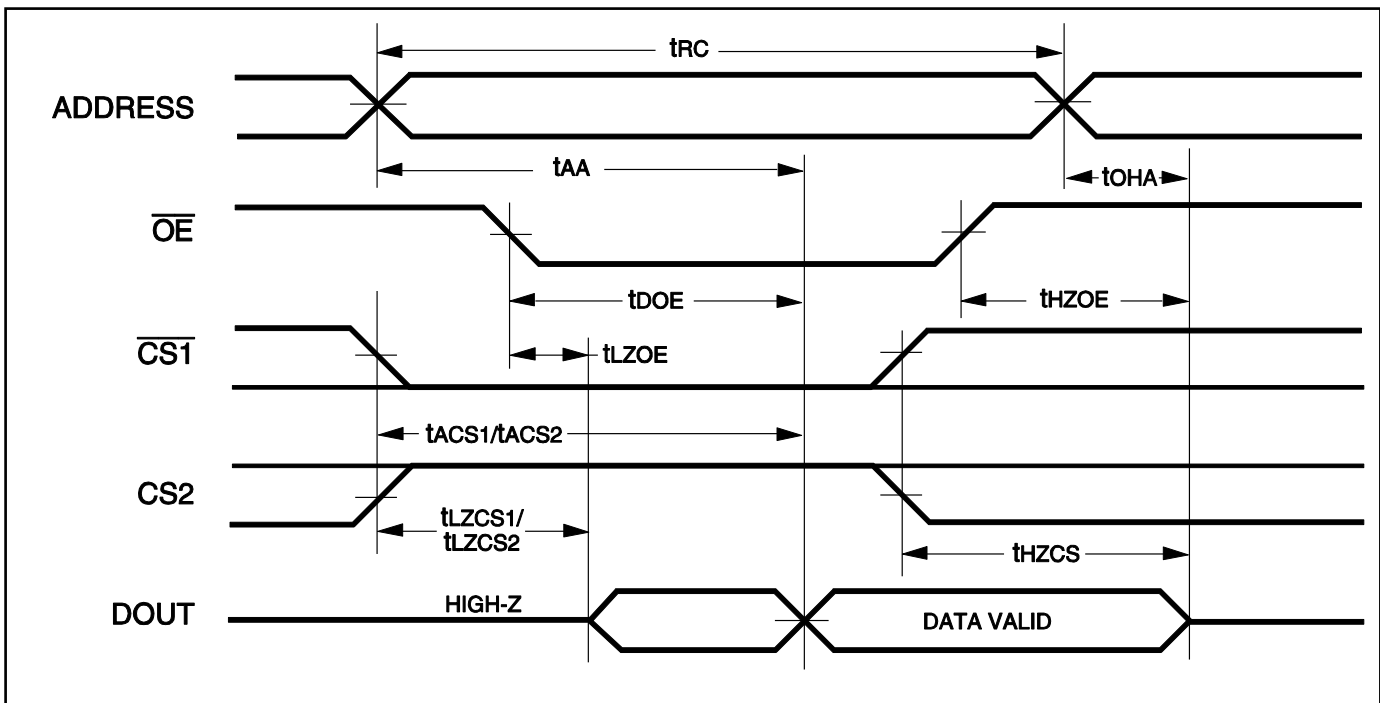
| Parameters | $V_{DD}=1.65\sim 1.98V$ | $V_{DD}=2.2\sim 2.7V$ | $V_{DD}=2.7\sim 3.6V$ |
|------------|-------------------------|-----------------------|-----------------------|
| R1 | 13500 Ω | 16667 Ω | 1103 Ω |
| R2 | 10800 Ω | 15385 Ω | 1554 Ω |
| V_{TM} | VDD | VDD | VDD |

TIMING DIAGRAM

READ CYCLE NO. 1^(1,2) (ADDRESS CONTROLLED) ($\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



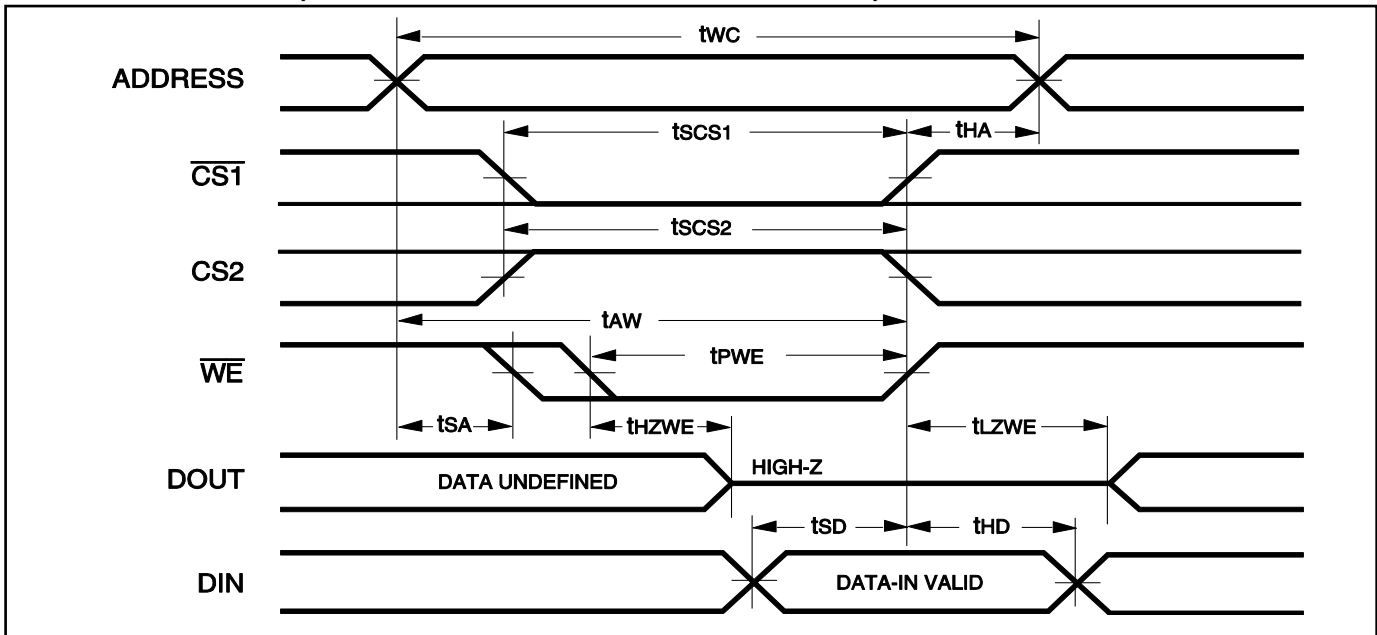
READ CYCLE NO. 2^(1,3) ($\overline{CS1}$, $CS2$, AND \overline{OE} CONTROLLED)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CS1}=V_{IL}$. $CS2=\overline{WE}=V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW and $CS2$ HIGH transition.

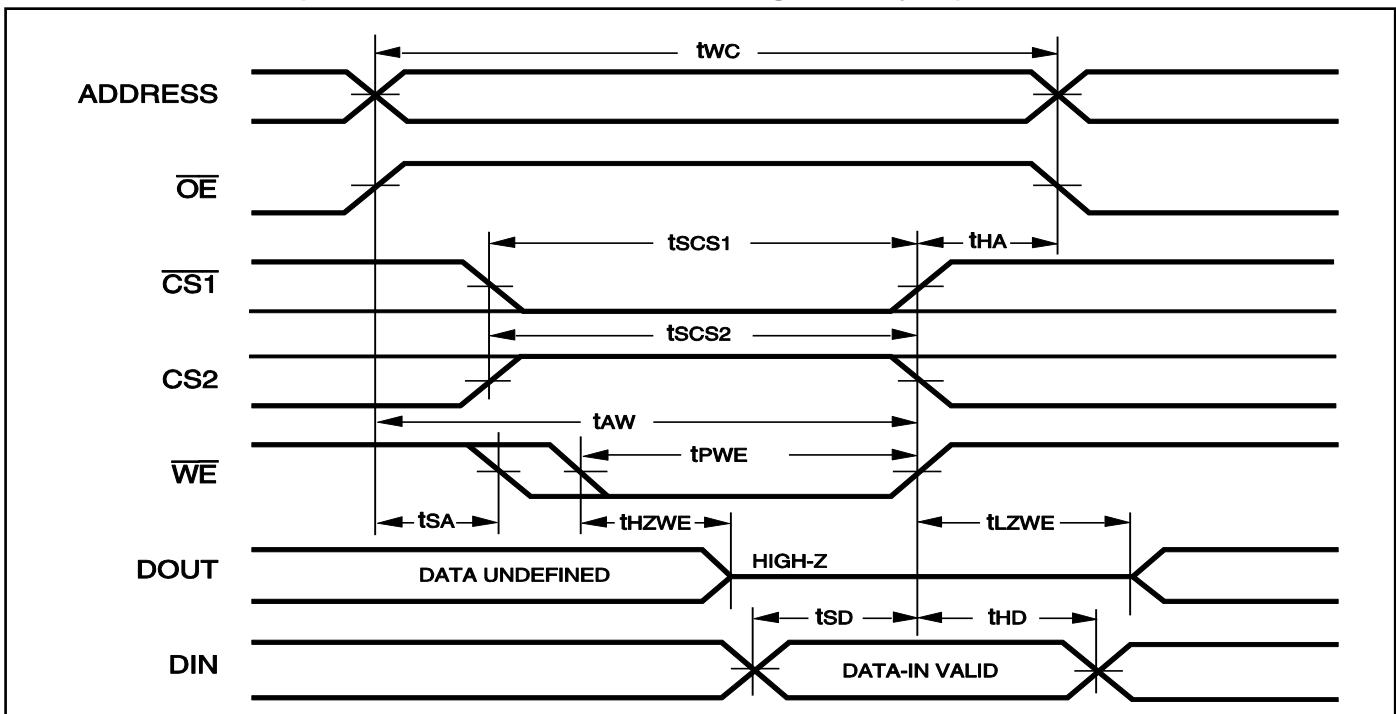
WRITE CYCLE NO. 1 ($\overline{CS1}$ CONTROLLED, \overline{OE} = HIGH OR LOW)



Notes:

1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if \overline{OE} goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after \overline{OE} goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

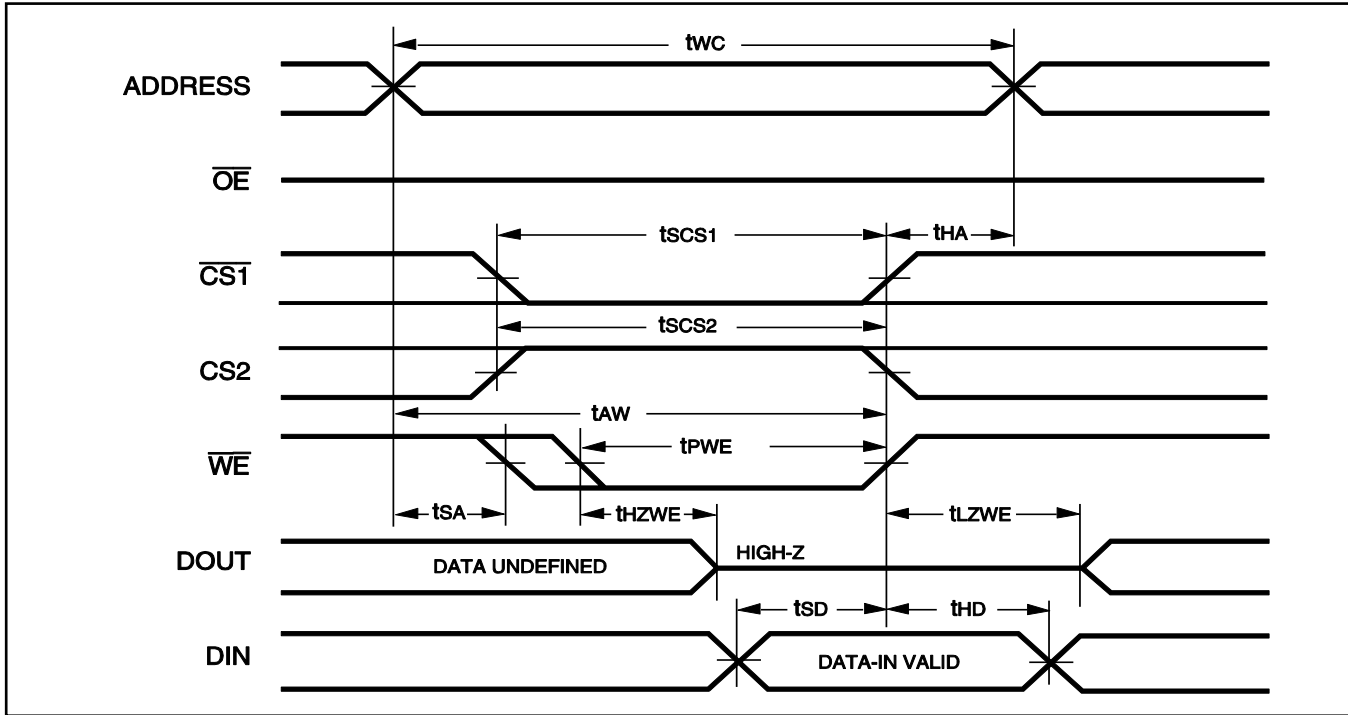
WRITE CYCLE NO. 2 (\overline{WE} Controlled: \overline{OE} is HIGH During Write Cycle)



Notes:

1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if \overline{OE} goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after \overline{OE} goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3 (\overline{WE} CONTROLLED: \overline{OE} IS LOW DURING WRITE CYCLE)



Notes:

If \overline{OE} is low during write cycle, t_{HZWE} must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

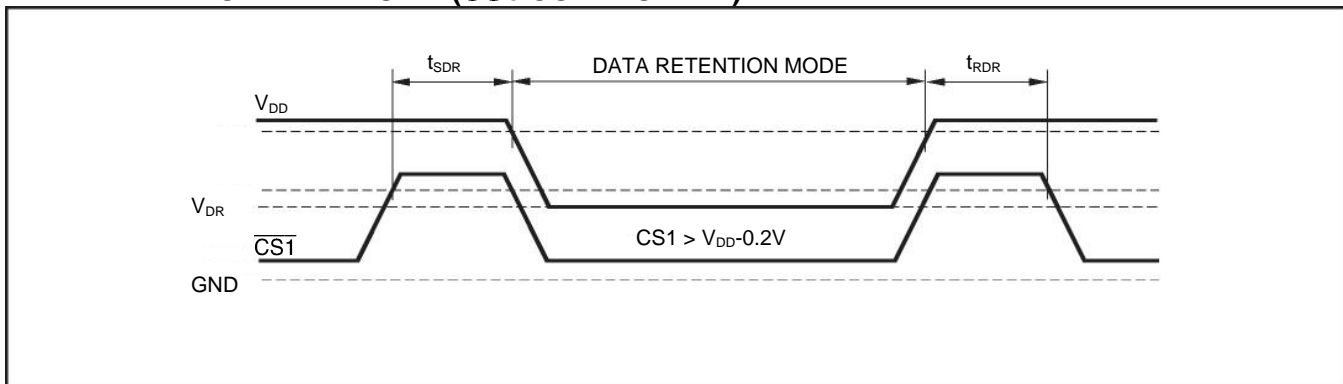
DATA RETENTION CHARACTERISTICS

| Symbol | Parameter | Test Condition | OPTION | Min. | Typ. ⁽²⁾ | Max. | Unit |
|------------------|------------------------------------|--|--------------------|-----------------|---------------------|------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | IS62(5)WV20488EALL | 1.5 | | - | V |
| | | | IS62(5)WV20488EBLL | 1.5 | | - | V |
| I _{DR} | Data Retention Current | V _{DD} = V _{DR} (min), (1) 0V ≤ CS2 ≤ 0.2V, or (2) $\overline{CS1} \geq V_{DD} - 0.2V$, CS2 ≥ V _{DD} - 0.2V | Com. | - | - | 50 | uA |
| | | | Ind. | - | - | 65 | |
| | | | Auto | - | - | 165 | |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | - | - | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | | t _{RC} | - | - | ns |

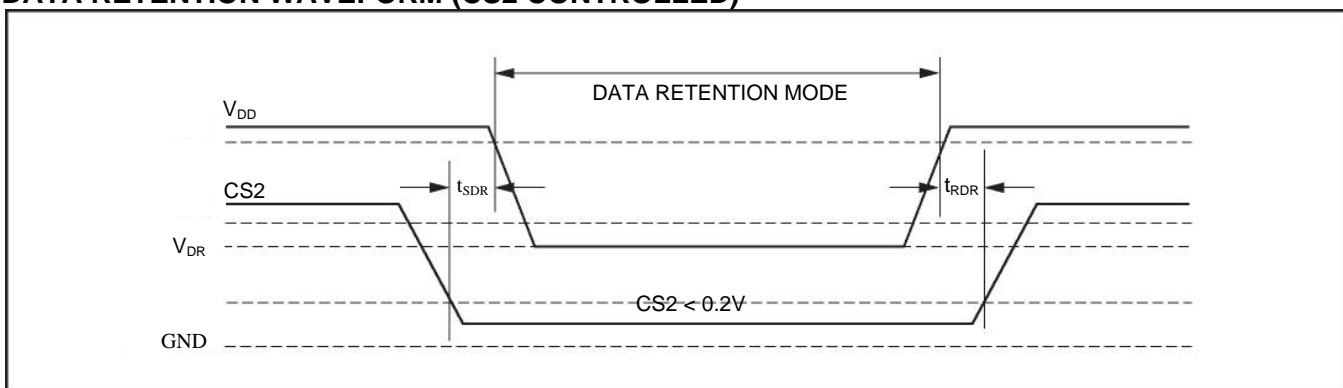
Note:

1. If $\overline{CS1} > V_{DD} - 0.2V$, all other inputs including CS2 must meet this condition.
2. Typical values are measured at V_{DD}=V_{DR}(min), TA = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ CONTROLLED)



DATA RETENTION WAVEFORM (CS2 CONTROLLED)



ORDERING INFORMATION: IS62WV20488EALL

1.65V-1.98V Industrial Range (-40°C to +85°C)

| Speed (ns) | Order Part No | Package |
|------------|-----------------------|--------------------------------------|
| 55 | IS62WV20488EALL-55BI | 48-pin mini BGA (6mmx8mm) |
| | IS62WV20488EALL-55BLI | 48-pin mini BGA (6mmx8mm), Lead-free |

ORDERING INFORMATION: IS62WV20488EBLL

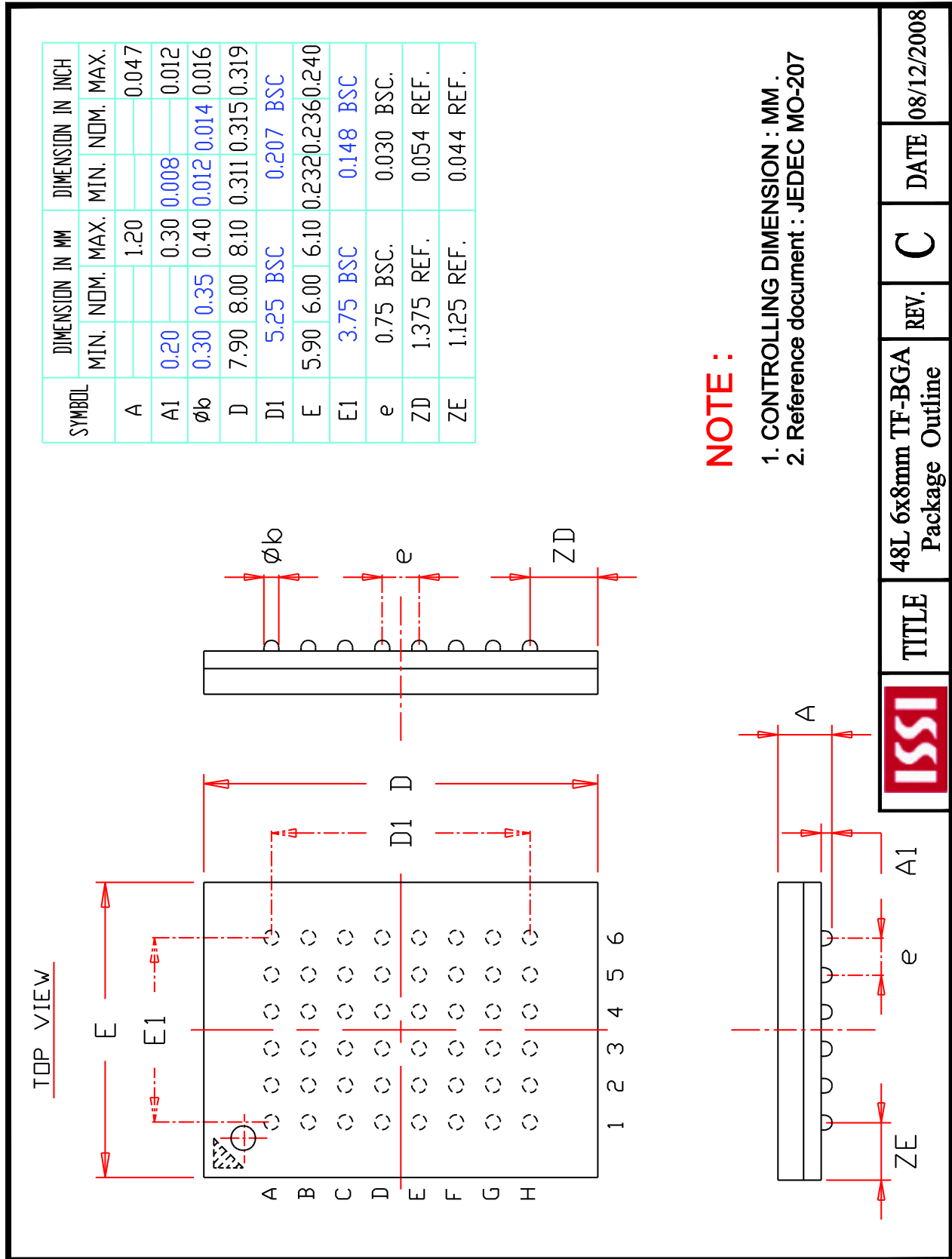
2.2V-3.6V Industrial Range (-40°C to +85°C)

| Speed (ns) | Order Part No | Package |
|------------|-----------------------|--------------------------------------|
| 45 | IS62WV20488EBLL-45BI | 48-pin mini BGA (6mmx8mm) |
| | IS62WV20488EBLL-45BLI | 48-pin mini BGA (6mmx8mm), Lead-free |
| 55 | IS62WV20488EBLL-55BI | 48-pin mini BGA (6mmx8mm) |
| | IS62WV20488EBLL-55BLI | 48-pin mini BGA (6mmx8mm), Lead-free |

ORDERING INFORMATION: IS65WV20488EBLL

2.2V-3.6V Automotive Range (-40°C to +125°C)

| Speed (ns) | Order Part No | Package |
|------------|------------------------|--------------------------------------|
| 55 | IS65WV20488EBLL-55BA3 | 48-pin mini BGA (6mmx8mm) |
| | IS65WV20488EBLL-55BLA3 | 48-pin mini BGA (6mmx8mm), Lead-free |



| SYMBOL | DIMENSION IN MM | | DIMENSION IN INCH | |
|----------|-----------------|------|-------------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.20 | | 0.047 |
| A1 | 0.20 | 0.30 | 0.008 | 0.012 |
| ϕb | 0.30 | 0.40 | 0.012 | 0.016 |
| D | 7.90 | 8.00 | 0.311 | 0.315 |
| D1 | 5.25 | BSC | 0.207 | BSC |
| E | 5.90 | 6.00 | 0.232 | 0.240 |
| E1 | 3.75 | BSC | 0.148 | BSC |
| e | 0.75 | BSC. | 0.030 | BSC. |
| ZD | 1.375 | REF. | 0.054 | REF. |
| ZE | 1.125 | REF. | 0.044 | REF. |

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

| | | | | | | |
|--|-------|-------------------------------------|------|---|------|------------|
| | TITLE | 48L 6x8mm TF-BGA Package Outline | REV. | C | DATE | 08/12/2008 |
|--|-------|-------------------------------------|------|---|------|------------|

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Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

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