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**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

## Features

- Very high speed: 45 ns
  - Wide voltage range: 4.5 V–5.5 V
- Ultra low active power
  - Typical active current: 1.8 mA at  $f = 1$  MHz
  - Typical active current: 18 mA at  $f = f_{max}$
- Ultra low standby power
  - Typical standby current: 2  $\mu$ A
  - Maximum standby current: 8  $\mu$ A
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 44-pin TSOP II package

## Functional Description

The CY62158E MoBL® is a high performance CMOS static RAM organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable

applications. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption significantly when deselected ( $CE_1$  HIGH or  $CE_2$  LOW).

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) input LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

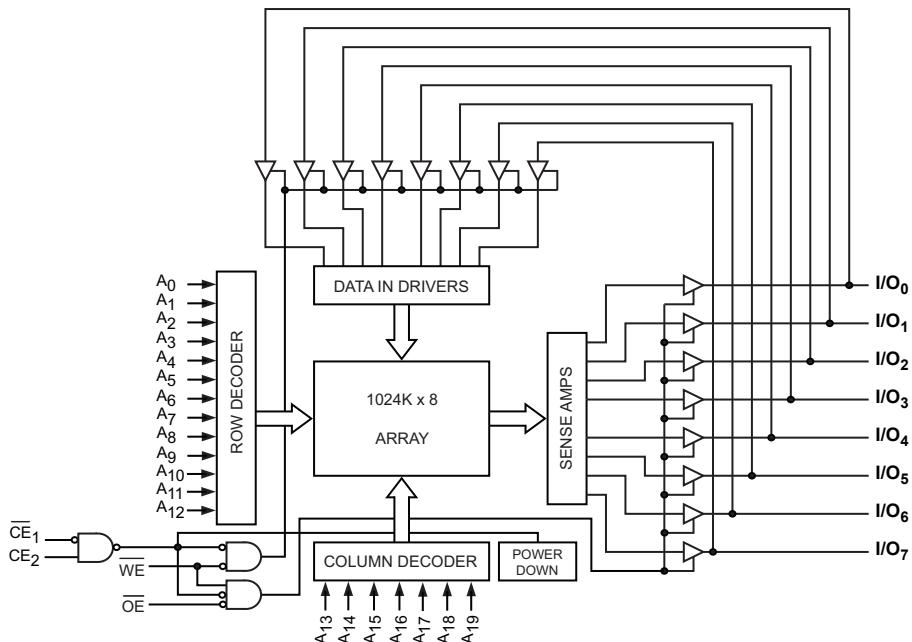
To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and  $\overline{OE}$  LOW while forcing the  $WE$  HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $CE_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $OE$  HIGH), or a write operation is in progress ( $CE_1$  LOW and  $CE_2$  HIGH and  $WE$  LOW). See the [Truth Table on page 11](#) for a complete description of read and write modes.

The CY62158E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram

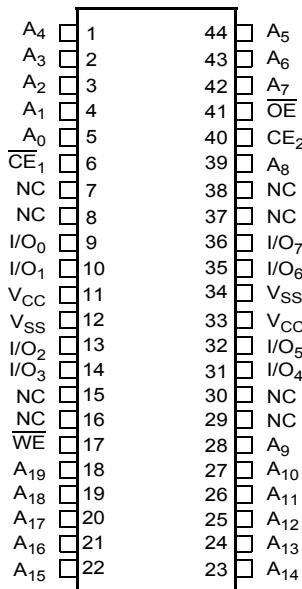


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## Pin Configuration

Figure 1. 44-pin TSOP II pinout (Top View) <sup>[1]</sup>



## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1 MHz		f = f <sub>max</sub>			
	Min	Typ <sup>[2]</sup>	Max		Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62158ELL	4.5	5.0	5.5	45	1.8	3	18	25	2	8

### Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>; T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature  
with Power Applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply Voltage  
to Ground Potential [3, 4] .....  $-0.5\text{ V}$  to  $V_{\text{CC}(\text{max})} + 0.5\text{ V}$

DC Voltage Applied to Outputs  
in High Z State [3, 4] .....  $-0.5\text{ V}$  to  $V_{\text{CC}(\text{max})} + 0.5\text{ V}$

DC Input Voltage [3, 4] .....  $-0.5\text{ V}$  to  $V_{\text{CC}(\text{max})} + 0.5\text{ V}$

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage  
(MIL-STD-883, Method 3015) .....  $> 2001\text{ V}$

Latch up Current .....  $> 200\text{ mA}$

## Operating Range

Device	Range	Ambient Temperature	$V_{\text{CC}}^{[5]}$
CY62158ELL	Industrial	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	4.5 V–5.5 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-45			Unit
		Min	Typ [6]	Max			
$V_{\text{OH}}$	Output HIGH Voltage	$V_{\text{CC}} = 4.5\text{ V}$	$I_{\text{OH}} = -1\text{ mA}$	2.4	–	–	V
		$V_{\text{CC}} = 5.5\text{ V}$	$I_{\text{OH}} = -0.1\text{ mA}$	–	–	3.4 [7]	
$V_{\text{OL}}$	Output LOW Voltage	$I_{\text{OL}} = 2.1\text{ mA}$		–	–	0.4	V
$V_{\text{IH}}$	Input HIGH Voltage	$V_{\text{CC}} = 4.5\text{ V}$ to $5.5\text{ V}$		2.2	–	$V_{\text{CC}} + 0.5\text{ V}$	V
$V_{\text{IL}}$	Input LOW Voltage	$V_{\text{CC}} = 4.5\text{ V}$ to $5.5\text{ V}$		–0.5	–	0.8	V
$I_{\text{IX}}$	Input Leakage Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$		–1	–	+1	$\mu\text{A}$
$I_{\text{OZ}}$	Output Leakage Current	$\text{GND} \leq V_{\text{O}} \leq V_{\text{CC}}$ , Output Disabled		–1	–	+1	$\mu\text{A}$
$I_{\text{CC}}$	$V_{\text{CC}}$ Operating Supply Current	$f = f_{\text{MAX}} = 1/t_{\text{RC}}$	$V_{\text{CC}} = V_{\text{CC}(\text{max})}$	–	18	25	mA
		$f = 1\text{ MHz}$	$I_{\text{OUT}} = 0\text{ mA}$ CMOS levels		1.8	3	mA
$I_{\text{SB1}}$	Automatic CE Power down Current — CMOS Inputs	$\text{CE}_1 \geq V_{\text{CC}} - 0.2\text{ V}$ , $\text{CE}_2 \leq 0.2\text{ V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{ V}$ , $V_{\text{IN}} \leq 0.2\text{ V}$ $f = f_{\text{MAX}}$ (Address and Data Only), $f = 0$ (OE, and WE), $V_{\text{CC}} = V_{\text{CCmax}}$		–	2	8	$\mu\text{A}$
$I_{\text{SB2}}^{[8]}$	Automatic CE Power-down Current — CMOS Inputs	$\text{CE}_1 \geq V_{\text{CC}} - 0.2\text{ V}$ or $\text{CE}_2 \leq 0.2\text{ V}$ , $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{ V}$ or $V_{\text{IN}} \leq 0.2\text{ V}$ , $f = 0$ , $V_{\text{CC}} = V_{\text{CCmax}}$		–	2	8	$\mu\text{A}$

### Notes

3.  $V_{\text{IL}}(\text{min}) = -2.0\text{ V}$  for pulse durations less than 20 ns.
4.  $V_{\text{IH}}(\text{max}) = V_{\text{CC}} + 0.75\text{ V}$  for pulse durations less than 20 ns.
5. Full Device AC operation assumes a 100  $\mu\text{s}$  ramp time from 0 to  $V_{\text{CC}}$  (min) and 200  $\mu\text{s}$  wait time after  $V_{\text{CC}}$  stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{\text{CC}} = V_{\text{CC}(\text{typ})}$ ,  $T_A = 25^{\circ}\text{C}$ .
7. Please note that the maximum  $V_{\text{OH}}$  limit does not exceed minimum CMOS  $V_{\text{IH}}$  of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum  $V_{\text{IH}}$  of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.
8. Chip enables ( $\text{CE}_1$  and  $\text{CE}_2$ ), must be tied to CMOS levels to meet the  $I_{\text{SB1}}$  /  $I_{\text{SB2}}$  /  $I_{\text{CCDR}}$  spec. Other inputs can be left floating.

## Capacitance

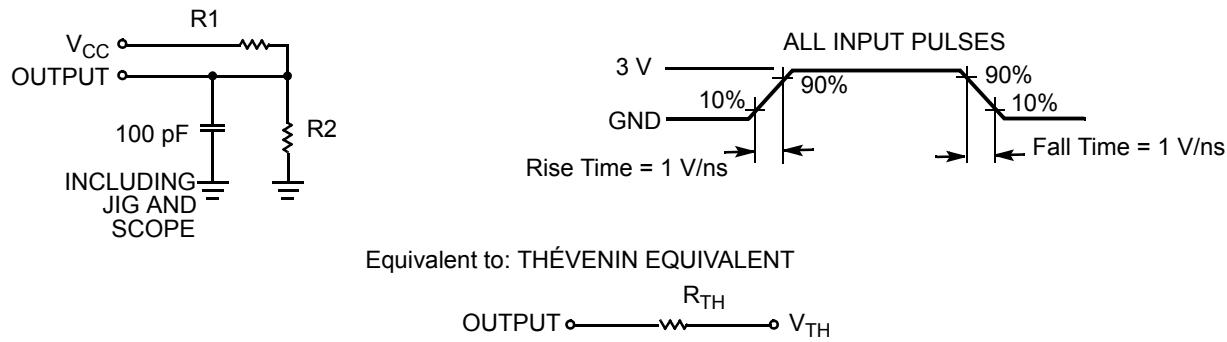
Parameter <sup>[9]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ C$ , $f = 1$ MHz, $V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[9]</sup>	Description	Test Conditions	44-pin TSOP II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	55.84	°C/W
$\Theta_{JC}$	Thermal resistance (junction to case)		15.79	°C/W

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	5.0 V	Unit
R1	1838	$\Omega$
R2	994	$\Omega$
$R_{TH}$	645	$\Omega$
$V_{TH}$	1.75	V

### Note

9. Tested initially and after any design or process changes that may affect these parameters.

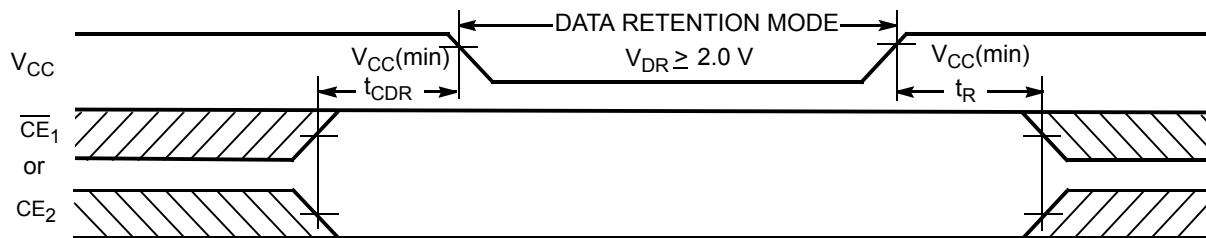
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [10]	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2	—	—	V
$I_{CCDR}$ [11]	Data Retention Current	$V_{CC} = V_{DR}$ $CE_1 \geq V_{CC} - 0.2 \text{ V}$ , $CE_2 \leq 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	—	—	8	$\mu\text{A}$
$t_{CDR}$ [12]	Chip Deselect to Data Retention Time		0	—	—	ns
$t_R$ [13]	Operation Recovery Time		45	—	—	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ})}$ ,  $T_A = 25 \text{ }^\circ\text{C}$ .
11. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ), must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} \geq 100 \mu\text{s}$  or stable at  $V_{CC(\text{min})} \geq 100 \mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	45	–	ns
$t_{AA}$	Address to Data Valid	–	45	ns
$t_{OHA}$	Data Hold from Address Change	10	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid	–	45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid	–	22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z [16]	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z [16, 17]	–	18	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z [16]	10	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to High Z [16, 17]	–	18	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to Power Down	–	45	ns
<b>Write Cycle</b> [18, 19]				
$t_{WC}$	Write Cycle Time	45	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	35	–	ns
$t_{AW}$	Address Setup to Write End	35	–	ns
$t_{HA}$	Address Hold from Write End	0	–	ns
$t_{SA}$	Address Setup to Write Start	0	–	ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35	–	ns
$t_{SD}$	Data Setup to Write End	25	–	ns
$t_{HD}$	Data Hold from Write End	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z [16, 17]	–	18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z [16]	10	–	ns

### Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note [AN66311](#). However, the issue has been fixed and is in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(\text{typ})}/2$ , input pulse levels of 0 to  $V_{CC(\text{typ})}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in [Figure 2 on page 5](#).
16. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of WE,  $CE_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 (WE controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

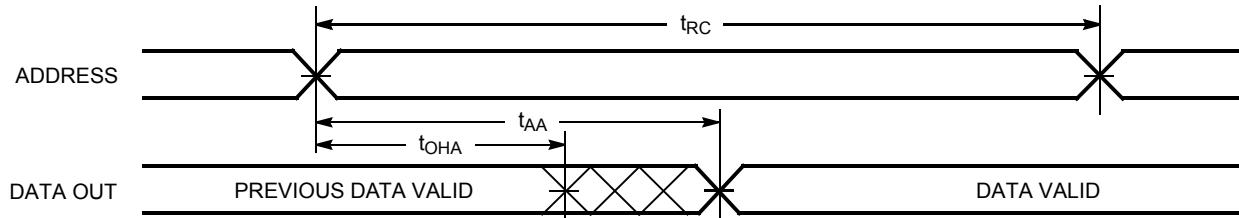
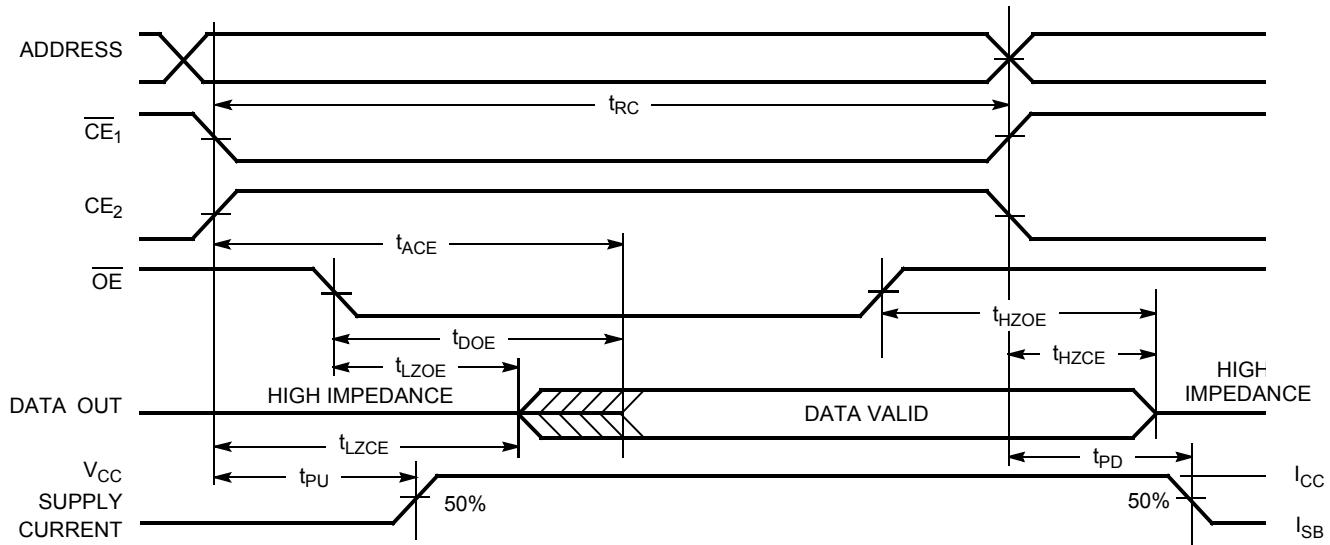


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [21, 22]

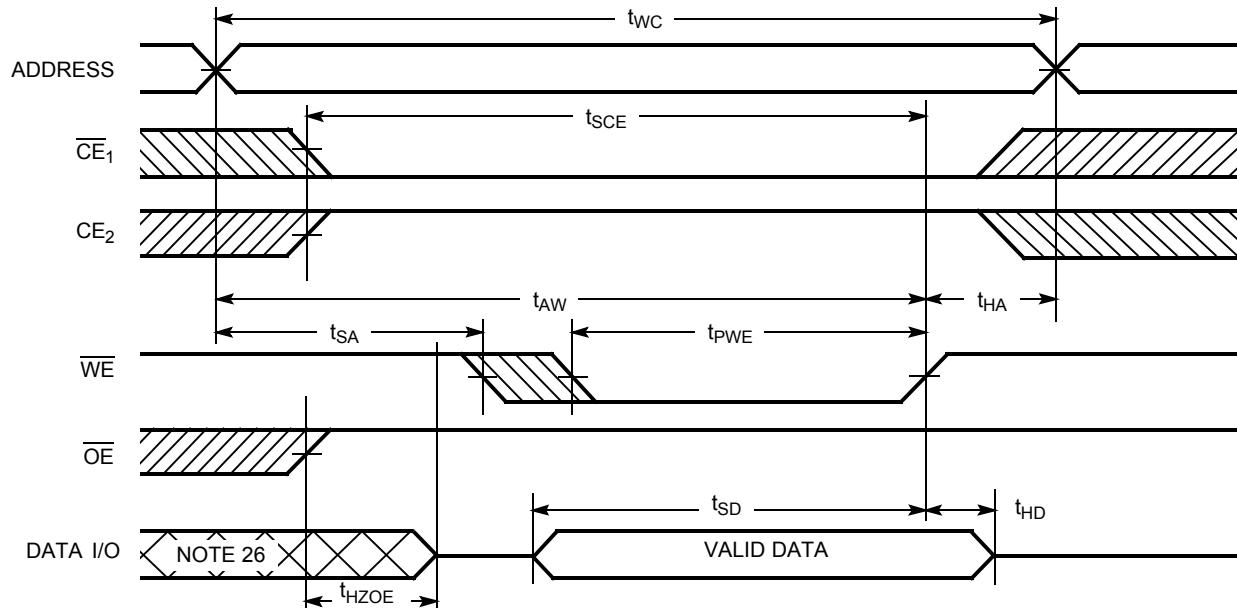


### Notes

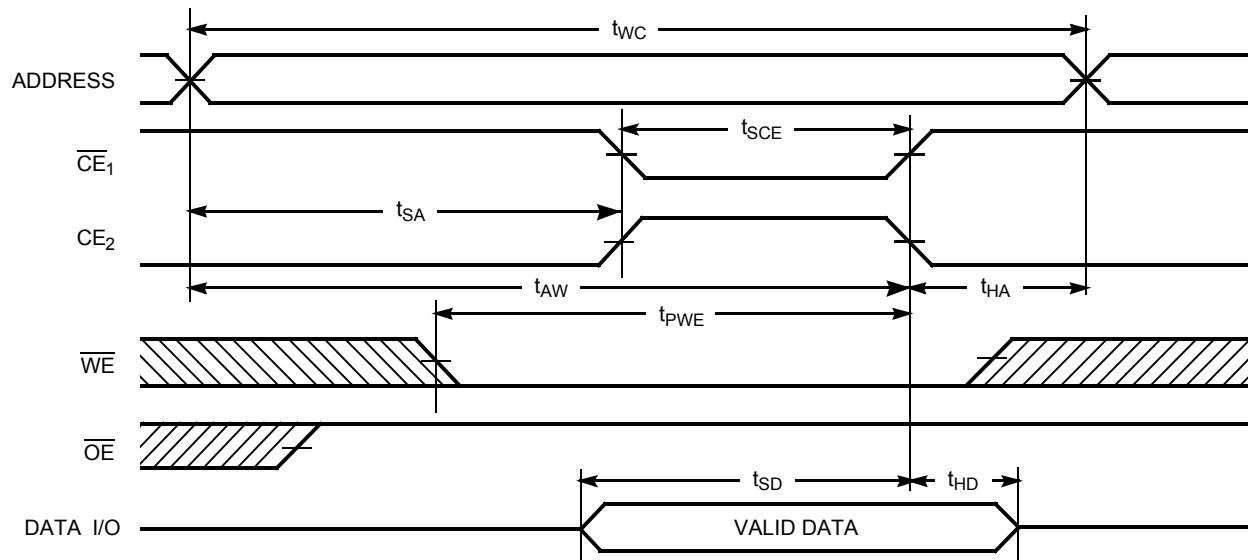
20. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
21.  $WE$  is HIGH for read cycle.
22. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled) [23, 24, 25]**



**Figure 7. Write Cycle No. 2 ( $\overline{CE}_1$  or  $\overline{CE}_2$  Controlled) [23, 24, 25]**

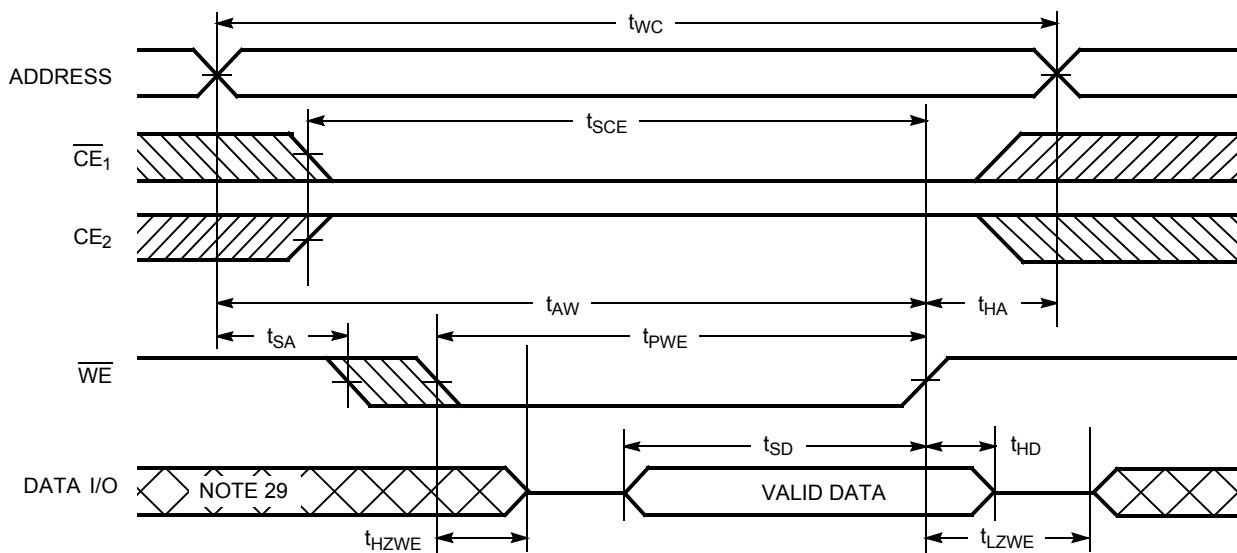


### Notes

23. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $\overline{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
25. If  $\overline{CE}_1$  goes HIGH or  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [27, 28]**



### Notes

27. If  $\overline{\text{CE}}_1$  goes HIGH or  $\overline{\text{CE}}_2$  goes LOW simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in high impedance state.
28. The minimum write cycle pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .
29. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

<b><math>\overline{CE_1}</math></b>	<b><math>\overline{CE_2}</math></b>	<b><math>\overline{WE}</math></b>	<b><math>\overline{OE}</math></b>	<b>Inputs/Outputs</b>	<b>Mode</b>	<b>Power</b>
H	$X^{[30]}$	X	X	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
$X^{[30]}$	L	X	X	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	H	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	H	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	Data in	Write	Active ( $I_{CC}$ )

### Note

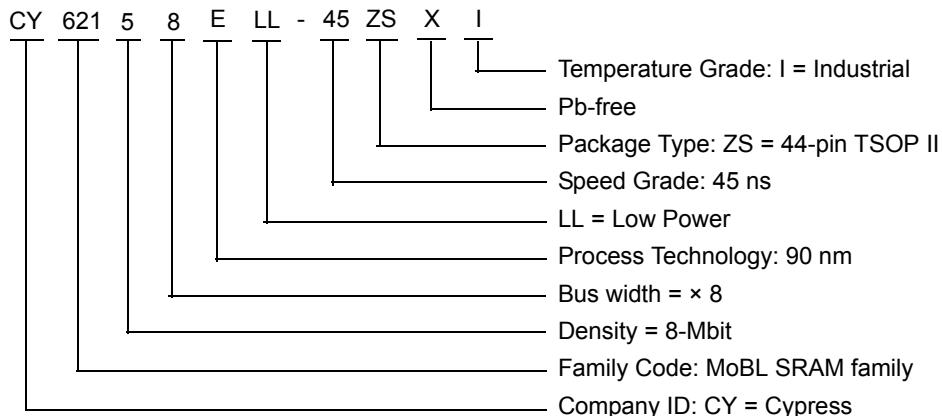
30. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62158ELL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

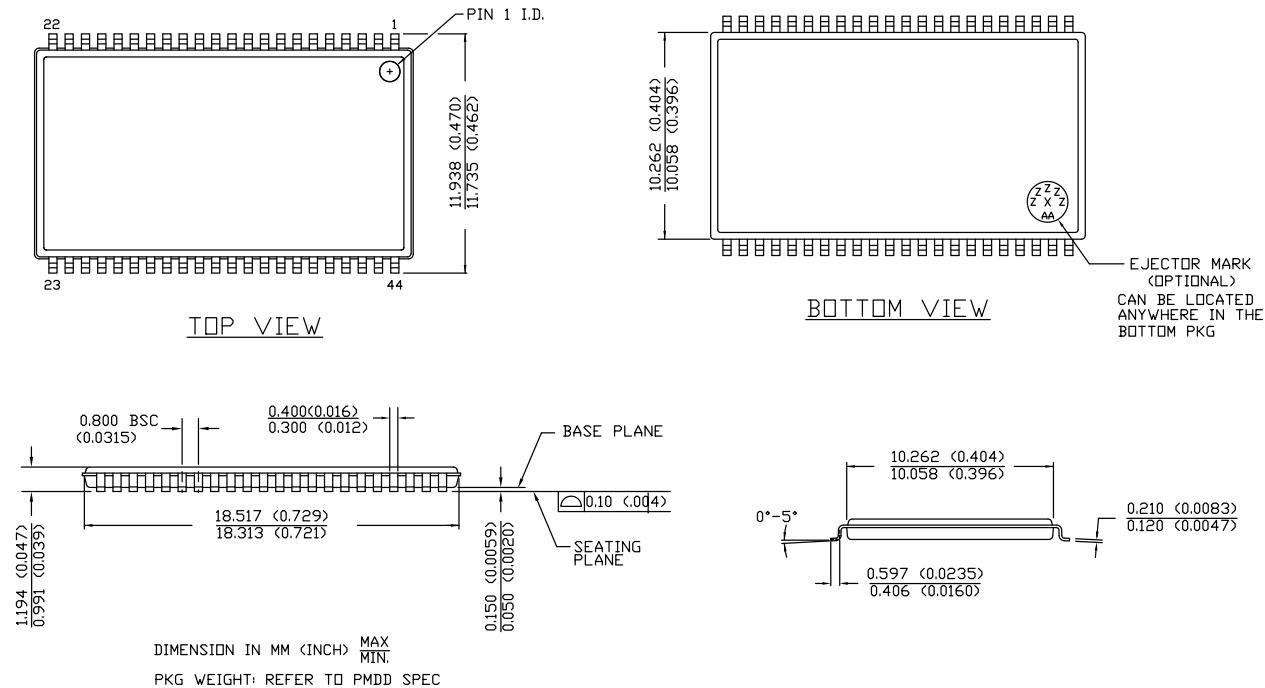
Contact your local Cypress sales representative for availability of this part.

## Ordering Code Definitions



## Package Diagrams

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 \*E

## Acronyms

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
WE	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62158E MoBL®, 8-Mbit (1 M × 8) Static RAM  
 Document Number: 38-05684

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	270350	See ECN	PCI	New data sheet.
*A	291271	See ECN	SYT	Converted from Advance Information to Preliminary Changed input pulse level from $V_{CC}$ to 3V in the AC Test Loads and Waveforms Modified footnote #9 to include timing reference level of 1.5V and input pulse level of 3V
*B	1462592	See ECN	VKN / AESA	Converted from preliminary to final Removed 35 ns speed bin Removed "L" parts Removed 48-Ball VFBGA package Changed $I_{CC(max)}$ spec from 2.3 mA to 3 mA at $f=1$ MHz Changed $I_{CC(typ)}$ spec from 16 mA to 18 mA at $f=f_{MAX}$ Changed $I_{CC(max)}$ spec from 28 mA to 25 mA at $f=f_{MAX}$ Changed $I_{SB1(typ)}$ and $I_{SB2(typ)}$ spec from 0.9 $\mu$ A to 2 $\mu$ A Changed $I_{SB1(max)}$ and $I_{SB2(max)}$ spec from 4.5 $\mu$ A to 8 $\mu$ A Changed $I_{CCDR(max)}$ spec from 4.5 $\mu$ A to 8 $\mu$ A Changed $t_{LZOE}$ spec from 3 ns to 5 ns Changed $t_{LZCE}$ spec from 6 ns to 10 ns Changed $t_{HZCE}$ spec from 22 ns to 18 ns Changed $t_{PWE}$ spec from 30 ns to 35 ns Changed $t_{SD}$ spec from 22 ns to 25 ns Changed $t_{LZWE}$ spec from 6 ns to 10 ns Added footnote# 6 related to $I_{SB2}$ and $I_{CCDR}$ Updated Ordering information table
*C	2428708	See ECN	VKN / PYRS	Corrected typo in the Ordering Information table
*D	2516494	See ECN	PYRS	Corrected ECN number
*E	2934396	06/03/10	VKN	Added footnote #19 related to chip enable Updated package diagram Updated to new template.
*F	3110202	12/14/2010	PRAS	Updated Logic Block Diagram. Added Ordering Code Definitions.
*G	3121955	12/28/2010	SRIH	Updated the missing header and footer in Pg 12.
*H	3279426	06/10/2011	RAME	Updated <a href="#">Functional Description</a> (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines"). Updated <a href="#">Data Retention Characteristics</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*I	4024759	06/10/2013	MEMJ	Updated <a href="#">Functional Description</a> . Updated <a href="#">Electrical Characteristics</a> : Added one more Test Condition " $V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA" for $V_{OH}$ parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for $V_{OH}$ parameter corresponding to Test Condition " $V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA". Updated <a href="#">Package Diagrams</a> : spec 51-85087 – Changed revision from *C to *E.
*J	4099182	08/19/2013	VINI	Updated <a href="#">Switching Characteristics</a> : Added Note 14 and referred the same note in "Parameter" column. Updated to new template.

**Document History Page** (continued)

<b>Document Title:</b> CY62158E MoBL®, 8-Mbit (1 M × 8) Static RAM <b>Document Number:</b> 38-05684				
<b>Rev.</b>	<b>ECN No.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
*K	4575245	11/19/2014	VINI	<p>Updated <a href="#">Functional Description</a>:            Added "For a complete list of related documentation, <a href="#">click here</a>." at the end.</p> <p>Updated <a href="#">Switching Characteristics</a>:            Added Note 19 and referred the same note in "Write Cycle".</p> <p>Updated <a href="#">Switching Waveforms</a>:            Added Note 28 and referred the same note in <a href="#">Figure 8</a>.</p>
*L	4841338	07/20/2015	VINI	<p>Updated <a href="#">Maximum Ratings</a>:            Referred Notes 3, 4 in "Supply Voltage to Ground Potential".</p> <p>Updated <a href="#">Thermal Resistance</a>:            Replaced "two-layer" with "four-layer" in "Test Conditions" column.            Changed value of <math>\Theta_{JA}</math> parameter from 75.13 °C/W to 55.84 °C/W corresponding to 44-pin TSOP II package.            Changed value of <math>\Theta_{JC}</math> parameter from 8.95 °C/W to 15.79 °C/W corresponding to 44-pin TSOP II package.</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a>:            Updated <a href="#">Figure 2</a>:            Replaced "V" with "<math>V_{TH}</math>" in part c.            Updated to new template.            Completing Sunset Review.</p>

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**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

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