OKI Semiconductor

FEDSMS81V26000-02
Issue Date: Dec 15, 2004

MS81V26000

1,114,112-Word × 24-Bit Field Memory

GENERAL DESCRIPTION

The OKI MS81V26000 is a high performance 26-Mbit, 1,100K × 24-bit, Field Memory. It is especially designed for high-speed serial access applications such as HDTVs, conventional NTSC TVs, VTRs, digital movies and Multi-media systems. MS81V26000 is a FRAM for wide or low end use in general commodity TVs and VTRs exclusively. MS81V26000 is not designed for the other use or high end use in medical systems, professional graphics systems which require long term picture storage, data storage systems and others. More than two MS81V26000s can be cascaded directly without any delay devices among the MS81V26000s. (Cascading of MS81V26000 provides larger storage depth or a longer delay).

Each of the 24-bit planes has separate serial write and read ports. These employ independent control clocks to support asynchronous read and write operations. Different clock rates are also supported that allow alternate data rates between write and read data streams.

The MS81V26000 provides high speed FIFO, First-In First-Out, operation without external refreshing: MS81V26000 refreshes its DRAM storage cells automatically, so that it appears fully static to the users.
Moreover, fully static type memory cells and decoders for serial access enable the refresh free serial access operation, so that serial read and/or write control clock can be halted high or low for any duration as long as the power is on. Internal conflicts of memory access and refreshing operations are prevented by special arbitration logic.

The MS81V26000's function is simple, and similar to a digital delay device whose delay-bit-length is easily set by reset timing. The delay length, number of read delay clocks between write and read, is determined by externally controlled write and read reset timings.

Additionally, the MS81V26000 has write mask function or input enable function (IE), and read-data skipping function or output enable function (OE) . The differences between write enable (WE) and input enable (IE), and between read enable (RE) and output enable (OE) are that WE and RE can stop serial write/read address increments, but IE and OE cannot stop the increment, when write/read clocking is continuously applied to MS81V26000. The input enable (IE) function allows the user to write into selected locations of the memory only, leaving the rest of the memory contents unchanged. This facilitates data processing to display a "picture in picture" on a TV screen.

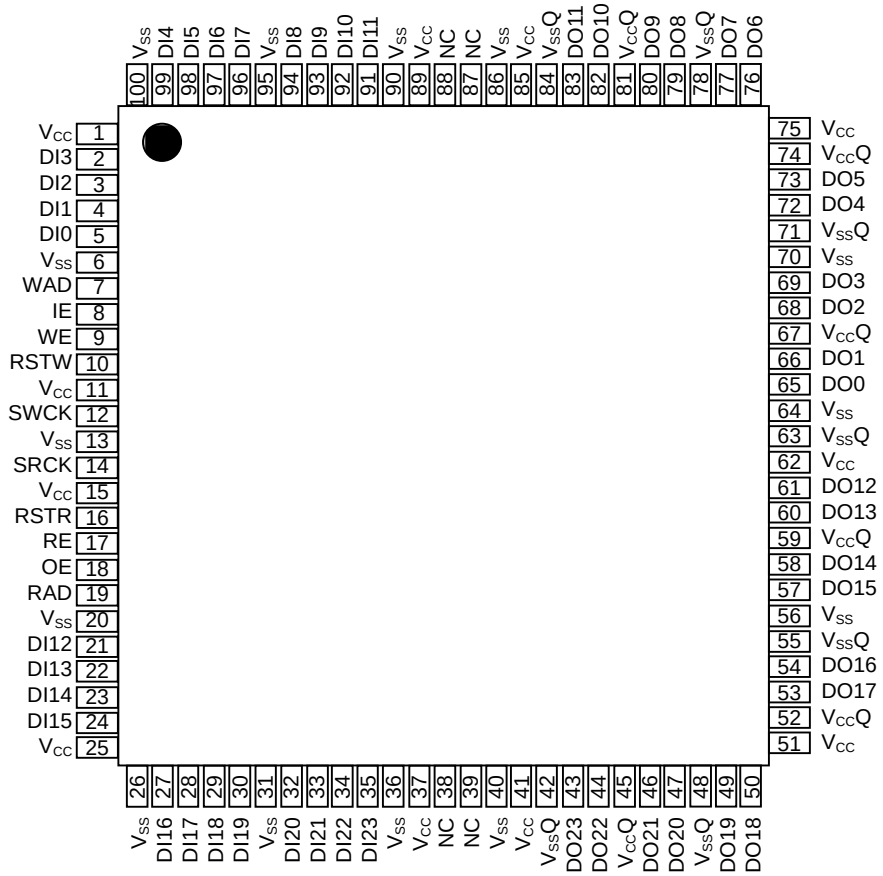
FEATURES

- Single power supply: 3.3 V ±0.3 V
- 1,114,112 words × 24 bits
- Fast FIFO (First-In First-Out) operation
- High speed asynchronous serial access
  - Read/write cycle time 12 ns
  - Access time 9 ns
- Randomly accessible leading address
- Variable length delay bit (350 to 1,114,112)
- Write/Read start address settable
- Write mask function (Input enable control)
- Data skipping function (Output enable control)
- Self refresh (No refresh control is required)
- Package options:
  100-pin plastic TQFP (TQFP100-P-1414-0.50-K) (MS81V26000-xxTB)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)	Cycle Time (Min.)	Package
MS81V26000-12TB	9 ns	12 ns (83 MHz)	100-pin TQFP

PIN CONFIGURATION (TOP VIEW)

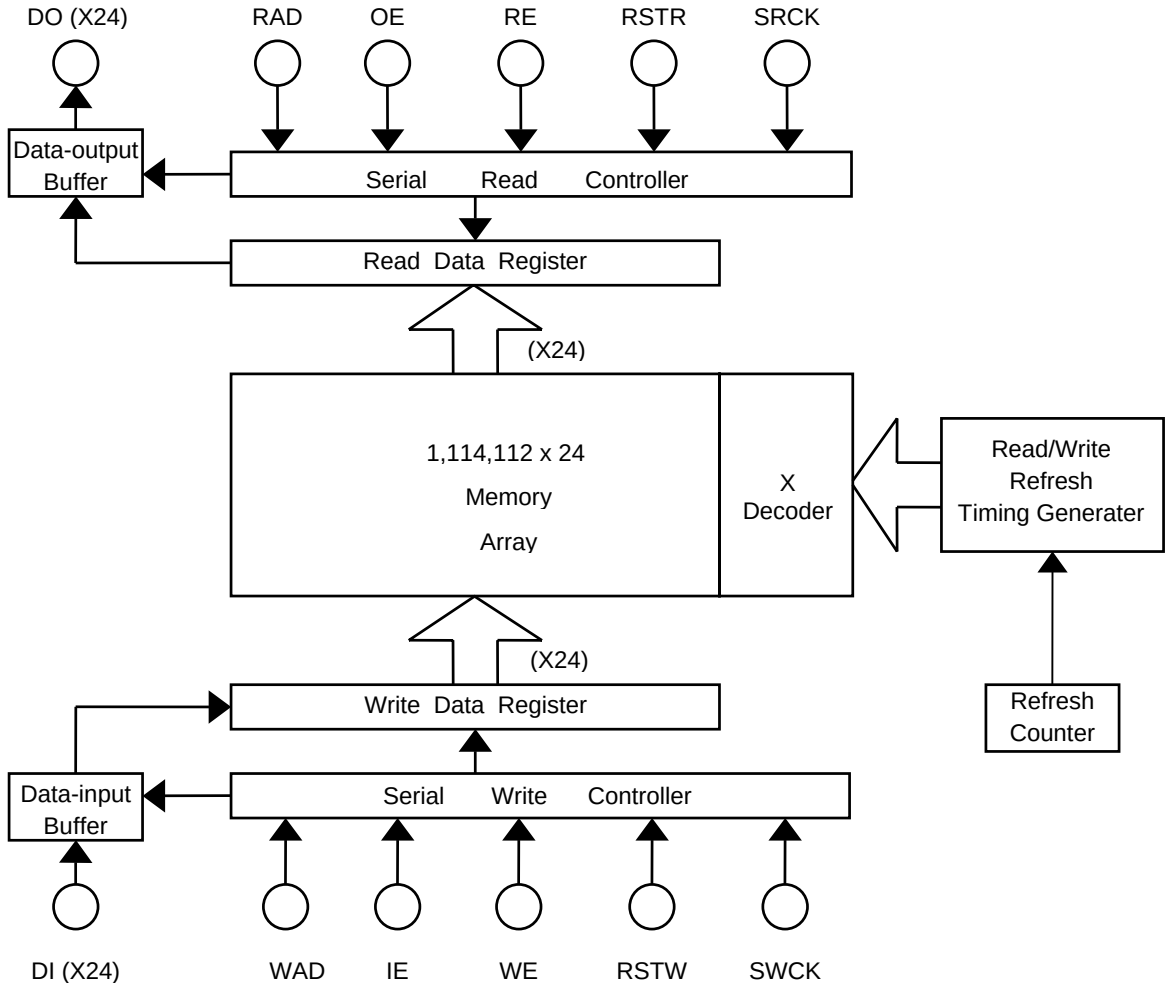


100-Pin TQFP

Pin Name	Function
SWCK	Serial Write Clock
SRCK	Serial Read Clock
WE	Write Enable
RE	Read Enable
IE	Input Enable
OE	Output Enable
RSTW	Write Reset Clock
RSTR	Read Reset Clock
WAD	Write Address Input
RAD	Read Address Input
D_{IN}0 to 23	Data Input
D_{OUT}0 to 23	Data Output
V_{CC}	Power Supply (3.3 V)
V_{SS}	Ground (0 V)
$V_{CC}Q$	Power Supply for output
$V_{SS}Q$	Ground for output
NC	No Connection

Note: The same power supply voltage must be provided to every V_{CC} pin and $V_{CC}Q$ pin, and the same GND voltage level must be provided to every V_{SS} pin and $V_{SS}Q$ pin.

BLOCK DIAGRAM



PIN DESCRIPTION

Serial Write Clock: SWCK
The SWCK latches the input data on chip when WE is high, and also increments the internal write address pointer. Data-in setup time tDS, and hold time tDH are referenced to the rising edge of SWCK.

Write Reset: RSTW
RSTW is used to set the internal write address pointer. RSTW setup and hold times are referenced to the rising edge of SWCK. The SWCK latches the write address data (21bits serial LSB) from WAD.

Write Enable: WE
WE is used for data write enable/disable control. WE high level enables the input, and WE low level disables the input and holds the internal write address pointer. There are no WE disable time (low) and WE enable time (high) restrictions, because the MS81V26000 is in fully static operation as long as the power is on. Note that WE setup and hold times are referenced to the rising edge of SWCK. The latency for the write operation control by WE is 4. After write reset, WE must remain low for more than 1600 ns (tFWD). After write reset, the write operation at address 0 is started after a time tWL form the cycle in which WE is brought high.
After write reset, WE should be remained high for 2 cycles after driving WE high first.

Input Enable: IE
IE is used to enable/disable writing into memory. IE high level enables writing. The internal write address pointer is always incremented by cycling SWCK regardless of the IE level. Note that IE setup and hold times are referenced to the rising edge of SWCK. The latency for the write operation control by IE is 4.

Write Address Input: WAD
These pins are used for write address input.

Data Inputs: (DI0-23)
These pins are used for serial data inputs.

Write Reset: RSTW
RSTW is used to set the internal write address pointer. RSTW setup and hold times are referenced to the rising edge of SWCK. The SWCK latches the write address data (21bits serial LSB) from WAD.

Data Out: (DO0-23)
These pins are used for serial data outputs.

Serial Read Clock: SRCK
Data is shifted out of the data registers. It is triggered by the rising edge of SRCK when RE is high during a read operation. The SRCK input increments the internal read address pointer when RE is high.
The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval tAC that begins with the rising edge of SRCK. *There are no output valid time restriction on MS81V26000.

Read Reset: RSTR
RSTR is used to set the internal read address pointer. RSTR setup and hold times are referenced to the rising edge of SRCK. The SWCK latches the read address data (21bits serial LSB) from RAD.

Read Enable: RE
The function of RE is to gate of the SRCK clock for incrementing the read pointer. When RE is high before the rising edge of SRCK, the read pointer is incremented. When RE is low, the read pointer is not incremented. RE setup times (tRENS and tRDSS) and RE hold times (tRENH and tRDSH) are referenced to the rising edge of the SRCK clock.

The latency for the read operation control by RE is 4. After read reset, RE must remain low for more than 1600 ns (tFRD). After read reset, the read data at address 0 is output after a time tRL from the cycle in which WE is brought high.
After read reset, RE should be remained high for 2 cycles after driving RE high first.

Output Enable: OE
OE is used to enable/disable the outputs. OE high level enables the outputs. The internal read address pointer is always incremented by cycling SRCK regardless of the OE level. Note that OE setup and hold times are referenced to the rising edge of SRCK. The latency for the read operation control by OE is 4.

Read Address Input: RAD
These pins are used for read address input.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditon	Rating	Unit
Power Supply Voltage	V_{CC}	Ta = 25°C	–0.5 to +4.6	V
Input Output Voltage	V_T	at Ta = 25°C, V_{SS}	–0.5 to +4.6	V
Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–55 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	V_{CC}	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	0	+0.8	V

DC Characteristics

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Leakage Current	I_{LI}	$0 < V_I < V_{CC} + 0.3$ V, Other Pins Tested at V = 0 V	–10	+10	µA
Output Leakage Current	I_{LO}	$0 < V_O < V_{CC}$	–10	+10	µA
Output “H” Level Voltage	V_{OH}	I_{OH} = –2 mA	2.4	—	V
Output “L” Level Voltage	V_{OL}	I_{OL} = 2 mA	—	0.4	V
Operating Current	I_{CC1}	Minimum Cycle Time, Output Open	—	200	mA
Standby Current	I_{CC2}	Input Pin = V_{IH}/V_{IL}	—	5	mA

Capacitance

(V_{CC} = 3.3 V ±0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance	C_I	6	pF
Output Capacitance	C_O	7	pF

AC Characteristics

(V_{CC} = 3.3 V ±0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	MS81V26000-12		Unit
		Min.	Max.	
Access Time from SRCK	t_{AC}	—	9	ns
D_{OUT} Hold Time from SRCK	t_{DDCK}	3	—	ns
D_{OUT} Enable Time from SRCK	t_{DECK}	3	9	ns
SWCK “H” Pulse Width	t_{WSWH}	4	—	ns
SWCK “L” Pulse Width	t_{WSWL}	4	—	ns
Input Data Setup Time	t_{DS}	3	—	ns
Input Data Hold Time	t_{DH}	1	—	ns
WE Enable Setup Time	t_{WENS}	3	—	ns
WE Enable Hold Time	t_{WENH}	1	—	ns
WE Disable Setup Time	t_{WDSS}	3	—	ns
WE Disable Hold Time	t_{WDSH}	1	—	ns
IE Enable Setup Time	t_{IENS}	3	—	ns
IE Enable Hold Time	t_{IENH}	1	—	ns
IE Disable Setup Time	t_{IDSS}	3	—	ns
IE Disable Hold Time	t_{IDSH}	1	—	ns
WE “H” Pulse Width	t_{WWEH}	4	—	ns
WE “L” Pulse Width	t_{WWEL}	4	—	ns
IE “H” Pulse Width	t_{WIEH}	4	—	ns
IE “L” Pulse Width	t_{WIEL}	4	—	ns
RSTW Setup Time	t_{RSTWS}	3	—	ns
RSTW Hold Time	t_{RSTWH}	1	—	ns
SRCK “H” Pulse Width	t_{WSRH}	4	—	ns
SRCK “L” Pulse Width	t_{WSRL}	4	—	ns
RE Enable Setup Time	t_{RENS}	3	—	ns
RE Enable Hold Time	t_{RENH}	1	—	ns
RE Disable Setup Time	t_{RDSS}	3	—	ns
RE Disable Hold Time	t_{RDSH}	1	—	ns
OE Enable Setup Time	t_{OENS}	3	—	ns
OE Enable Hold Time	t_{OENH}	1	—	ns
OE Disable Setup Time	t_{ODSS}	3	—	ns
OE Disable Hold Time	t_{ODSH}	1	—	ns
RE “H” Pulse Width	t_{WREH}	4	—	ns
RE “L” Pulse Width	t_{WREL}	4	—	ns
OE “H” Pulse Width	t_{WOEH}	4	—	ns
OE “L” Pulse Width	t_{WOEL}	4	—	ns
RSTR Setup Time	t_{RSTRS}	3	—	ns
RSTR Hold Time	t_{RSTRH}	1	—	ns
SWCK Cycle Time	t_{SWC}	12	—	ns
SRCK Cycle Time	t_{SRC}	12	—	ns
Transition Time (Rise and Fall)	t_T	1	5	ns

Parameter	Symbol	MS81V26000-12		Unit
		Min.	Max.	
WE "L" Period before W Reset	t_{LWE}	4	—	clk
RE "L" Period before R Reset	t_{LRE}	4	—	clk
RE Delay after Reset	t_{FRD}	1,600	—	ns
WE Delay after Reset	t_{FWD}	1,600	—	ns
Write address input period	T_{WAE}	21	—	Clk
Read address input period	T_{RAE}	21	—	clk

Latency

Parameter	Symbol	MS81V26000-12	Unit
Write Latency	t_{WL}	4	clk
Read Latency	t_{RL}	4	clk
WE Write Control Latency	t_{WEL}	4	clk
IE Write Control Latency	t_{IEL}	4	clk
RE Read Control Latency	t_{REL}	4	clk
OE Read Control Latency	t_{OEL}	4	clk

AC Characteristic Measuring Conditions

Output Compare Level	1.4 V
Output Load	1 TTL + 30 pF
Input Signal Level	2.4 V/0.4 V
Input Signal Rise/Fall Time	1 ns
Input Signal Measuring Reference Level	1.4 V

Note: When transition time t_T becomes 1 ns or more, the input signal reference levels for the parameter measurement are V_{IH} (min.) and V_{IL} (max.).

OPERATION MODE

Write Operation Cycle

The write operation is controlled by four control signals, SWCK, RSTW, WE and IE. The write operation is accomplished by cycling SWCK, and holding WE high after the write address pointer reset operation or RSTW. RSTW must be performed for internal circuit initialization before write operation. WE must be low before and after the reset cycle ($t_{LWE} + t_{WAE} + t_{FWD}$).

Each write operation, which begins after RSTW must contain at least 231 active write cycles, i.e., SWCK cycles while WE and IE are high.

Settings of WE and IE to the operation mode of Write address pointer and Data input.

WE	IE	Internal Write address pointer	Data input (Latency 4)
H	H	Incremented	Input
H	L		Not input
L	X	Halted	

X indicates "don't care"

Read Operation Cycle

The read operation is controlled by four control signals, SRCK, RSTR, RE, and OE. The read operation is accomplished by cycling SRCK, and holding both RE and OE high after the read address pointer reset operation or RSTR.

Each read operation, which begins after RSTR, must contain at least 231 active read cycles, i.e., SRCK cycles while RE and OE are high. RE must be low before and after the reset cycle ($t_{LRE} + t_{RAE} + t_{FWD}$).

Settings of RE and OE to the operation mode of read address pointer and Data output.

RE	OE	Internal Read address pointer	Data output (Latency 4)
H	H	Incremented	Output
H	L		High impedance
L	H	Halted	Output
L	L		High impedance

Power-up and Initialization

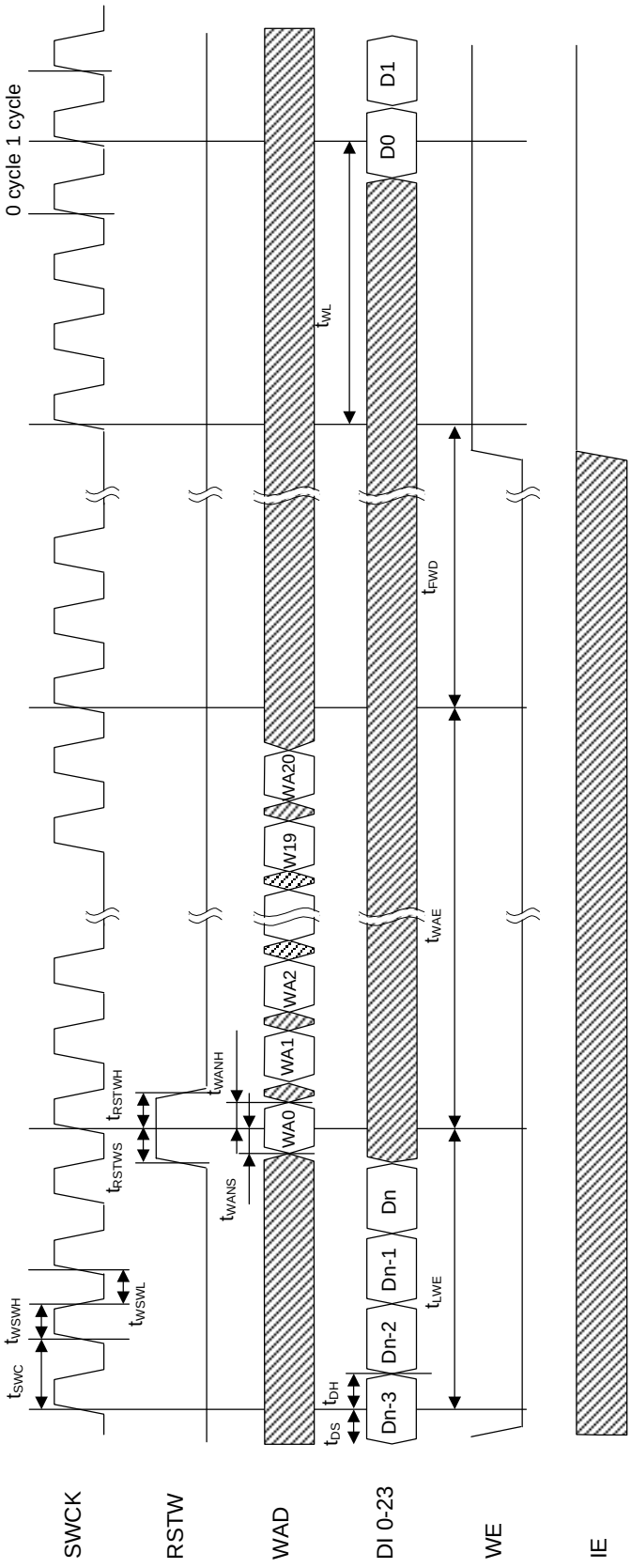
To assure proper operation of this Memory, place an interval of at least 200 µs after Vcc has stabilized to a value within the range of recommended operating conditions after power-up prior to the operation start. After this 200 µs stabilization interval, the following initialization sequence must be performed. Because the read and write address pointers are undefined after power-up, a minimum of 150 dummy write operations (SWCK cycles) and read operations (SRCK cycles) must be performed, followed by an RSTW operation and an RSTR operation, to properly initialize the write and the read address pointer.

New Data Read Access
In order to read out "new data," i.e., to read out data that has been written in a follow-up manner, read reset must be input after write address 150 and the difference between the read address and the write address must be 350 or more but 1,114,111 or less.

Old Data Read Access
In order to read out "old data," i.e., to read out data that was written prior to the write operation being carried out, the difference between the read address and the write address must be 0 or more but 30 or less. If the difference between the read address and the write address is between 31 and 349 or 1,114,112 or more, it is unpredictable whether the new data is output or whether the old data is output. In this case, however, the write data will be written normally.

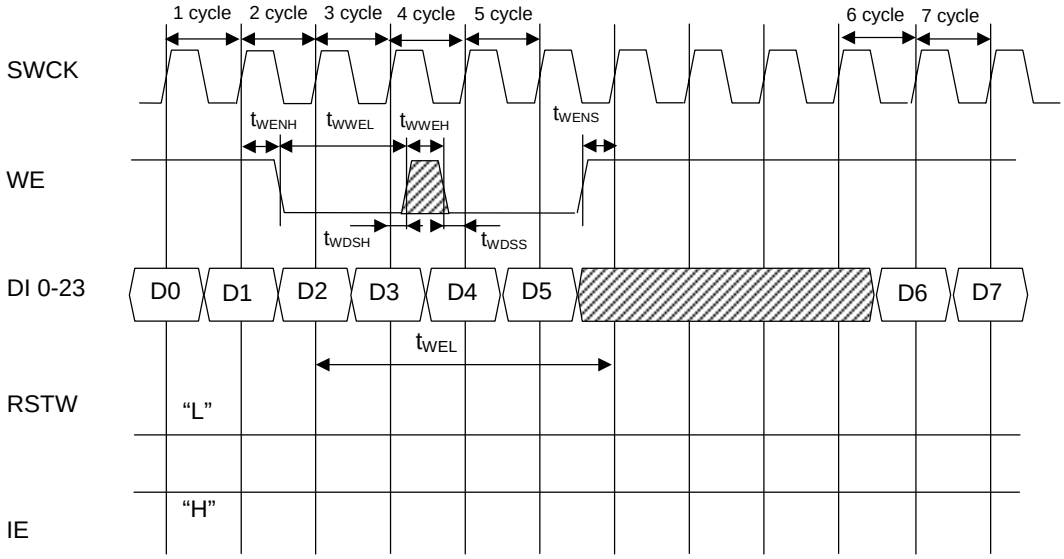
TIMING DIAGRAM

Write Cycle Timing (Write Reset)

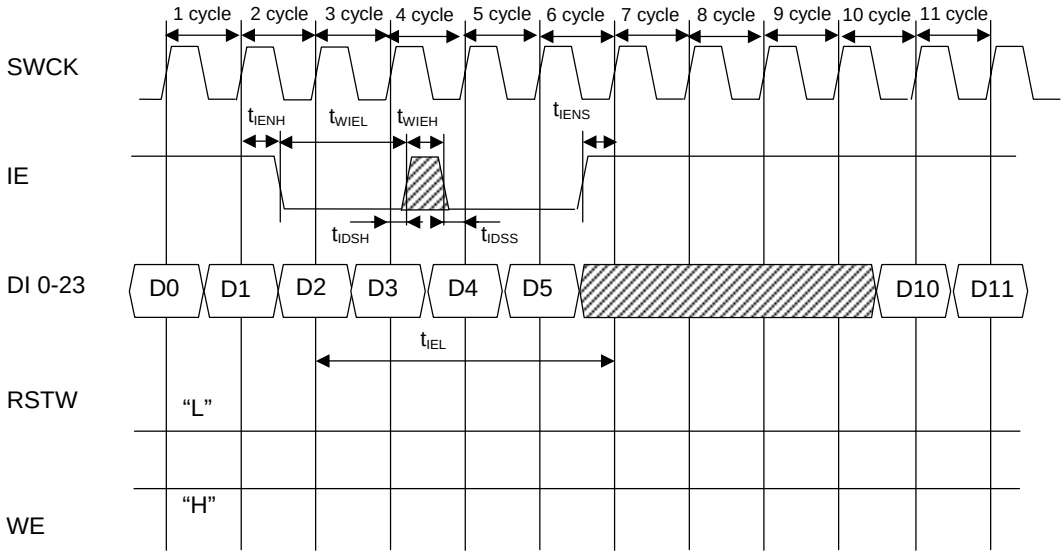


t_{WAE} (=21clk):Period of Address input from Write Reset.
After write reset, WE should be remained high for 2 cycles after driving WE high first.

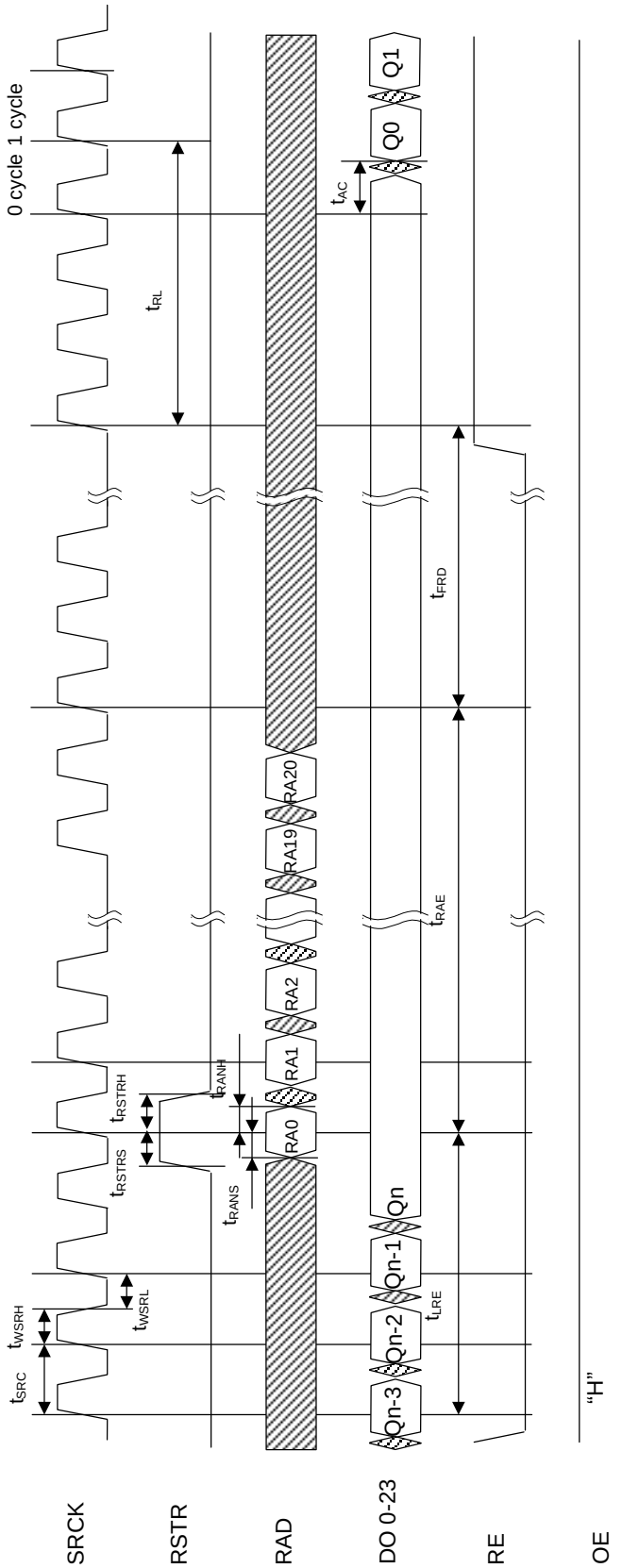
Write Cycle Timing (Write Enable)



Write Cycle Timing (Input Enable)

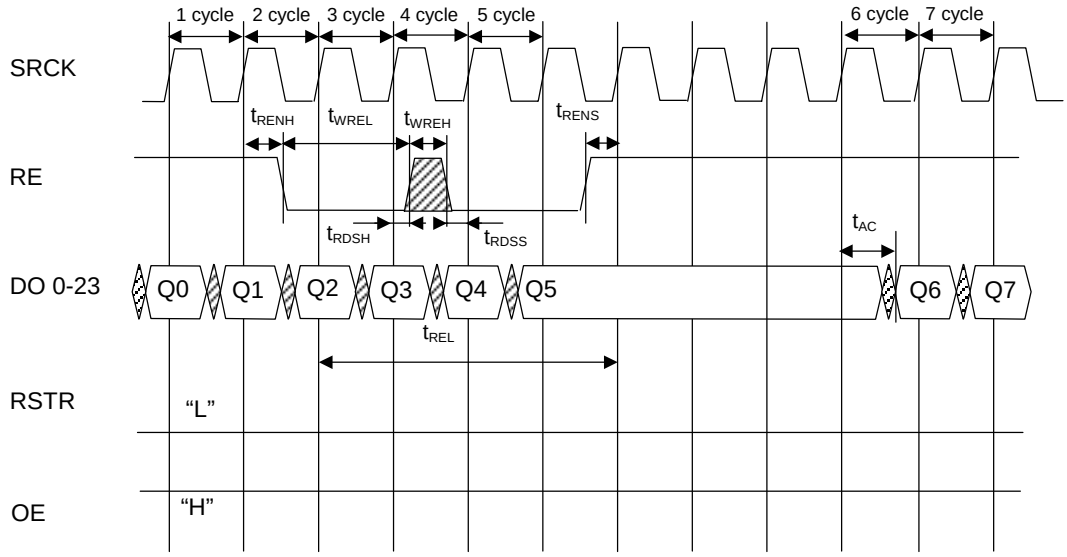


Read Cycle Timing (Read Reset)

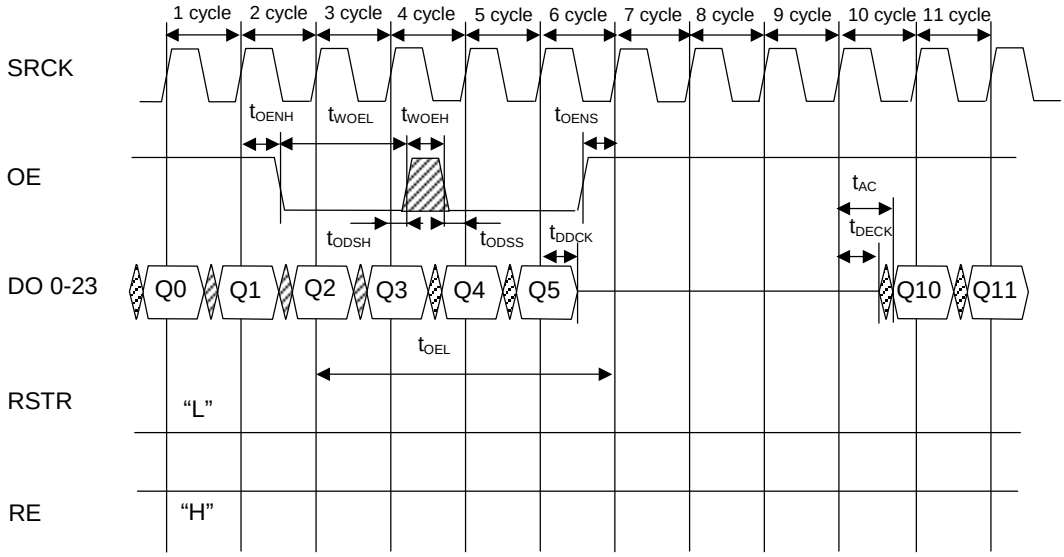


t_{RAE} (=21clk): Period of Address input from Read Reset.
After read reset, RE should be remained high for 2 cycles after driving RE high first.

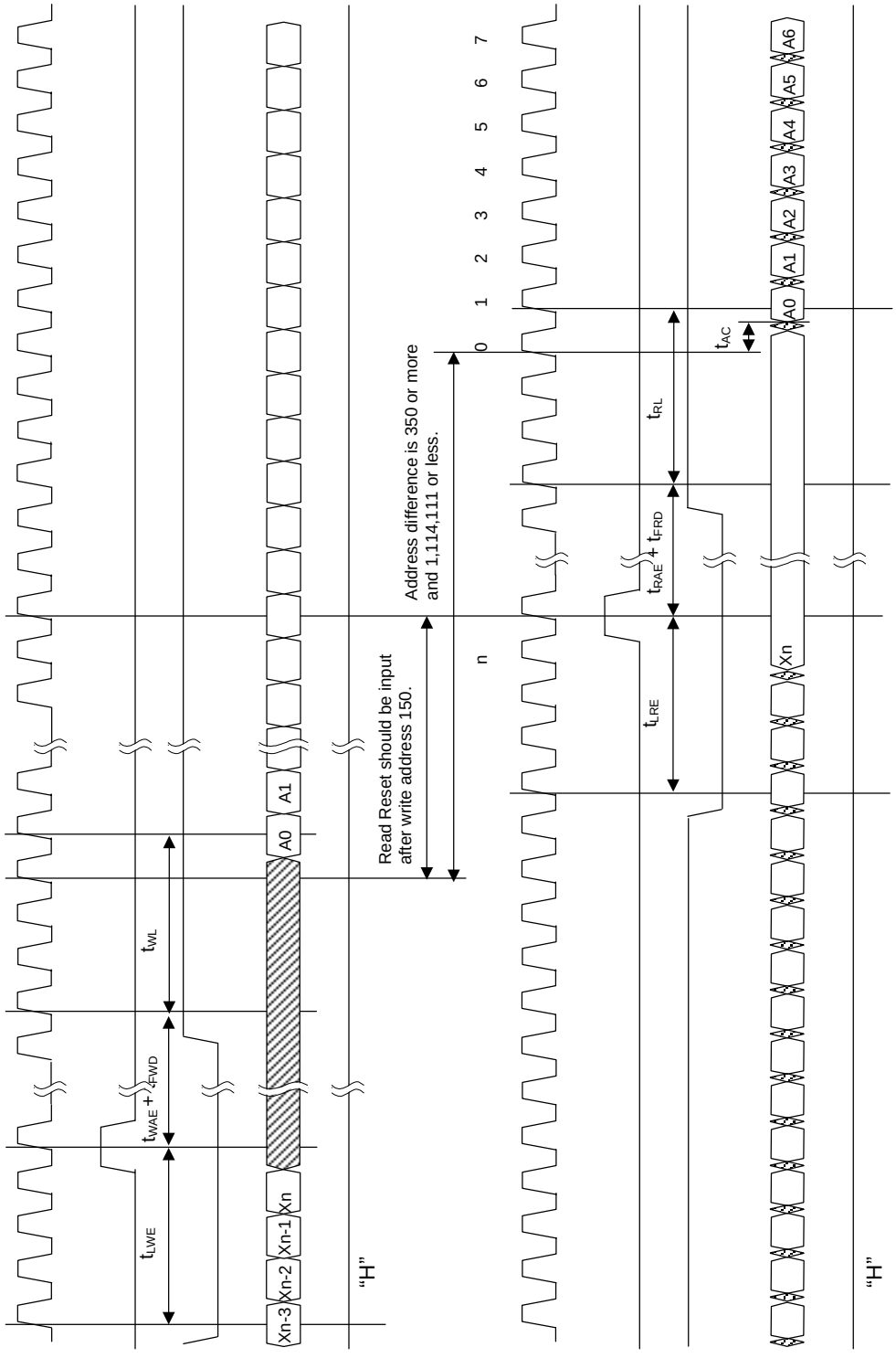
Read Cycle Timing (Read Enable)



Read Cycle Timing (Output Enable)

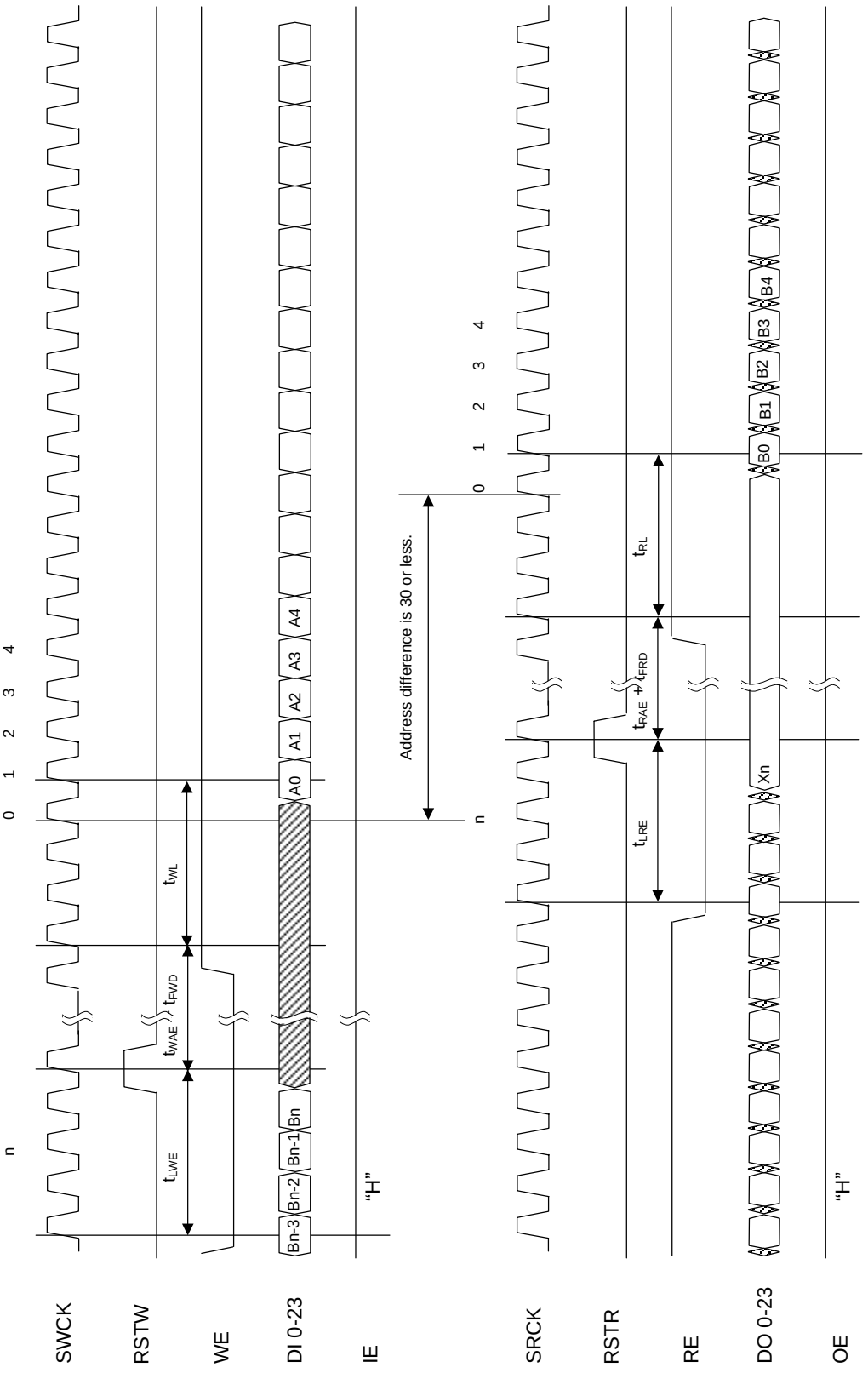


Read / Write Cycle Timing (New Data Read)



The setting address for reading and that for writing are the same.

Read / Write Cycle Timing (Old Data Read)

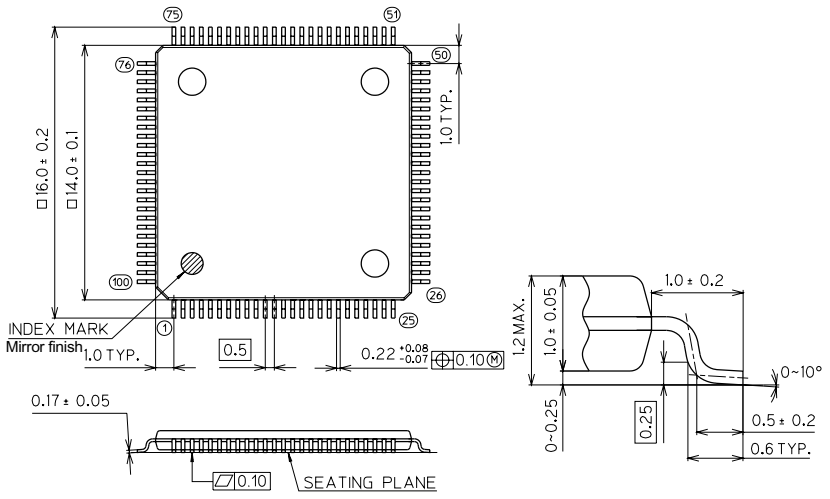


The setting address for reading and that for writing are the same.

PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDS81V26000-01	May 14, 2004	—	—	Final edition 1
FEDS81V26000-01	Dec 15, 2004	20	20	P17 DI0-23 Xn→Bn

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