Fully Accurate 16-Bit V_{OUT} *nano*DAC SPI Interface 2.7 V to 5.5 V in an MSOP

AD5063

FEATURES

Single 16-bit DAC, 1 LSB INL
Power-on reset to midscale
Guaranteed monotonic by design
3 power-down functions
Low power serial interface with Schmitt-triggered inputs
10-lead MSOP, low power
Fast settling time of 1 µs maximum (AD5063-1 model)
2.7 V to 5.5 V power supply
Low glitch on power-up
Unbuffered voltage capable of driving 60 kΩ load
$\overline{\text{SYNC}}$ interrupt facility

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

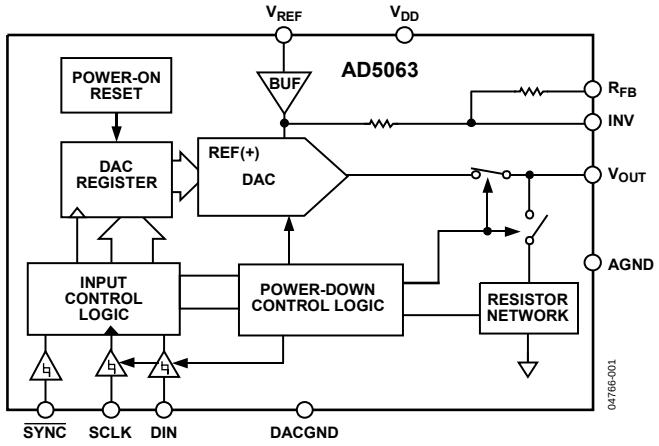

Figure 1.

Table 1. Related Devices

Part No.	Description
AD5061	2.7 V to 5.5 V, 16-bit *nano*DAC D/A, 4 LSBs INL, SOT-23.
AD5062	2.7 V to 5.5 V, 16-bit *nano*DAC D/A, 1 LSB INL, SOT-23.
AD5040/AD5060	2.7 V to 5.5 V, 14-/16-bit *nano*DAC D/A, 1 LSB INL, SOT-23.

GENERAL DESCRIPTION

The AD5063, a member of ADI's *nano*DAC™ family, is a low power, single 16-bit, unbuffered voltage-output DAC that operates from a single 2.7 V to 5 V supply. The part offers a relative accuracy specification of ±1 LSB, and operation is guaranteed monotonic with a ±1 LSB DNL specification. The AD5063 comes with on-board resistors in a 10-lead MSOP, allowing bipolar signals to be generated with an output amplifier. The part uses a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and that is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The reference for the AD5063 is supplied from an external V_{REF} pin. A reference buffer is also provided on-chip. The part incorporates a power-on reset circuit that ensures the DAC output powers up to midscale and remains there until a valid write to the device takes place. The part contains a power-down feature that reduces the current consumption of the device to typically 300 nA at 5 V and provides software-selectable output loads while in power-down mode. The part is put into power-down mode via the serial interface. Total unadjusted error for the part is <1 mV.

This part exhibits very low glitch on power-up.

PRODUCT HIGHLIGHTS

Available in 10-lead MSOP.

16-bit accurate, 1 LSB INL.

Low glitch on power-up.

High speed serial interface with clock speeds up to 30 MHz.

Three power-down modes available to the user.

Rev. C
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REVISION HISTORY

8/09—Rev. B to Rev. C

Changes to Features Section ... 1
Changes to Output Voltage Settling Time Parameter, Table 2 ... 3
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3/06—Rev. A to Rev. B

Updated Format ... Universal
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7/05—Rev. 0 to Rev. A

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4/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, V_{REF} = 4.096 V @ V_{DD} = 5.0 V, R_L = unloaded, C_L = unloaded to GND; T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	B Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE					
Resolution	16			Bits	
Relative Accuracy (INL)		±0.5	±1	LSB	−40°C to + 85°C, B grade over all codes
Total Unadjusted Error (TUE)		±500	±800	µV	
Differential Nonlinearity (DNL)		±0.5	±1	LSB	Guaranteed monotonic
Gain Error		±0.01	±0.02	% FSR	T_A = −40°C to +85°C
Gain Error Temperature Coefficient		1		ppm FSR/°C	
Zero-Code Error		±0.05	±0.1	mV	All 0s loaded to DAC register, T_A = −40°C to +85°C
Zero-Code Error Temperature Coefficient		0.05		µV/°C	
Offset Error		±0.05	±0.1	mV	T_A = −40°C to +85°C
Offset Error Temperature Coefficient		0.5		µV/°C	
Full-Scale Error		±500	±800	µV	All 1s loaded to DAC register, T_A = −40°C to +85°C
Bipolar Resistor Matching		1		Ω/Ω	R_{FB}/R_{INV}, $R_{FB} = R_{INV}$ = 30 kΩ typically
Bipolar Zero Offset Error		±8	±16	LSB	
Bipolar Zero Temperature Coefficient		±0.5		ppm FSR/°C	
Bipolar Gain Error		±16	±32	LSB	
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range	0		V_{REF}	V	Unipolar operation
	$-V_{REF}$		V_{REF}	V	Bipolar operation
Output Voltage Settling Time[3]					¼ scale to ¾ scale code transition to ±1 LSB
AD5063BRMZ		4		µs	
AD5063BRMZ-1			1	µs	V_{DD} = 4.5 V to 5.5 V
		4		µs	V_{DD} = 2.7 V to 5.5 V
Output Noise Spectral Density		64		nV/√Hz	DAC code = midscale, 1 kHz
Output Voltage Noise		6		µV p-p	DAC code = midscale, 0.1 Hz to 10 Hz bandwidth
Digital-to-Analog Glitch Impulse		2		nV-s	1 LSB change around major carry
Digital Feedthrough		0.002		nV-s	
DC Output Impedance (Normal)		8		kΩ	Output impedance tolerance ±10%
DC Output Impedance (Power-Down)					
(Output Connected to 1 kΩ Network)		1		kΩ	Output impedance tolerance ±400 Ω
(Output Connected to 10 kΩ Network)		100		kΩ	Output impedance tolerance ±20 kΩ
REFERENCE INPUT/OUPUT					
V_{REF} Input Range	2		V_{DD} − 50 mV		
Input Current (Power-Down)		±1		µA	Zero-scale loaded
Input Current (Normal)			±1	µA	
DC Input Impedance		1		MΩ	Bipolar/unipolar operation
LOGIC INPUTS					
Input Current[4]		±1	±2	µA	
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 4.5 V to 5.5 V
			0.8		V_{DD} = 2.7 V to 3.6 V
Input High Voltage, V_{IH}	2.0			V	V_{DD} = 2.7 V to 5.5 V
	1.8				V_{DD} = 2.7 V to 3.6 V
Pin Capacitance		4		pF	

Parameter	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	All digital inputs at 0 V or V_{DD}
I_{DD} (Normal Mode)					DAC active and excluding load current
V_{DD} = 4.5 V to 5.5 V		0.65	0.7	mA	$V_{IN} = V_{DD}$ and V_{IL} = GND, V_{DD} = 5 V, V_{REF} = 4.096 V, code = midscale
V_{DD} = 2.7 V to 3.6 V		0.5		mA	$V_{IH} = V_{DD}$ and V_{IL} = GND, V_{DD} = 3 V
I_{DD} (All Power-Down Modes)					
V_{DD} = 4.5 V to 5.5 V			1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V			1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
Power Supply Rejection Ratio (PSRR)		0.5		LSB	$\Delta V_{DD} \pm 10\%$, V_{DD} = 5 V, unloaded

[1] Temperature ranges for the B version: −40°C to +85°C, typical at +25°C, functional to +125°C.
[2] Guaranteed by design and characterization, not production tested.
[3] See the Ordering Guide.
[4] Total current flowing into all pins.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit[1]	Unit	Test Conditions/Comments
t_1[2]	33	ns min	SCLK cycle time
t_2	5	ns min	SCLK high time
t_3	3	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	3	ns min	Data setup time
t_6	2	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	12	ns min	Minimum $\overline{SYNC}$ high time
t_9	9	ns min	$\overline{SYNC}$ rising edge to next SCLK fall ignore

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Maximum SCLK frequency is 30 MHz.

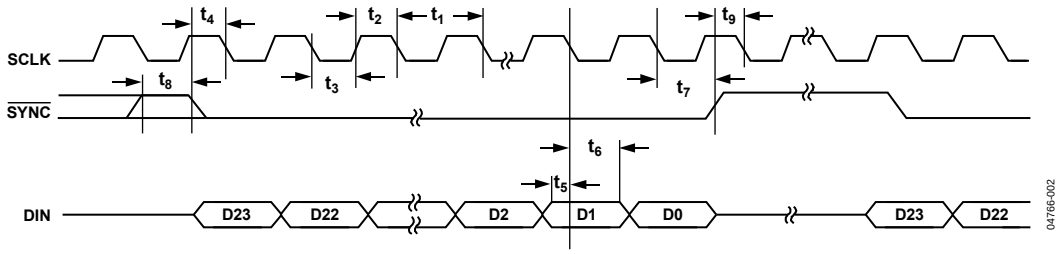


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
INV to GND	−0.3 V to V_{DD} + 0.3 V
R_{FB} to GND	+7 V to −7 V
Operating Temperature Range	
Industrial (B Version)	−40°C to + 85°C[1]
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
MSOP Package	
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260(0/−5)°C
Time at Peak Temperature	10 sec to 40 sec
ESD	1.5 kV

[1] Temperature range for this device is −40°C to +85°C; however, the device is still operational at 125°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

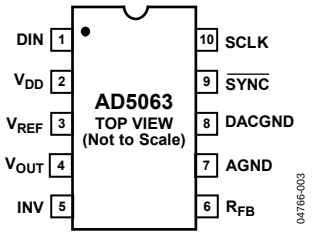


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DIN	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
2	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and V_{DD} should be decoupled to GND.
3	V_{REF}	Reference Voltage Input.
4	V_{OUT}	Analog Output Voltage from DAC.
5	INV	Connected to the Internal Scaling Resistors of the DAC. Connect the INV pin to the external op amp's inverting input in bipolar mode.
6	R_{FB}	Feedback Resistor. In bipolar mode, connect this pin to the external op amp circuit.
7	AGND	Ground Reference Point for Analog Circuitry.
8	DACGND	Ground Input to the DAC.
9	$\overline{\text{SYNC}}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and data is then transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless $\overline{\text{SYNC}}$ is taken high before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC.
10	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 30 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

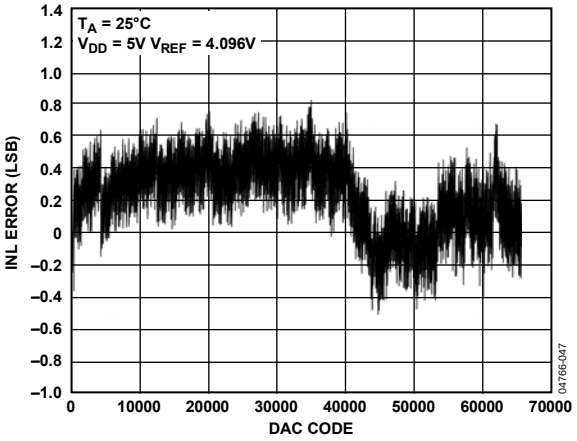


Figure 4. INL Error vs. DAC Code

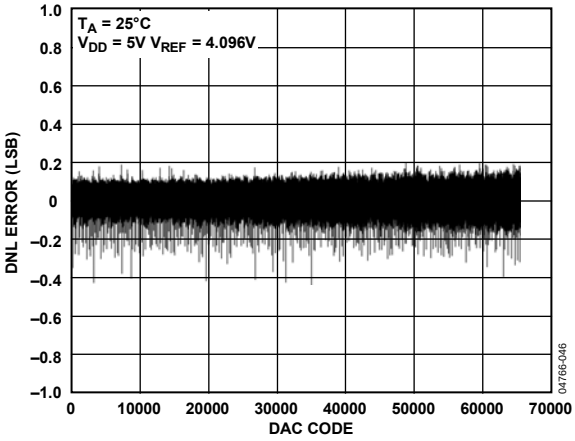


Figure 7. DNL Error vs. DAC Code

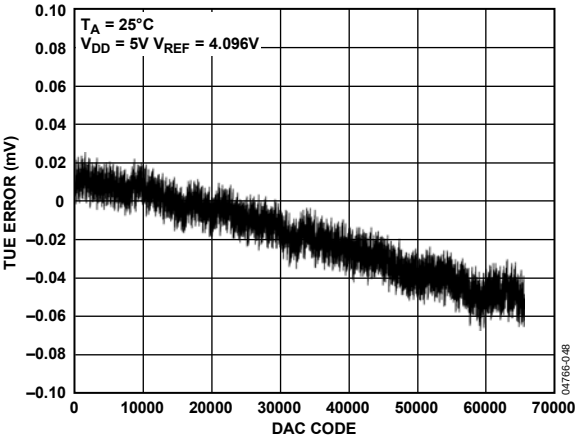


Figure 5. TUE Error vs. DAC Code

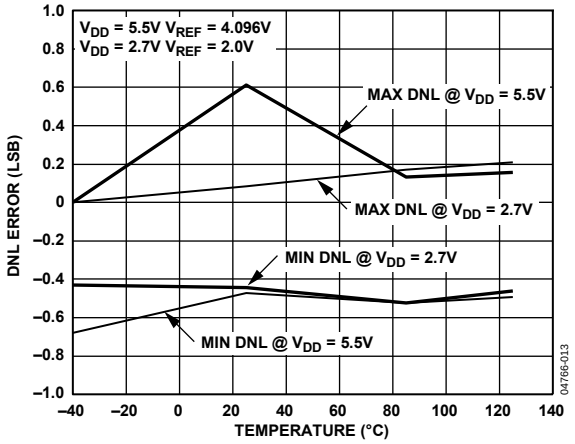


Figure 8. DNL Error vs. Temperature

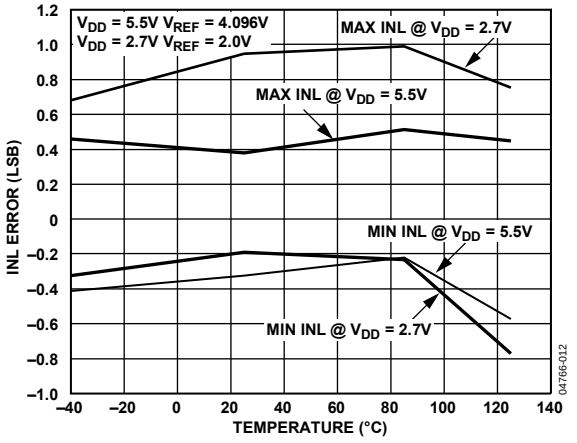


Figure 6. INL Error vs. Temperature

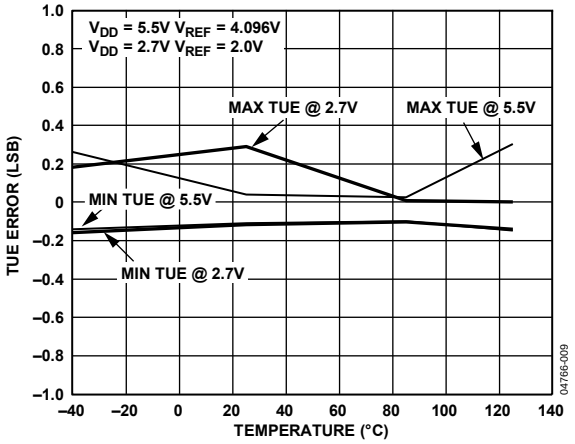


Figure 9. TUE Error vs. Temperature

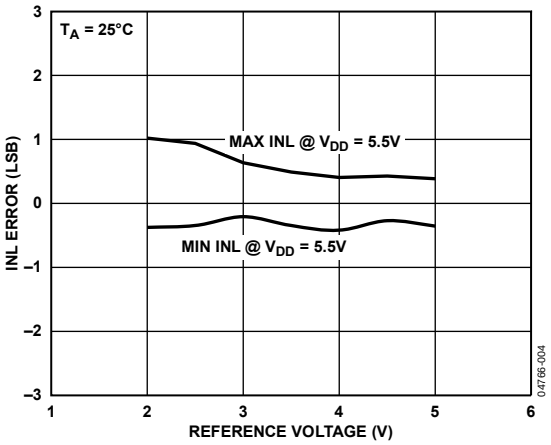


Figure 10. INL Error vs. Reference Input Voltage

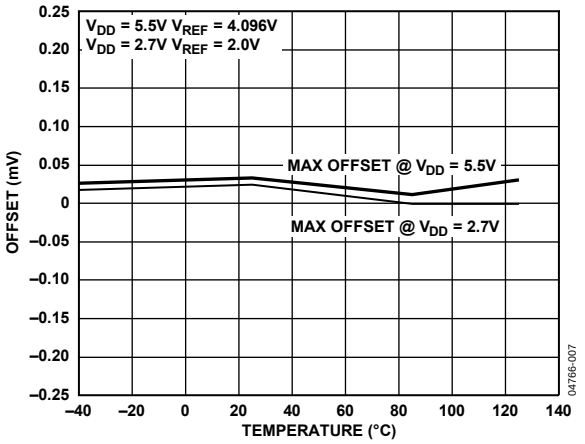


Figure 13. Offset vs. Temperature

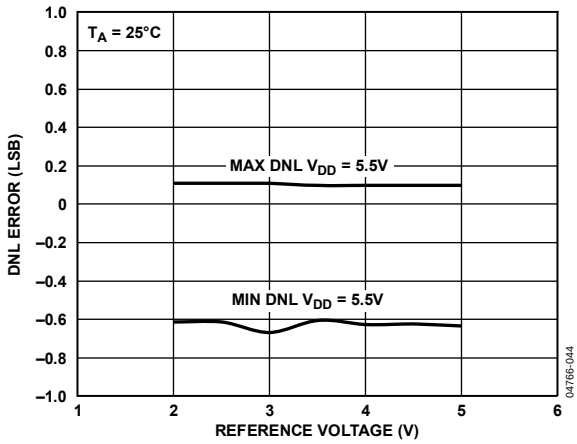


Figure 11. DNL Error vs. Reference Input Voltage

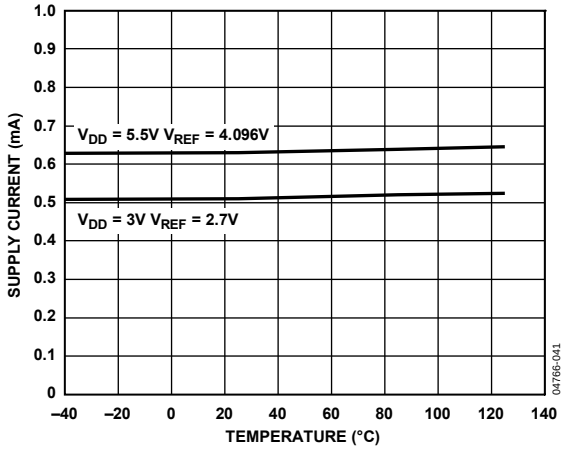


Figure 14. Supply Current vs. Temperature

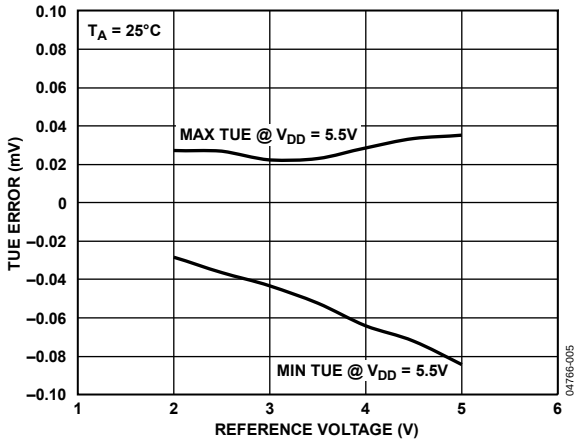


Figure 12. TUE Error vs. Reference Input Voltage

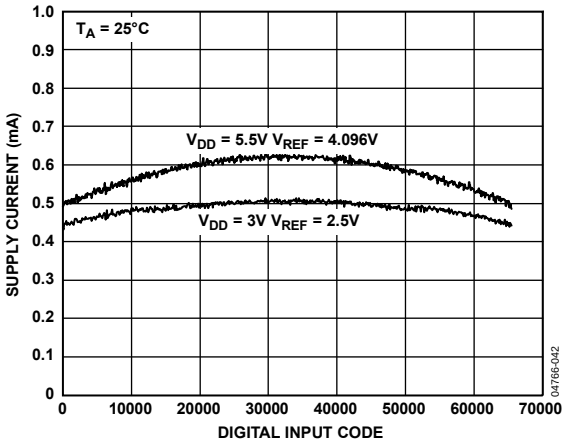


Figure 15. Supply Current vs. Digital Input Code

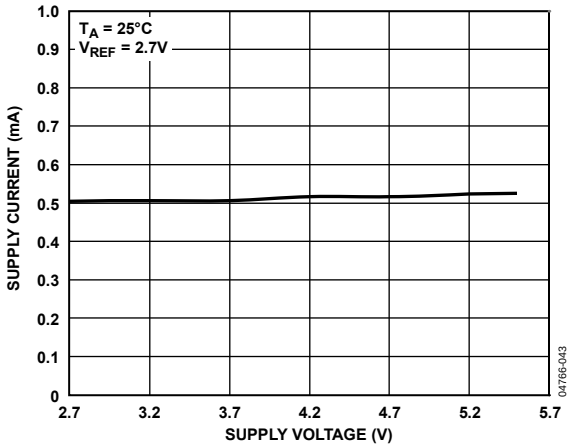


Figure 16. Supply Current vs. Supply Voltage

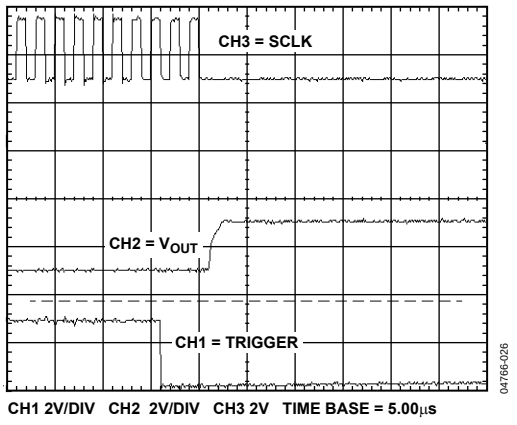


Figure 19. Exiting Power-Down Time to Midscale

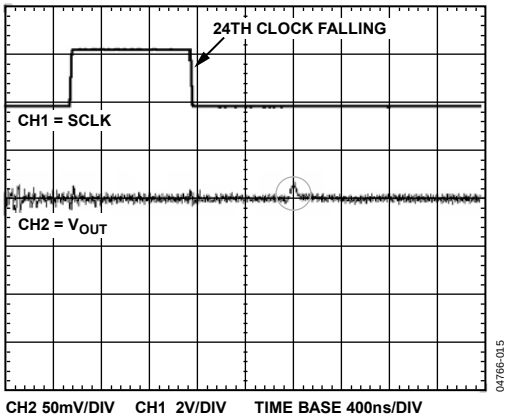


Figure 17. Digital-to-Analog Glitch Impulse (See Figure 21)

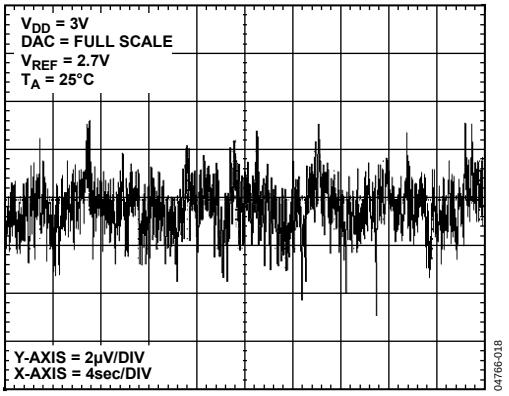


Figure 20. 0.1 Hz to 10 Hz Noise Plot

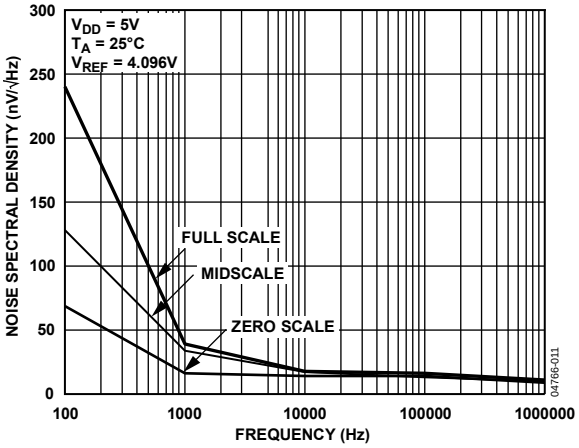


Figure 18. Output Noise Spectral Density

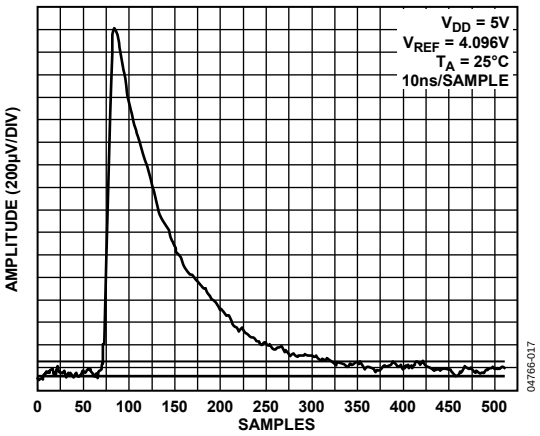


Figure 21. Glitch Energy

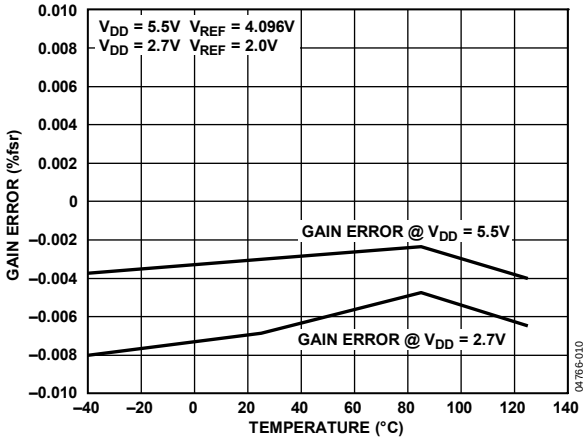


Figure 22. Gain Error vs. Temperature

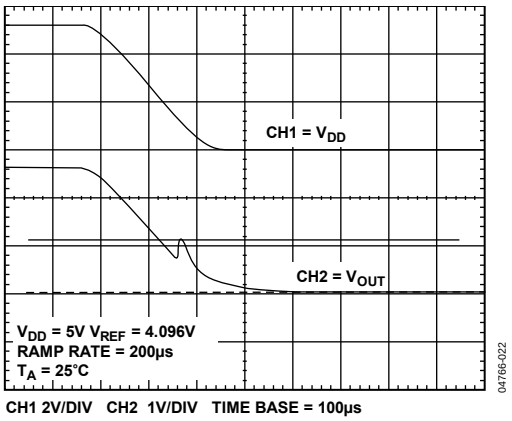


Figure 25. Hardware Power-Down Glitch

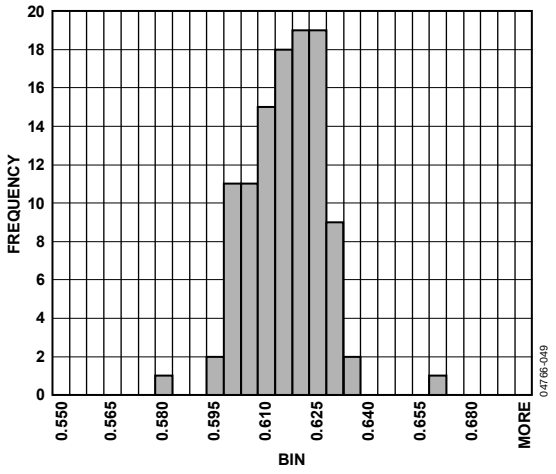


Figure 23. I_{DD} Histogram @ V_{DD} = 5 V

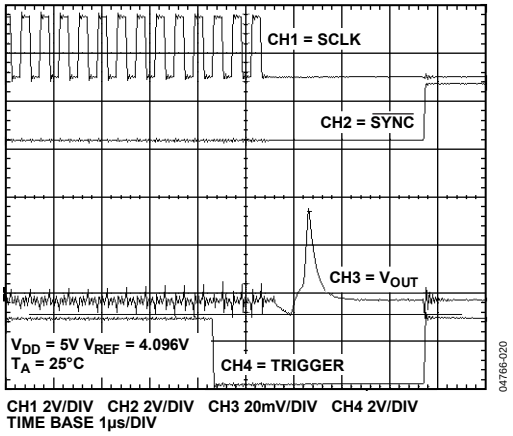


Figure 26. Exiting Software Power-Down Glitch

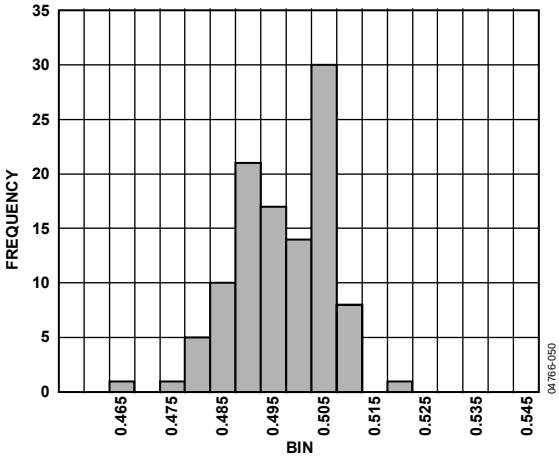


Figure 24. I_{DD} Histogram @ V_{DD} = 3 V

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. A typical INL error vs. code plot is shown in Figure 4.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL error vs. code plot is shown in Figure 7.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5063 because the output of the DAC cannot go below 0 V. This is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percentage of the full-scale range.

Total Unadjusted Error (TUE)
Total unadjusted error is a measure of the output error, taking all the various errors into account. A typical TUE vs. code plot is shown in Figure 5.

Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift
Gain error drift is a measure of the change in gain error with a change in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition. See Figure 17 and Figure 21. Figure 17 shows the glitch generated following completion of the calibration routine; Figure 21 zooms in on this glitch.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

THEORY OF OPERATION

The AD5063 is a single 16-bit, serial input, voltage-output DAC. It operates from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5063 in a 24-bit word format via a 3-wire serial interface.

The AD5063 incorporates a power-on reset circuit that ensures the DAC output powers up to midscale. The device also has a software power-down mode pin that reduces the typical current consumption to less than 1 μA.

DAC ARCHITECTURE

The DAC architecture of the AD5063 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 27. The four MSBs of the 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either the DACGND or V_{REF} buffer output. The remaining 12 bits of the data-word drive Switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

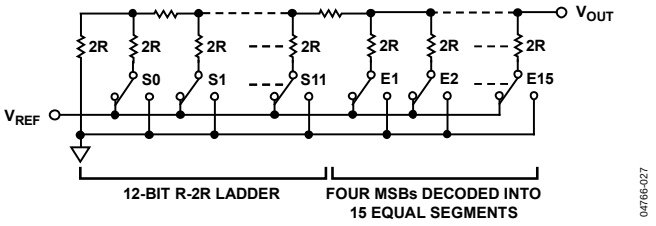


Figure 27. DAC Ladder Structure

REFERENCE BUFFER

The AD5063 operates with an external reference. The reference input (V_{REF}) has an input range of 2 V to AV_{DD} − 50 mV. This input voltage is used to provide a buffered reference for the DAC core.

SERIAL INTERFACE

The AD5063 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as most DSPs. (See Figure 2 for a timing diagram of a typical write sequence.)

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making these parts compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed (that is, a change in the DAC register contents and/or a change in the mode of operation).

At this stage, the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 12 ns before the next write sequence, so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Because the $\overline{SYNC}$ buffer draws more current when V_{IH} = 1.8 V than it does when V_{IH} = 0.8 V, $\overline{SYNC}$ should be idled low between write sequences for even lower power operation of the part. As previously indicated, however, it must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide (see Figure 28). PD1 and PD0 are bits that control the operating mode of the part (normal mode or any one of the three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next 16 bits are the data bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

$\overline{SYNC}$ INTERRUPT

In a normal write sequence, the $\overline{SYNC}$ line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However, if $\overline{SYNC}$ is brought high before the 24th falling edge, it acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 31).

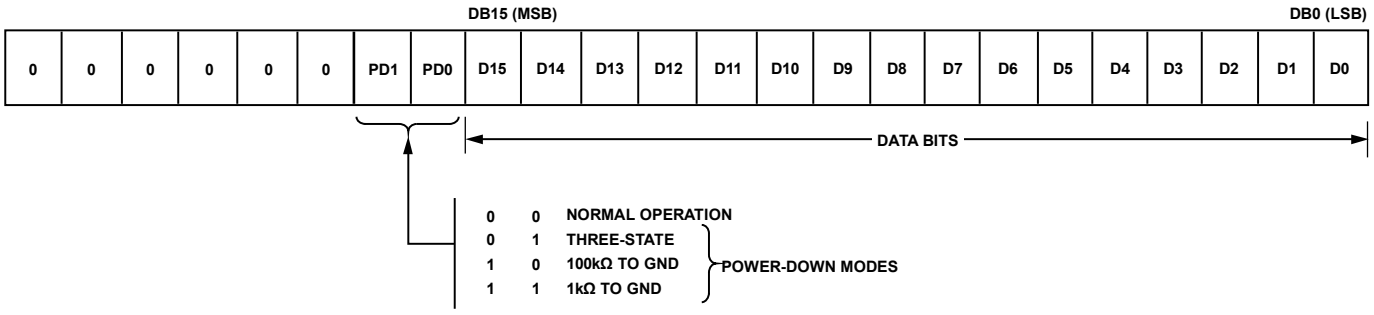


Figure 28. Input Register Contents

POWER-ON TO MIDSCALE

The AD5063 contains a power-on reset circuit that controls the output voltage during power-up. The DAC register is filled with the midscale code, and the output voltage is midscale until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the DAC output while it is in the process of powering up.

SOFTWARE RESET

The device can be put into software reset by setting all bits in the DAC register to 1; this includes writing 1s to Bits D23 to D16, which is not the normal mode of operation. Note that the $\overline{\text{SYNC}}$ interrupt command cannot be performed if a software reset command is started.

POWER-DOWN MODES

The AD5063 contains four separate modes of operation. These modes are software-programmable by setting two bits (DB17 and DB16) in the control register. Table 6 shows how the state of the bits corresponds to the operating mode of the device.

Table 6. Modes of Operation for the AD5063

DB17	DB16	Operating Mode
0	0	Normal operation
		Power-down mode:
0	1	Three-state
1	0	100 kΩ to GND
1	1	1 kΩ to GND

When both bits are set to 0, the part has normal power consumption. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three options: The output can be connected internally to GND through either a 1 kΩ resistor or a 100 kΩ resistor, or it can be left open-circuited (three-stated). The output stage is illustrated in Figure 29.

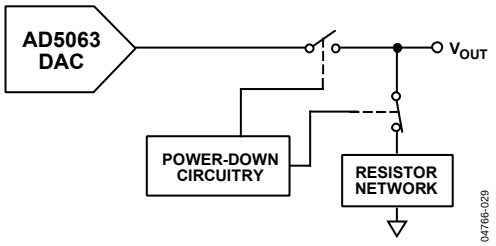


Figure 29. Output Stage During Power-Down

The bias generator, DAC core, and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V, and 5 μs for V_{DD} = 3 V (see Figure 19).

MICROPROCESSOR INTERFACING

AD5063 to ADSP-2101/ADSP-2103 Interface

Figure 30 shows a serial interface between the AD5063 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT are programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

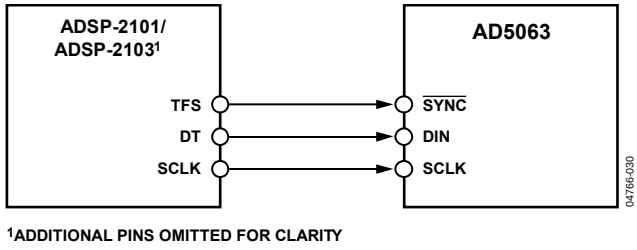


Figure 30. AD5063 to ADSP-2101/ADSP-2103 Interface

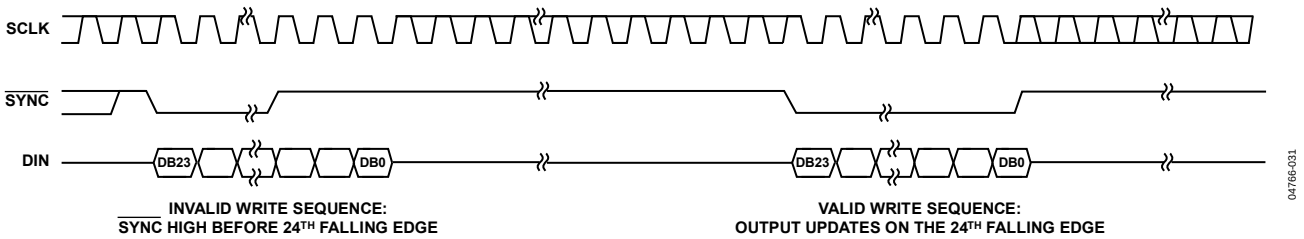
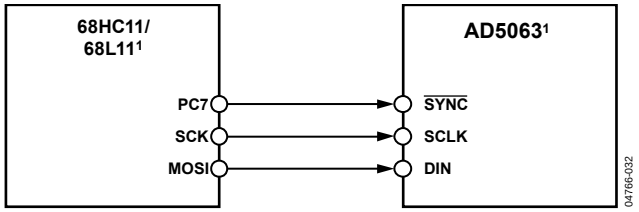


Figure 31. $\overline{\text{SYNC}}$ Interrupt Facility

AD5063 to 68HC11/68L11 Interface

Figure 32 shows a serial interface between the AD5063 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK pin of the AD5063, and the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface require that the 68HC11/68L11 be configured so that its CPOL bit is 0 and its CPHA bit is 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 are configured with their CPOL bit set to 0 and their CPHA bit set to 1, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5063, PC7 is left low after the first eight bits are transferred, and then a second serial write operation is performed to the DAC, with PC7 taken high at the end of this procedure.

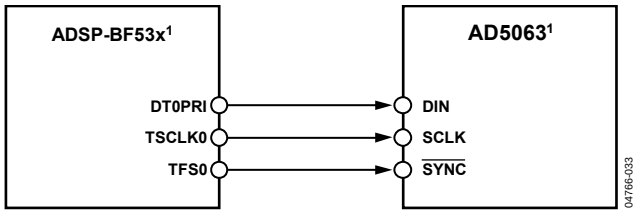


[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 32. AD5063 to 68HC11/68L11 Interface

AD5063 to Blackfin® ADSP-BF53x Interface

Figure 33 shows a serial interface between the AD5063 and the Blackfin® ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5063, the setup for the interface is as follows: DT0PRI drives the DIN pin of the AD5063, TSCLK0 drives the SCLK of the part, and TFS0 drives $\overline{\text{SYNC}}$.

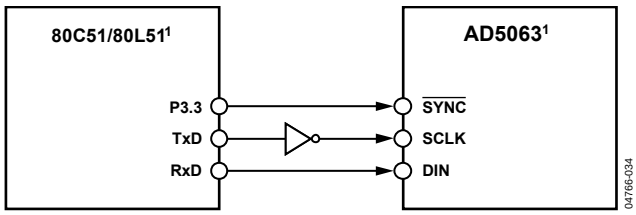


[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 33. AD5063 to Blackfin ADSP-BF53x Interface

AD5063 to 80C51/80L51 Interface

Figure 34 shows a serial interface between the AD5063 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5063, and RxD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5063, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; therefore, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 output the serial data in a format that has the LSB first. The AD5063 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

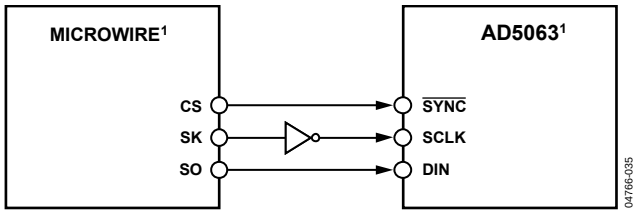


[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 34. AD5063 to 80C51/80L51 Interface

AD5063 to MICROWIRE Interface

Figure 35 shows an interface between the AD5063 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and clocked into the AD5063 on the rising edge of the SK.



[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 35. AD5063 to MICROWIRE Interface

APPLICATIONS

CHOOSING A REFERENCE FOR THE AD5063

To achieve optimum performance of the AD5063, thought should be given to the choice of a precision voltage reference. The AD5063 has one reference input, V_{REF}. The voltage on the reference input is used to supply the positive input to the DAC; therefore, any error in the reference is reflected in the DAC.

There are four possible sources of error when choosing a voltage reference for high accuracy applications: initial accuracy, ppm drift, long-term drift, and output voltage noise. Initial accuracy on the output voltage of the DAC leads to a full-scale error in the DAC. To minimize these errors, a reference with high initial accuracy is preferred. Also, choosing a reference with an output trim adjustment, such as the ADR423, allows a system designer to trim out system errors by setting a reference voltage to a voltage other than the nominal. The trim adjustment can also be used at any point within the operating temperature range to trim out error.

Because the supply current required by the AD5063 is extremely low, the parts are ideal for low supply applications. The ADR395 voltage reference is recommended; it requires less than 100 µA of quiescent current and can, therefore, drive multiple DACs in one system, if required. It also provides very good noise performance at 8 µV p-p in the 0.1 Hz to 10 Hz range.

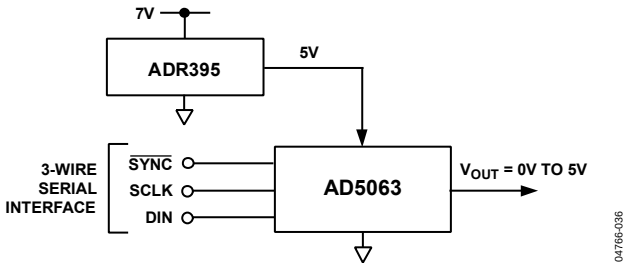


Figure 36. ADR395 as a Reference to AD5063

Long-term drift is a measure of how much the reference drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable during its entire lifetime. The temperature coefficient of a reference's output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce the temperature dependence of the DAC output voltage on ambient conditions.

In high accuracy applications, which have a relatively low tolerance for noise, reference output voltage noise needs to be considered. It is important to choose a reference with as low an output noise voltage as practical for the system noise resolution required. Precision voltage references, such as the ADR435, produce low output noise in the 0.1 Hz to 10 Hz region. Examples of some recommended precision references for use as the supply to the AD5063 are shown in Table 7.

Table 7. Recommended Precision References for the AD5063

Part No.	Initial Accuracy (mV max)	Temperature Drift (ppm/°C max)	0.1 Hz to 10 Hz Noise (µV p-p typ)
ADR435	±2	3 (R-8)	8
ADR425	±2	3 (R-8)	3.4
ADR02	±3	3 (R-8)	10
ADR02	±3	3 (SC-70)	10
ADR395	±5	9 (TSOT-23)	8

BIPOLAR OPERATION USING THE AD5063

The AD5063 has been designed for single-supply operation, but a bipolar output range is also possible by using the circuit shown in Figure 37. This circuit yields an output voltage range of ±4.096 V. Rail-to-rail operation at the amplifier output is achievable using AD8675/AD8031/AD8032 or an OP196.

The output voltage for any input code can be calculated as

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1+R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65,536).

With V_{REF} = 5 V, R1 = R2 = 30 kΩ

$$V_O = \left(\frac{10 \times D}{65536} \right) - 5\ \text{V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output and 0xFFFF corresponding to a +5 V output.

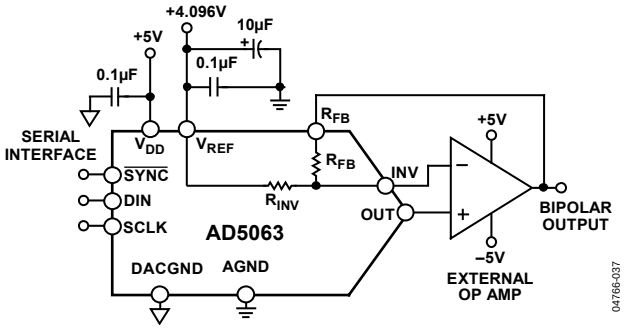


Figure 37. Bipolar Operation

USING THE AD5063 WITH A GALVANICALLY ISOLATED INTERFACE CHIP

In process-control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from hazardous common-mode voltages that may occur in the area where the DAC is functioning. *i*Coupler® provides isolation in excess of 2.5 kV. Because the AD5063 uses a 3-wire serial logic interface, the ADuM130x family provides an ideal digital solution for the DAC interface.

The ADuM130x isolators provide three independent isolation channels in a variety of channel configurations and data rates. They operate across the full range of 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier.

Figure 38 shows a typical galvanically isolated configuration using the AD5063. The power supply to the part also needs to be isolated; this is accomplished by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5063.

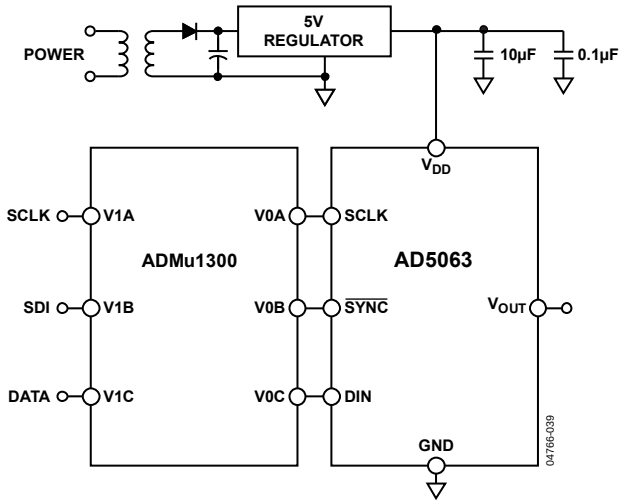


Figure 38. AD5063 with a Galvanically Isolated Interface

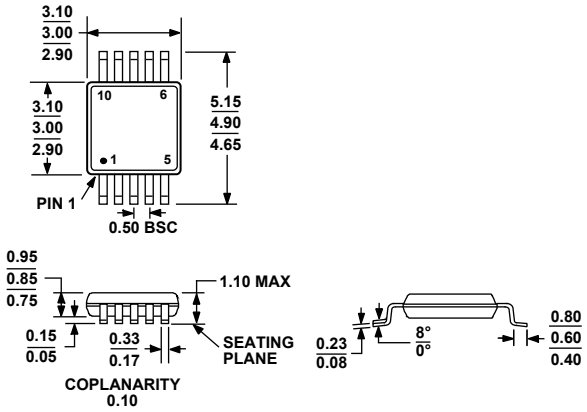
POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to consider carefully the power supply and ground return layout on the board. The printed circuit board containing the AD5063 should have separate analog and digital sections, each on its own area of the board. If the AD5063 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5063.

The power supply to the AD5063 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should physically be as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and low effective series inductance (ESI), as do common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents from internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by a digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 39. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	INL	Settling Time	Package Description	Package Option	Branding
AD5063BRMZ[1]	−40°C to +85°C	1 LSB	4 µs typ	10-Lead MSOP	RM-10	D49
AD5063BRMZ-REEL7[1]	−40°C to +85°C	1 LSB	4 µs typ	10-Lead MSOP	RM-10	D49
AD5063BRMZ-1[1]	−40°C to +85°C	1 LSB	1 µs max	10-Lead MSOP	RM-10	DCG
AD5063BRMZ-1-REEL7[1]	−40°C to +85°C	1 LSB	1 µs max	10-Lead MSOP	RM-10	DCG
EVAL-AD5063EB				Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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D04766-0-8/09(C)

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