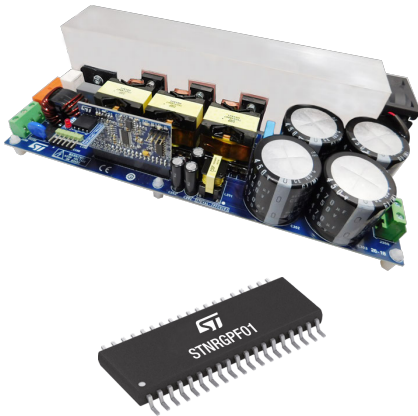


3 kW three-channel interleaved PFC reference design based on the STNRGPF01 digital controller



Features

- Input voltage range: 90 to 265 V_{AC}
- Line frequency range: 47 to 63 Hz
- Maximum output power: 3 kW at 230 V
- Output voltage: 400 V
- Power factor: > 0.98 at 20% load
- Total Harmonic Distortion: <5% at 20% load
- Mixed-signal average current mode control, CCM fixed frequency operation
- Switching Frequency: 111 kHz
- Cycle-by-cycle regulation (analog current control loop)
- Input voltage and load feed-forwards
- Phase shedding
- Burst-mode operation
- Overvoltage protection
- Thermal protection
- Status indicator LEDs
- Inrush current limiter function
- Cooling function

Description

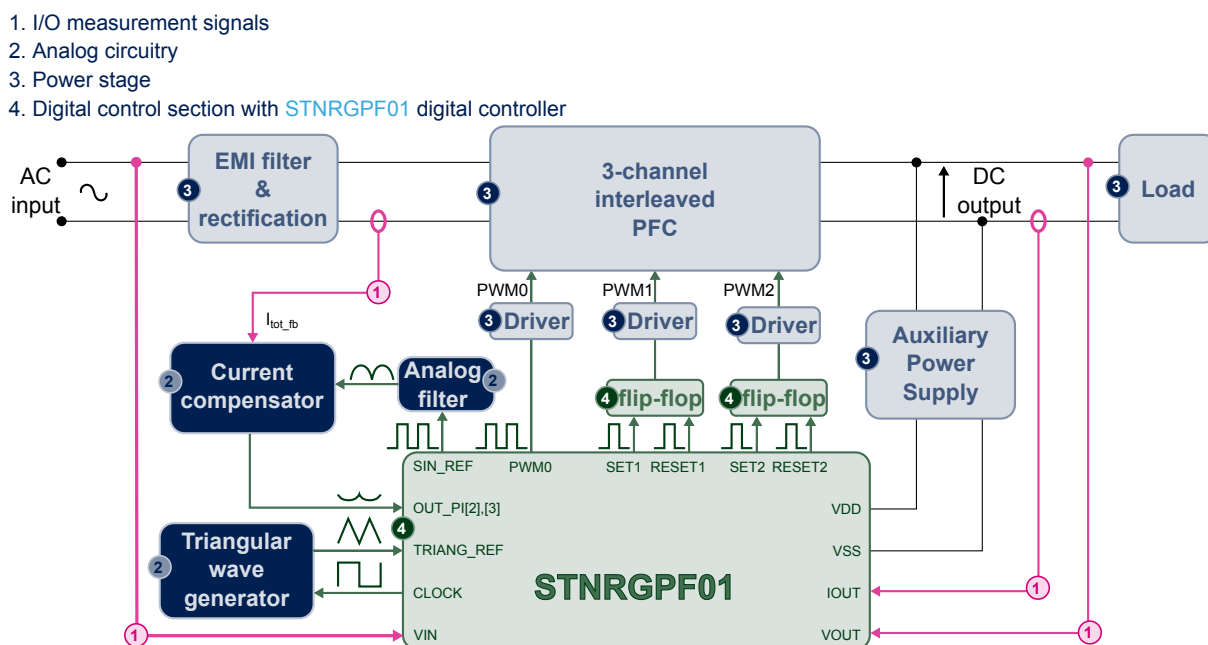
The STEVAL-IPFC01V1 3 kW interleaved PFC reference design is based on the STNRGPF01 digital controller and includes a separate power board, control board and programming board. The STNRGPF01 is a digital configurable ASIC developed by STMicroelectronics, which can drive up to three channels in an interleaved PFC for industrial applications.

The [STNRGPF01](#) digital controller on the control board implements mixed signal (analog/digital) average current mode control in CCM at fixed frequency. The analog section ensures cycle-by-cycle current regulation, while digital control manages the non-time critical operations. You can use the [eDesignSuite](#) software available on the ST website to configure the [STNRGPF01](#) to satisfy the specifications of each interleaved PFC.

Product summary	
3 kW three-channel interleaved PFC based on the STNRGPF01 digital controller	STEVAL-IPFC01V1
three-channel interleaved CCM PFC digital controller	STNRGPF01

1 STEVAL-IPFC01V1 overview

Figure 1. STEVAL-IPFC01V1 block diagram



The STEVAL-IPFC01V1 implements mixed signal (analog/digital) control, so the converter can manage a range of input and output conditions and still remain highly responsive to fast transients in input signals. The inner current loop is a hardware analog proportional-integral (PI) compensator that ensures the highest possible bandwidth and cycle-by-cycle sensing and regulation. The outer voltage loop is performed by a digital PI controller with fast dynamic response.

Figure 2. STEVAL-IPFC01P1 schematic - input section

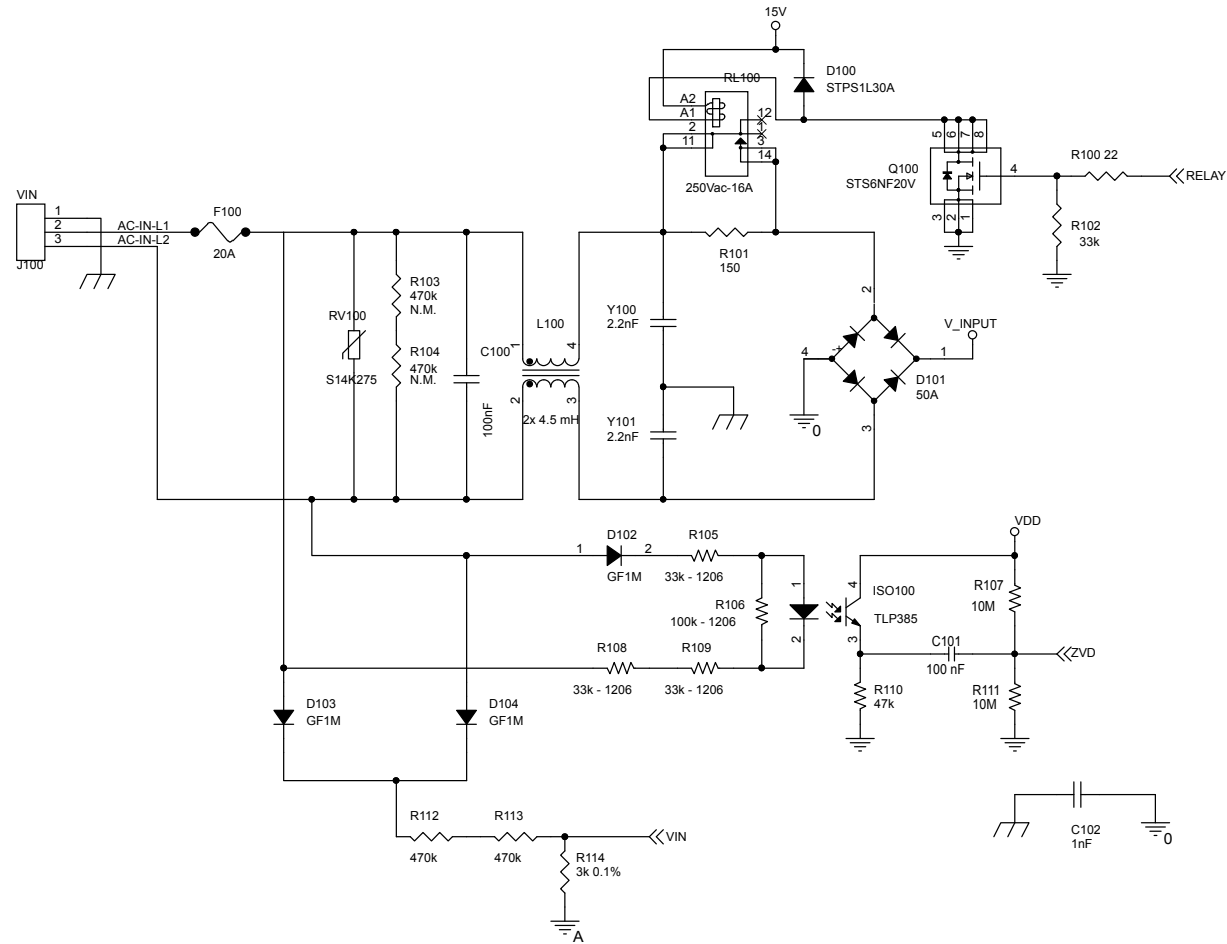


Figure 3. STEVAL-IPFC01P1 schematic - auxiliary power supply

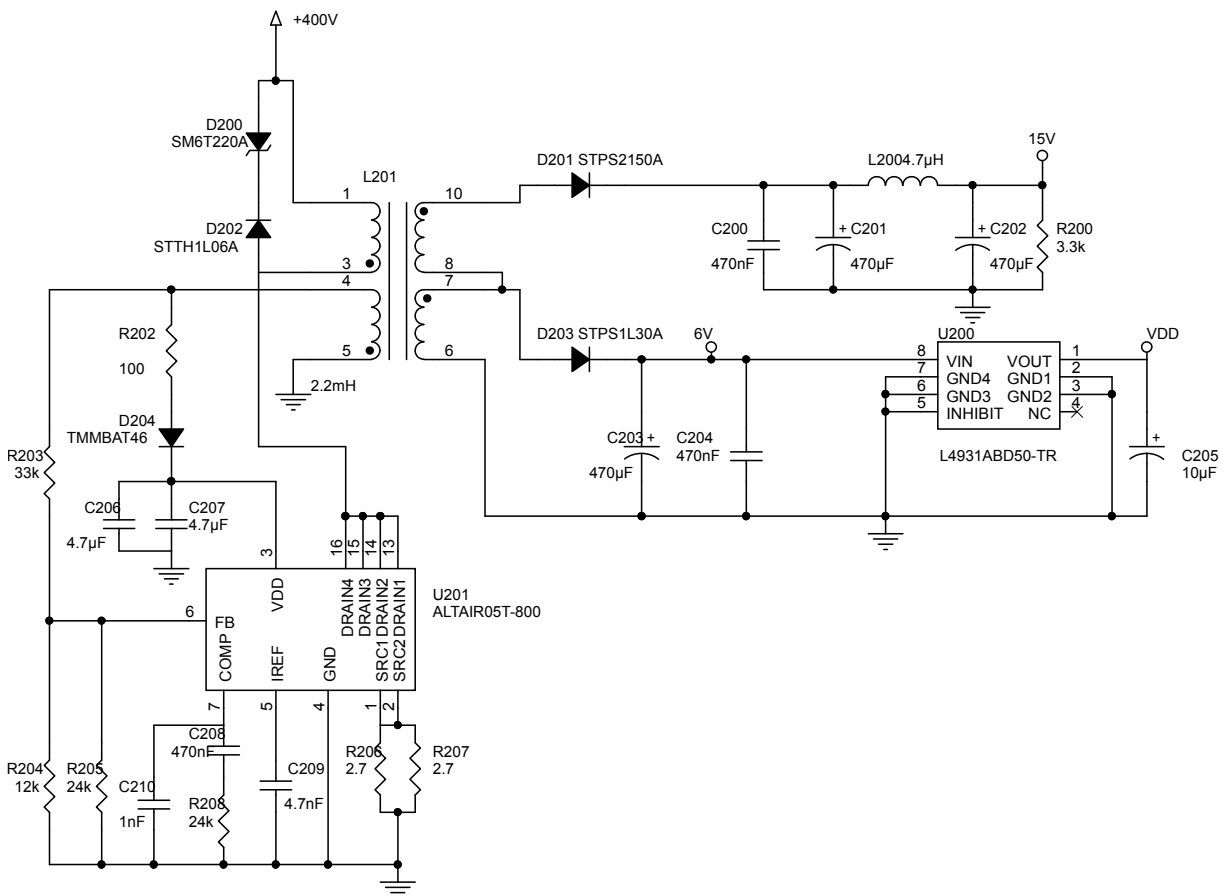
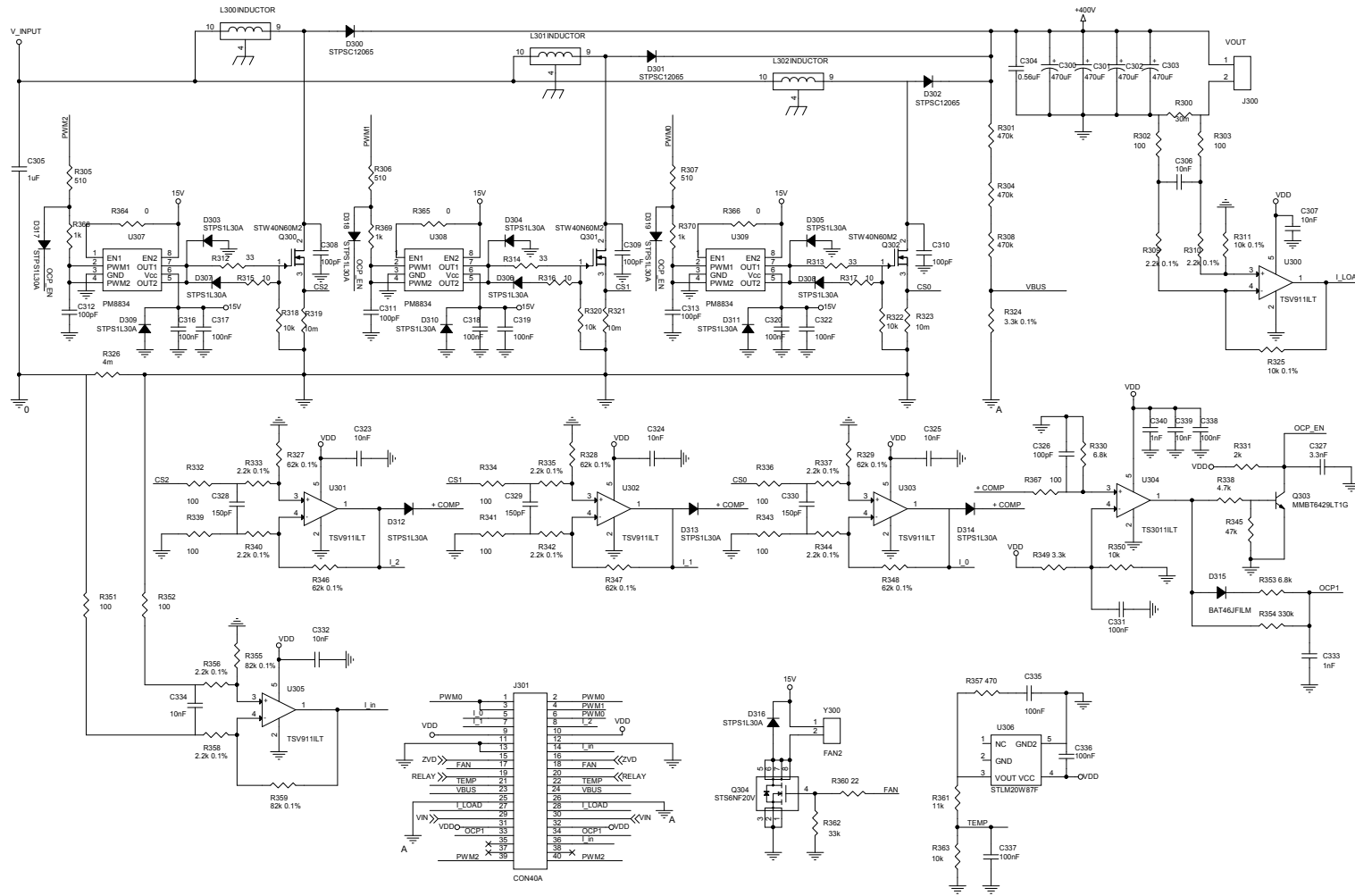
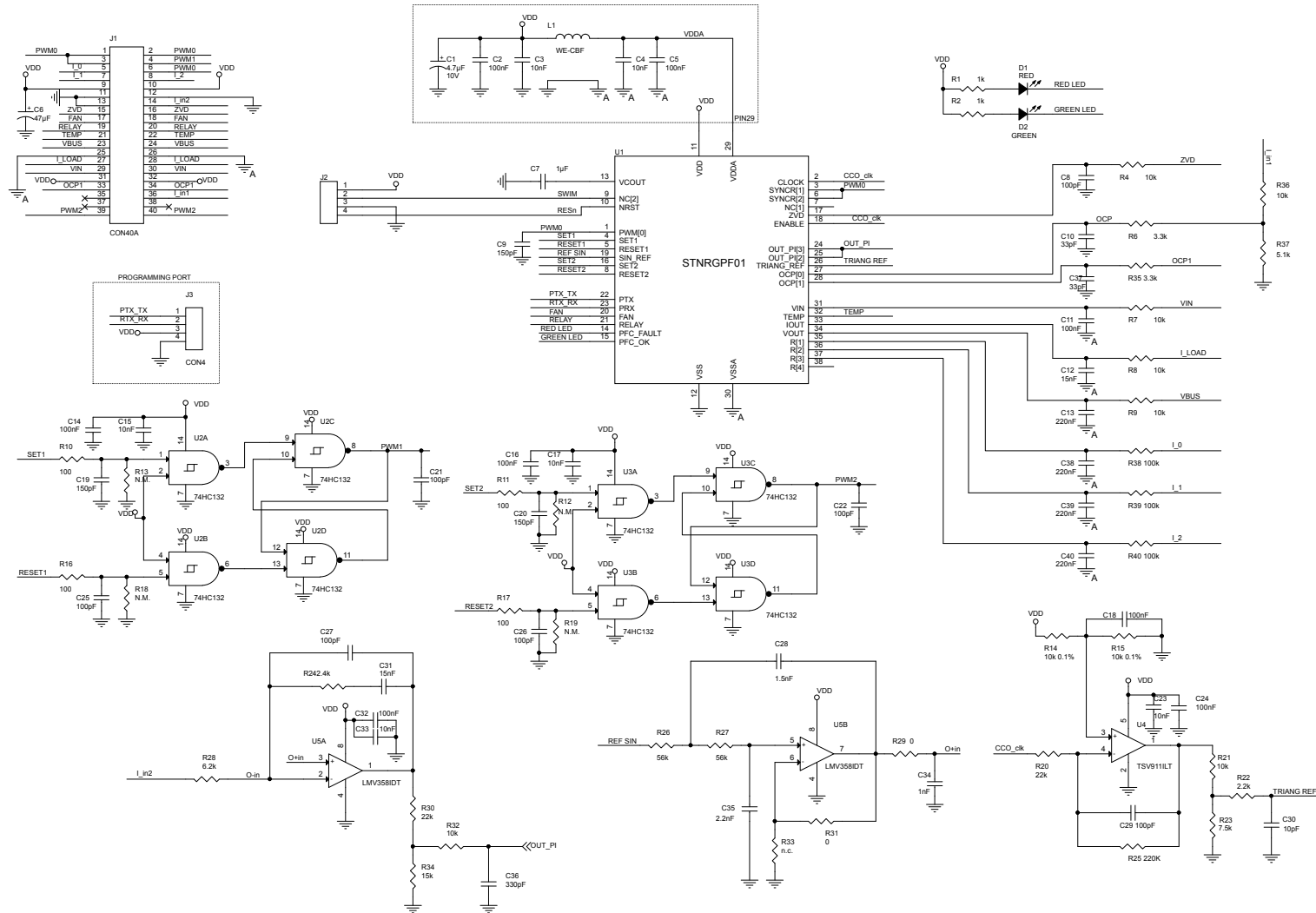


Figure 4. STEVAL-IPFC01P1 schematic - boost interleaving section



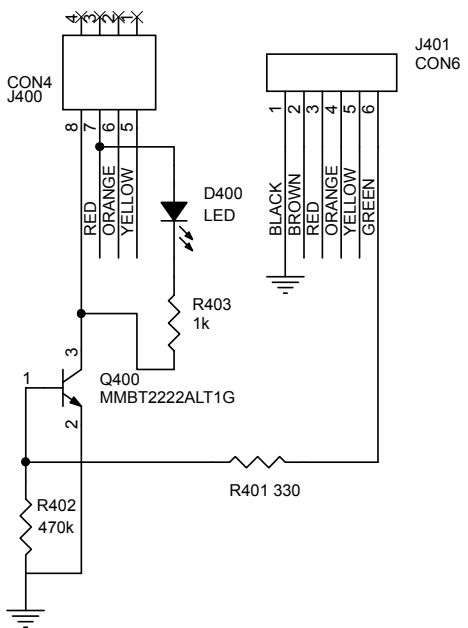
STEVAL-IPFC01C1 control board schematic

Figure 5. STEVAL-IPFC01C1 schematic



4 STEVAL-IPFC01A1 adapter board schematic

Figure 6. STEVAL-IPFC01A1 schematic



Revision history

Table 1. Document revision history

Date	Version	Changes
11-Sep-2018	1	Initial release.
02-Jan-2019	2	Updated <i>Figure 1. STEVAL-IPFC01V1 block diagram</i> and <i>Figure 4. STEVAL-IPFC01P1 schematic - boost interleaving section</i> .
09-Sep-2019	3	Throughout document: minor text edits Updated Figure 3. STEVAL-IPFC01P1 schematic - auxiliary power supply

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