# Si4710/11-B30 FM RADIO TRANSMITTER

## Features

- Integrated receive power measurement
- Worldwide FM band support (76–108 MHz)
- Requires only two external components
- Frequency synthesizer with integrated VCO
- Digital stereo modulator
- Programmable pre-emphasis
- Analog/digital audio interface
- Audio silence detector
- Programmable reference clock
- RDS/RBDS encoder (Si4711 only)
- PCB loop and stub antenna support with self-calibrated capacitor tuning
- Programmable transmit level
- Audio dynamic range control
- Advanced modulation control
- 2.7 to 5.5 V supply voltage
- Integrated LDO regulator
- 3 x 3 x 0.55 mm 20-pin QFN
  - Pb-free and RoHS Compliant
- Designed for compatibility with cellular operation

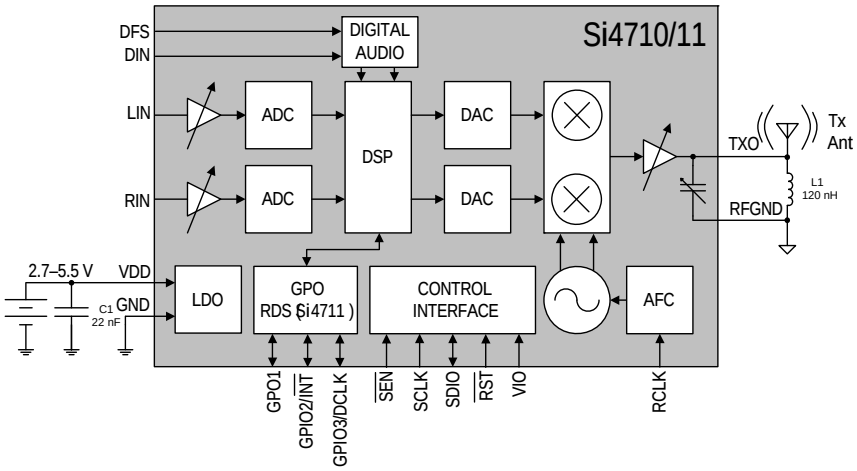
## Applications

- Cellular handsets/hands-free
- MP3 players
- Portable media players
- Wireless speakers/microphone
- Satellite digital audio radios
- Personal computers/notebooks

## Description

The Si4710/11 integrates the complete transmit functions for standards-compliant unlicensed FM broadcast stereo transmission. Users must comply with local regulations on radio frequency (RF) transmission.

## Functional Block Diagram



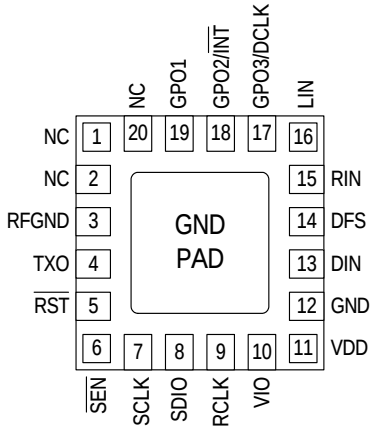
**Ordering Information:**

See page 32.

**Pin Assignments**

**Si4710/11**

(Top View)




Patents pending

**Note:** To ensure proper operation and performance, follow the guidelines in "AN383: Universal Antenna Selection and Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.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# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.7 | — | 5.5 | V |
| Interface Supply Voltage | $V_{IO}$ | | 1.5 | — | 3.6 | V |
| Power Supply Powerup Rise Time | $V_{DDRISE}$ | | 10 | — | — | µs |
| Interface Supply Powerup Rise Time | $V_{IORISE}$ | | 10 | — | — | µs |
| Ambient Temperature | $T_A$ | | –20 | 25 | 85 | °C |

**Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_{DD}$ = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

### Table 2. Absolute Maximum Ratings[1,2]

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | –0.5 to 5.8 | V |
| Interface Supply Voltage | $V_{IO}$ | –0.5 to 3.9 | V |
| Input Current[3] | $I_{IN}$ | 10 | mA |
| Input Voltage[3] | $V_{IN}$ | –0.3 to ($V_{IO}$ + 0.3) | V |
| Operating Temperature | $T_{OP}$ | –40 to 95 | °C |
| Storage Temperature | $T_{STG}$ | –55 to 150 | °C |
| RF Input Level[4] | | 0.4 | $V_{PK}$ |

**Notes:**
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4710/11 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, DIN, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.
4. At RF input pin, TXO.

## Table 3. DC Characteristics

Test conditions: $V_{RF}$ = 118 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, unless otherwise specified.
Production test conditions: $V_{DD}$ = 3.3 V, $V_{IO}$ = 3.3 V, $T_A$ = 25 °C, $F_{RF}$ = 98 MHz.
Characterization test conditions: $V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C, $F_{RF}$ = 76–108 MHz.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FM Transmitter from Line Input** | | | | | | |
| TX Supply Current | $I_{TX}$ | | — | 18.8 | 22.8 | mA |
| TX Interface Supply Current | $I_{IO}$ | | — | 320 | 600 | µA |
| **FM Transmitter from Digital Audio Input** | | | | | | |
| TX Supply Current | $I_{DTX}$ | DCLK = 3.072 MHz | — | 18.3 | — | mA |
| TX Interface Supply Current | $I_{DIO}$ | DCLK = 3.072 MHz | — | 320 | — | µA |
| **Supplies and Interface** | | | | | | |
| $V_{DD}$ Powerdown Current | $I_{DD}$ | Powerdown mode | — | 10 | 20 | µA |
| $V_{IO}$ Interface Powerdown Current | $I_{IO}$ | SCLK, RCLK inactive Powerdown mode | — | 3 | 10 | µA |
| High Level Input Voltage[1] | $V_{IH}$ | | 0.7 x $V_{IO}$ | — | $V_{IO}$ + 0.3 | V |
| Low Level Input Voltage[1] | $V_{IL}$ | | –0.3 | — | 0.3 x $V_{IO}$ | V |
| High Level Input Current[1] | $I_{IH}$ | $V_{IN}$ = $V_{IO}$ = 3.6 V | –10 | — | 10 | µA |
| Low Level Input Current[1] | $I_{IL}$ | $V_{IN}$ = 0 V, $V_{IO}$ = 3.6 V | –10 | — | 10 | µA |
| High Level Output Voltage[2] | $V_{OH}$ | $I_{OUT}$ = 500 µA | 0.8 x $V_{IO}$ | — | — | V |
| Low Level Output Voltage[2] | $V_{OL}$ | $I_{OUT}$ = –500 µA | — | — | 0.2 x $V_{IO}$ | V |

**Notes:**
1. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, DIN, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.
2. For output pins SDIO, GPO1, GPO2/$\overline{\text{INT}}$, and GPO3.

**Table 4. Reset Timing Characteristics[1,2,3]**
($V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}$↑[4] | $t_{SRST}$ | 100 | — | — | µs |
| GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}$↑ | $t_{HRST}$ | 30 | — | — | ns |

**Important Notes:**
1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the 1st start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum $t_{SRST}$ is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum $t_{SRST}$ is 100 µs, to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

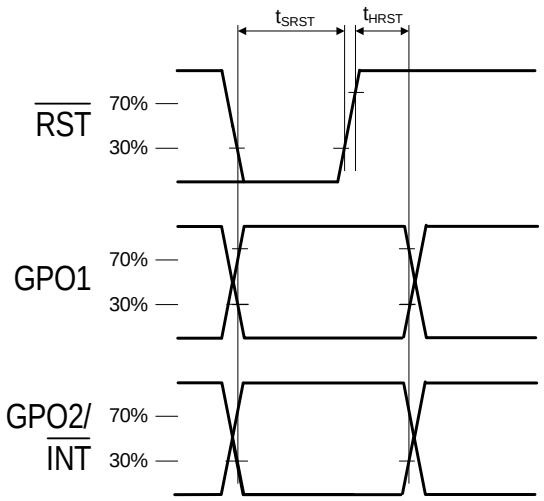



**Figure 1. Reset Timing Parameters for Busmode Select**

**Table 5. 2-Wire Control Interface Characteristics[1,2,3]**
($V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK Frequency | $f_{SCL}$ | | 0 | — | 400 | kHz |
| SCLK Low Time | $t_{LOW}$ | | 1.3 | — | — | µs |
| SCLK High Time | $t_{HIGH}$ | | 0.6 | — | — | µs |
| SCLK Input to SDIO↓ Setup (START) | $t_{SU:STA}$ | | 0.6 | — | — | µs |
| SCLK Input to SDIO↓ Hold (START) | $t_{HD:STA}$ | | 0.6 | — | — | µs |
| SDIO Input to SCLK↑ Setup | $t_{SU:DAT}$ | | 100 | — | — | ns |
| SDIO Input to SCLK↓ Hold[4,5] | $t_{HD:DAT}$ | | 0 | — | 900 | ns |
| SCLK input to SDIO↑ Setup (STOP) | $t_{SU:STO}$ | | 0.6 | — | — | µs |
| STOP to START Time | $t_{BUF}$ | | 1.3 | — | — | µs |
| SDIO Output Fall Time | $t_{f:OUT}$ | | $20 + 0.1\frac{C_b}{1\ pF}$ | — | 250 | ns |
| SDIO Input, SCLK Rise/Fall Time | $t_{f:IN}$ $t_{r:IN}$ | | $20 + 0.1\frac{C_b}{1\ pF}$ | — | 300 | ns |
| SCLK, SDIO Capacitive Loading | $C_b$ | | — | — | 50 | pF |
| Input Filter Pulse Suppression | $t_{SP}$ | | — | — | 50 | ns |

**Notes:**
1. When $V_{IO}$ = 0 V, SCLK and SDIO are low-impedance. 2-wire control interface is $I^2C$ compatible.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4710/11 delays SDIO by a minimum of 300 ns from the $V_{IH}$ threshold of SCLK to comply with the minimum t
5. $_{HD:DAT}$ specification.
6. The maximum $t_{HD:DAT}$ has only to be met when $f_{SCL}$ = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

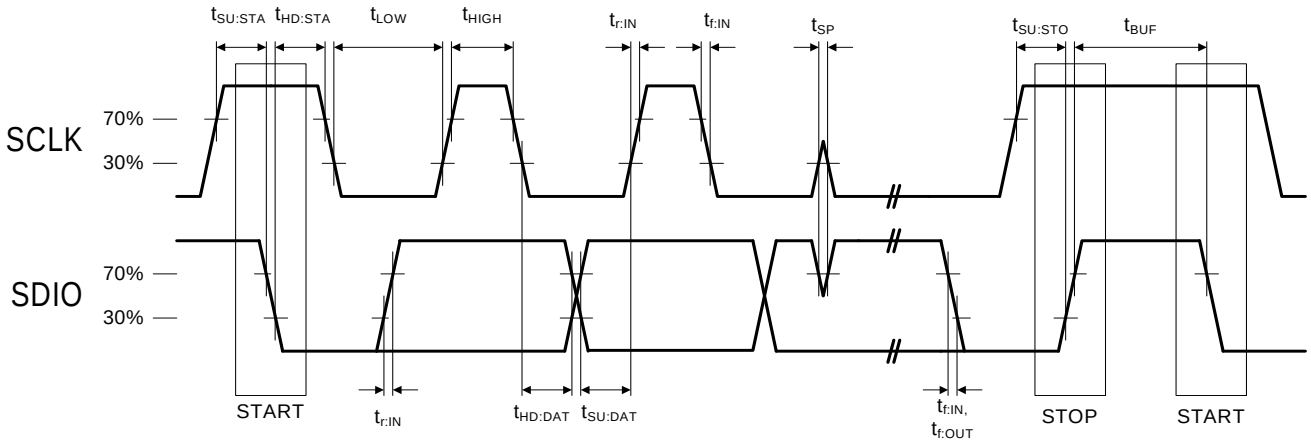



**Figure 2. 2-Wire Control Interface Read and Write Timing Parameters**

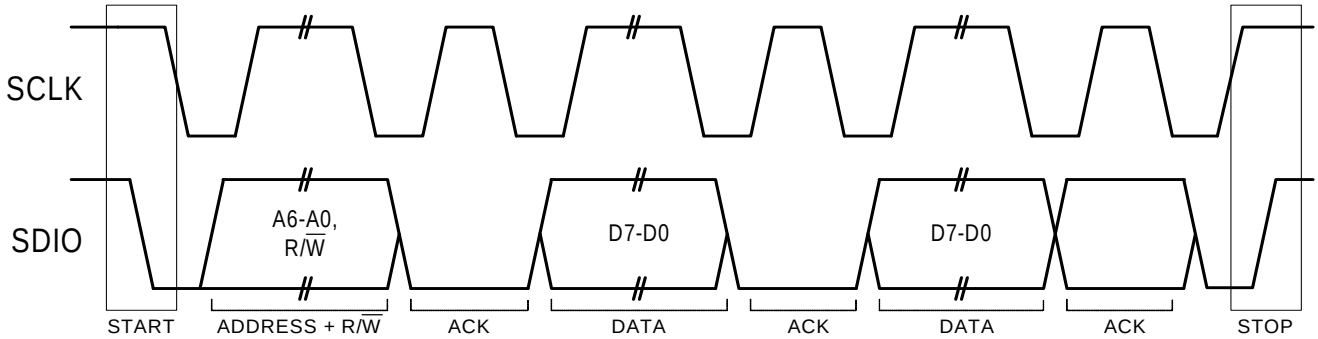



**Figure 3. 2-Wire Control Interface Read and Write Timing Diagram**

**Table 6. 3-Wire Control Interface Characteristics**
($V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK Frequency | $f_{CLK}$ | | 0 | — | 2.5 | MHz |
| SCLK High Time | $t_{HIGH}$ | | 25 | — | — | ns |
| SCLK Low Time | $t_{LOW}$ | | 25 | — | — | ns |
| SDIO Input, $\overline{SEN}$ to SCLK↑ Setup | $t_S$ | | 20 | — | — | ns |
| SDIO Input to SCLK↑ Hold | $t_{HSDIO}$ | | 10 | — | — | ns |
| $\overline{SEN}$ Input to SCLK↓ Hold | $t_{HSEN}$ | | 10 | — | — | ns |
| SCLK↑ to SDIO Output Valid | $t_{CDV}$ | Read | 2 | — | 25 | ns |
| SCLK↑ to SDIO Output High Z | $t_{CDZ}$ | Read | 2 | — | 25 | ns |
| SCLK, $\overline{SEN}$, SDIO, Rise/Fall time | $t_R$ $t_F$ | | — | — | 10 | ns |
| **Note:** When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$. | | | | | | |

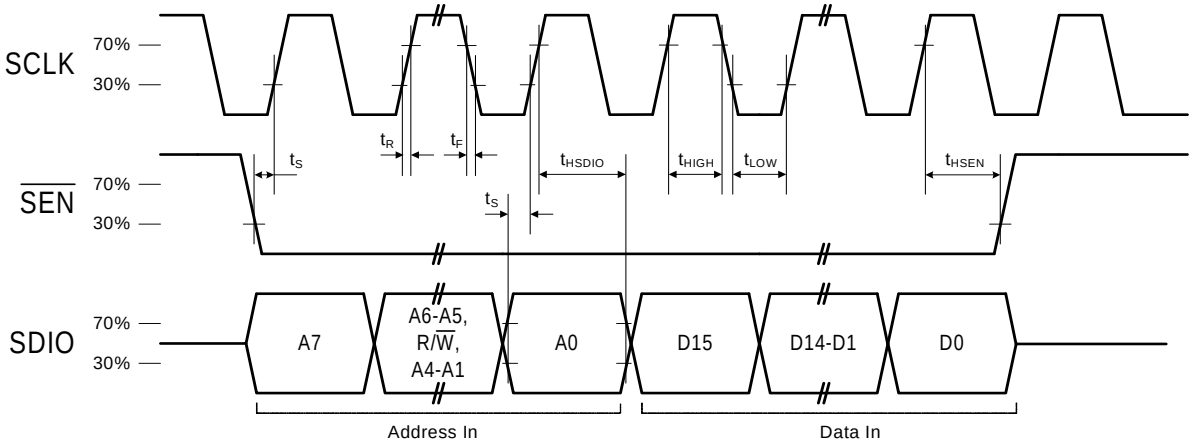



**Figure 4. 3-Wire Control Interface Write Timing Parameters**

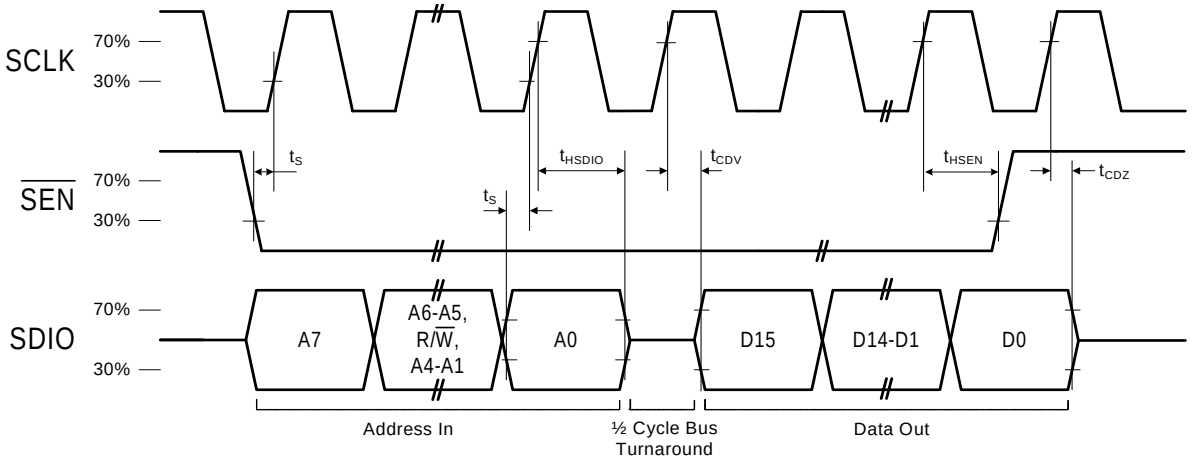



**Figure 5. 3-Wire Control Interface Read Timing Parameters**

**Table 7. SPI Control Interface Characteristics**
($V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK Frequency | $f_{CLK}$ | | 0 | — | 2.5 | MHz |
| SCLK High Time | $t_{HIGH}$ | | 25 | — | — | ns |
| SCLK Low Time | $t_{LOW}$ | | 25 | — | — | ns |
| SDIO Input, $\overline{SEN}$ to SCLK↑ Setup | $t_S$ | | 15 | — | — | ns |
| SDIO Input to SCLK↑ Hold | $t_{HSDIO}$ | | 10 | — | — | ns |
| $\overline{SEN}$ Input to SCLK↓ Hold | $t_{HSEN}$ | | 5 | — | — | ns |
| SCLK↓ to SDIO Output Valid | $t_{CDV}$ | Read | 2 | — | 25 | ns |
| SCLK↓ to SDIO Output High Z | $t_{CDZ}$ | Read | 2 | — | 25 | ns |
| SCLK, $\overline{SEN}$, SDIO, Rise/Fall time | $t_R$, $t_F$ | | — | — | 10 | ns |
| **Note:** When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$. | | | | | | |

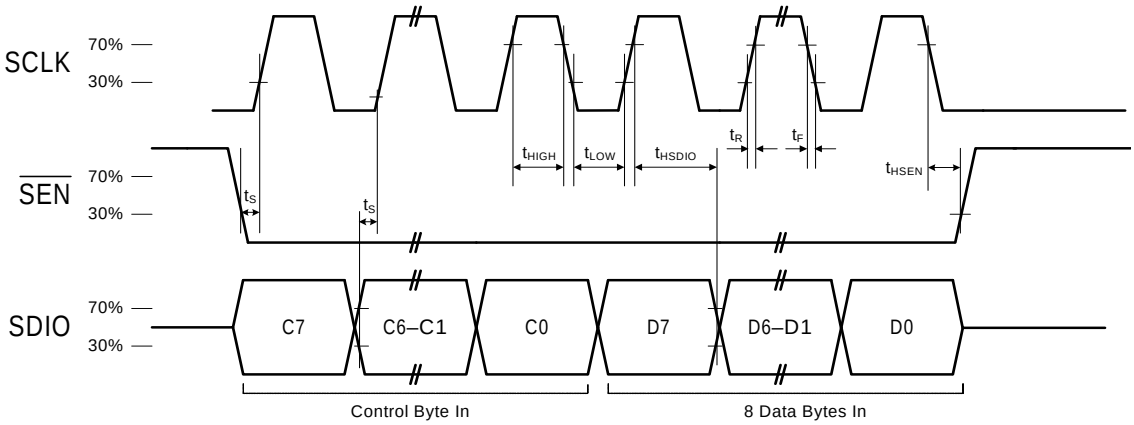



**Figure 6. SPI Control Interface Write Timing Parameters**

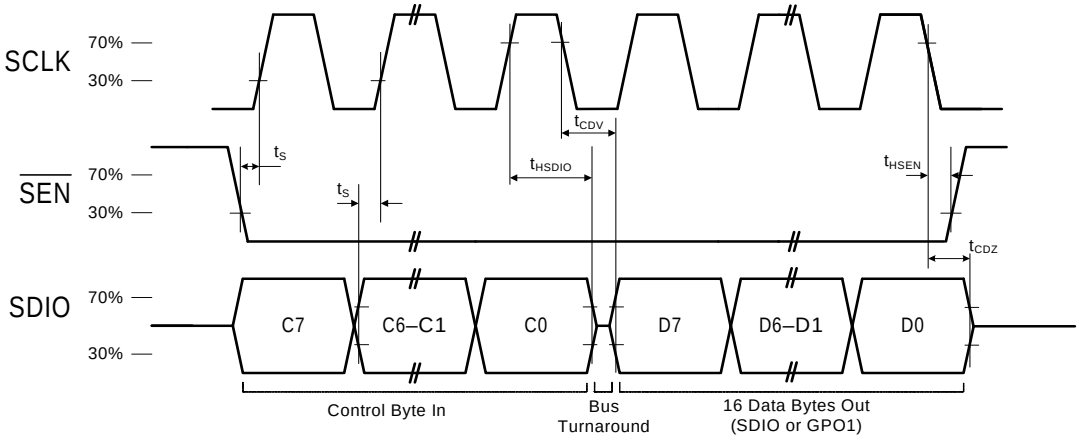



**Figure 7. SPI Control Interface Read Timing Parameters**

**Table 8. Digital Audio Interface Characteristics**
($V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DCLK pulse width high | $t_{DCH}$ | | 10 | — | — | ns |
| DCLK pulse width low | $t_{DCL}$ | | 10 | — | — | ns |
| DFS set-up time to DCLK rising edge | $t_{SU:DFS}$ | | 5 | — | — | ns |
| DFS hold time from DCLK rising edge | $t_{HD:DFS}$ | | 5 | — | — | ns |
| DIN set-up time from DCLK rising edge | $t_{SU:DIN}$ | | 5 | — | — | ns |
| DIN hold time from DCLK rising edge | $t_{HD:DIN}$ | | 5 | — | — | ns |
| DCLK, DFS, DIN, Rise/Fall time | $t_R$ $t_F$ | | — | — | 10 | ns |
| DCLK Tx Frequency[1,2] | | | 1.0 | — | 40.0 | MHz |

**Notes:**
1. Guaranteed by characterization.
2. The DCLK frequency may be set below the minimum specification if DIGITAL_INPUT_SAMPLE_RATE is first set to 0 (disable).

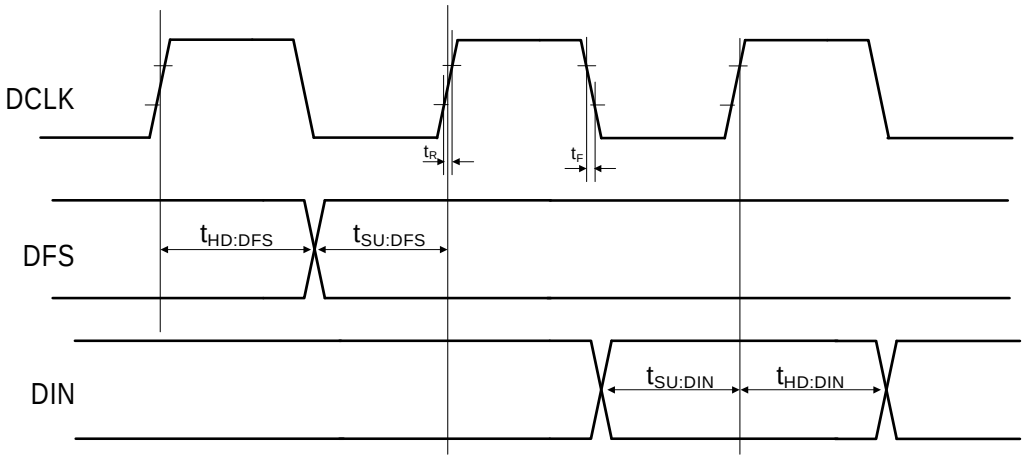



**Figure 8. Digital Audio Interface Timing Parameters, I²S Mode**

## Table 9. FM Transmitter Characteristics[1]

(Test conditions: $V_{RF}$ = 118 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, 75 µs pre-emphasis, unless otherwise specified.
Production test conditions: $V_{DD}$ = 3.3 V, $V_{IO}$ = 3.3 V, $T_A$ = 25 °C, $F_{RF}$ = 98 MHz.
Characterization test conditions: $V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C, $F_{RF}$ = 76–108 MHz.
All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
Typical values apply at $V_{DD}$ = 3.3 V and 25 °C unless otherwise stated.
Parameters are tested in production unless otherwise specified.)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit Frequency Range[2] | $f_{RF}$ | | 76 | — | 108 | MHz |
| Transmit Frequency Accuracy and Stability[2,3] | | | –3.5 | — | 3.5 | kHz |
| Transmit Voltage Accuracy[2] | | $V_{RF}$ = 103–117 dBµV | –2.5 | — | 2.5 | dB |
| Transmit Voltage Accuracy | | $V_{RF}$ = 102, 118 dBµV | –2.5 | — | 2.5 | dB |
| Transmit Voltage Temperature Coefficient[2] | | | –0.075 | — | –0.025 | dB/ºC |
| Transmit Channel Edge Power | | > ±100 kHz, pre-emphasis off | — | — | –20 | dBc |
| Transmit Adjacent Channel Power | | > ±200 kHz, pre-emphasis off | — | –30 | –26 | dBc |
| Transmit Alternate Channel Power | | > ±400 kHz, pre-emphasis off | — | –30 | –26 | dBc |
| Transmit Emissions | | In-band (76–108 MHz) | — | — | –30 | dBc |
| Output Capacitance Max[2] | $C_{tune}$ | | — | 53 | — | pF |
| Output Capacitance Min[2] | $C_{tune}$ | | — | 5 | — | pF |
| Pre-emphasis Time Constant[2] | | TX_PREMPHASIS = 75 µs | 70 | 75 | 80 | µs |
| | | TX_PREMPHASIS = 50 µs | 45 | 50 | 54 | µs |
| Audio SNR Mono[2] | | Δf = 22.5 kHz, Mono, limiter off | 58 | 63 | — | dB |
| Audio SNR Stereo | | Δf = 22.5 kHz, Δfpilot = 6.75 kHz, Stereo, limiter off | 53 | 58 | — | dB |
| Audio THD Mono | | Δf = 75 kHz, Mono, limiter off | — | 0.1 | 0.5 | % |
| Audio THD Stereo[2] | | Δf = 22.5 kHz, Δfpilot = 6.75 kHz, Stereo, limiter off | — | 0.1 | 0.5 | % |
| Audio Stereo Separation[2] | | left channel only | 30 | 35 | — | dB |

**Notes:**
1. FM transmitter performance specifications are subject to adherence to Silicon Laboratories guidelines in "AN383: Universal Antenna Selection and Layout Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested with test schematic (L = 120 nH, Q ≥ 30) shown in Figure 9 on page 14.
2. Guaranteed by characterization.
3. No measurable $\Delta fRF/\Delta V_{DD}$ at $\Delta V_{DD}$ of 500 mVpk-pk at 100 Hz to 10 kHz.

## Table 9. FM Transmitter Characteristics[1] (Continued)

(Test conditions: $V_{RF}$ = 118 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, 75 µs pre-emphasis, unless otherwise specified.
Production test conditions: $V_{DD}$ = 3.3 V, $V_{IO}$ = 3.3 V, $T_A$ = 25 °C, $F_{RF}$ = 98 MHz.
Characterization test conditions: $V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C, $F_{RF}$ = 76–108 MHz.
All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
Typical values apply at $V_{DD}$ = 3.3 V and 25 °C unless otherwise stated.
Parameters are tested in production unless otherwise specified.)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Sub Carrier Rejection Ratio | SCR | | 40 | 50 | — | dB |
| Powerup Settling Time[2] | | | — | — | 110 | ms |
| Input Signal Level[2] | $V_{AI}$ | | — | — | 0.636 | $V_{PK}$ |
| Frequency Flatness[2] | | Mono, ±1.5 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off | 30 | — | 15 k | Hz |
| High Pass Corner Frequency[2] | | Mono, –3 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off | 5 | — | 30 | Hz |
| Low Pass Corner Frequency[2] | | Mono, –3 dB, Δf = 75 kHz, 0, 50, 75 µs pre-emphasis, limiter off | 15 k | — | 16 k | Hz |
| Audio Imbalance | | Mono | –1 | — | 1 | dB |
| Pilot Modulation Rate Accuracy[2] | | Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo | –10 | — | 10 | % |
| Audio Modulation Rate Accuracy[2] | | Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo | –10 | — | 10 | % |
| Input Resistance[2] | | LIATTEN[1:0] = 11 | 50 | 60 | — | kΩ |
| Input Capacitance[2] | | | — | 10 | — | pF |

**Notes:**
1. FM transmitter performance specifications are subject to adherence to Silicon Laboratories guidelines in “AN383: Universal Antenna Selection and Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested with test schematic (L = 120 nH, Q ≥ 30) shown in Figure 9 on page 14.
2. Guaranteed by characterization.
3. No measurable $\Delta fRF/\Delta V_{DD}$ at $\Delta V_{DD}$ of 500 mVpk-pk at 100 Hz to 10 kHz.

## Table 10. Reference Clock Characteristics

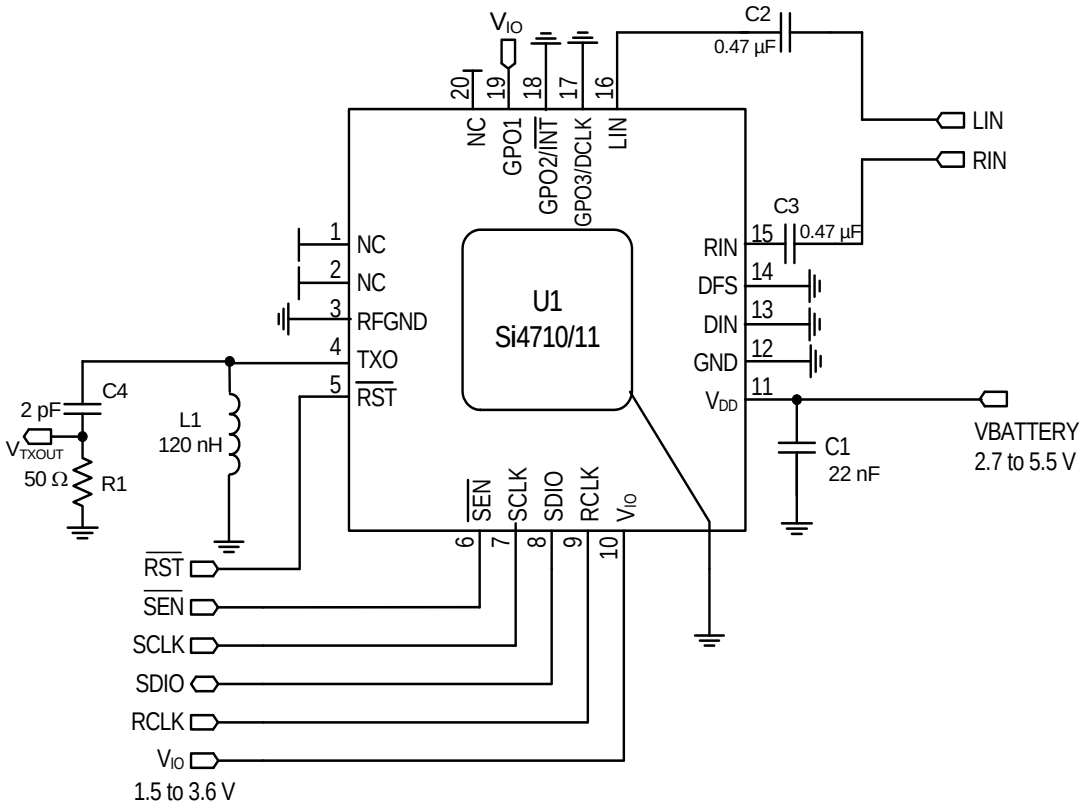
($V_{DD}$ = 2.7 to 5.5 V, $V_{IO}$ = 1.5 to 3.6 V, $T_A$ = –20 to 85 °C, $F_{RF}$ = 76–108 MHz)

| Supported Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RCLK Frequency Range[1,2] | | | 31.130 | 32.768 | 40,000 | kHz |
| Frequency Tolerance[1] | | | –50 | — | 50 | ppm |

**Notes:**
1. Guaranteed by characterization.
2. The RCLK frequency divided by an integer number (the prescaler value) must fall in the range of 31,130 to 34,406 Hz. Therefore, the range of RCLK frequencies is not continuous below frequencies of 311.3 kHz.

# 2. Test Circuit

## 2.1. Test Circuit Schematic




Notes:
1. Si4710/11 is shown configured in I²C compatible bus mode.
2. GPO2/INT can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN383: 3 mm x 3 mm QFN Universal Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. LIN, RIN line inputs must be ac-coupled.

**Figure 9. Test Circuit Schematic**

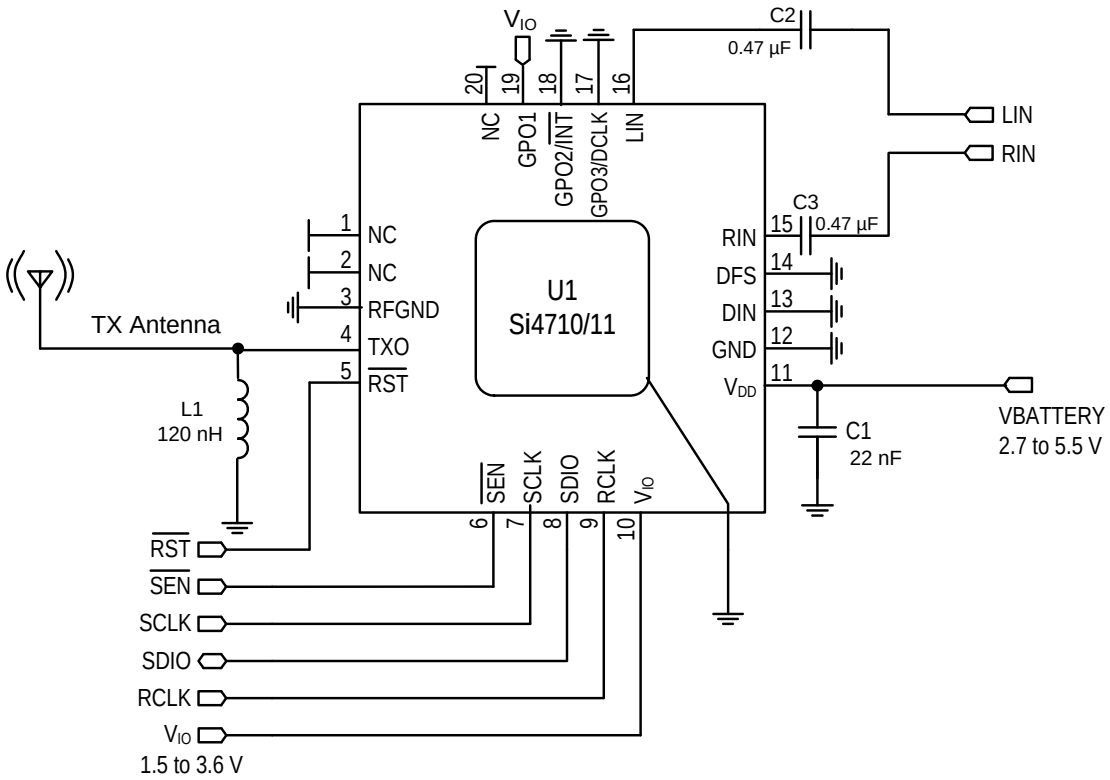
## 2.2. Test Circuit Bill of Materials

**Table 11. Si4710/11 Test Circuit Bill of Materials**

| Component(s) | Value/Description | Supplier(s) |
|---|---|---|
| C1 | Supply bypass capacitor, 22 nF, 20%, Z5U/X7R | Murata |
| C2, C3 | AC Coupling Capacitor, 0.47 µF | Murata |
| C4 | 2 pF, ±.05 pF, 06035JZR0AB | AVX |
| L1 | 120 nH inductor, Qmin = 30 | Murata |
| R1 | 49.9 Ω, 5% | Murata |
| U1 | Si4710/11 FM Radio Transmitter | Silicon Laboratories |

# 3. Typical Application Schematics

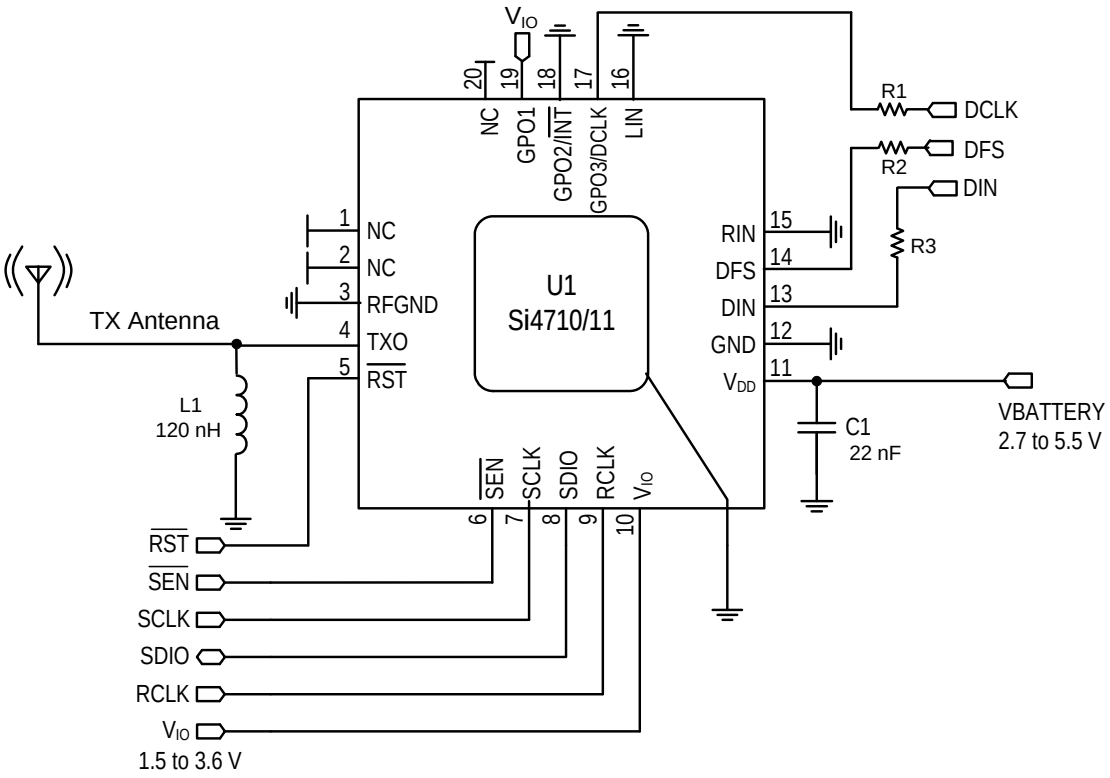
## 3.1. Analog Audio Inputs




Notes:
1. Si4710/11 is shown configured in I²C compatible bus mode.
2. GPO2/INT can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN383: 3 mm x 3 mm QFN Universal Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. LIN, RIN line inputs must be ac-coupled.

**Figure 10. Analog Audio Inputs (LIN, RIN)**

## 3.2. Digital Audio Inputs




Notes:
1. Si4710/11 is shown configured in I²C compatible bus mode.
2. GPO2/INT can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN383: Si47xx 3 mm x 3 mm QFN Universal Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.

**Figure 11. Digital Audio Inputs (DIN, DFS, DCLK)**

## 3.3. Typical Application Schematic Bill of Materials

**Table 12. Si4710/11 Bill of Materials**

| Component(s) | Value/Description | Supplier(s) |
|---|---|---|
| C1 | Supply bypass capacitor, 22 nF, 20%, Z5U/X7R | Murata |
| C2, C3 | AC Coupling Capacitor, 0.47 µF | Murata |
| L1 | 120 nH inductor, Qmin = 30 | Murata |
| R1, R2 | 2 kΩ Resistor | Any |
| R3 | 600 Ω Resistor | Any |
| U1 | Si4710/11 FM Radio Transmitter | Silicon Laboratories |

# 4. Universal AM/FM RX/FM TX Application Schematic

Figure 12 shows an application schematic that supports the Si47xx family of 3 mm x 3 mm QFN products, including the Si4702/3/4/5 FM receivers, Si471x FM transmitters, Si472x FM transceivers, and Si473x AM/FM receivers.

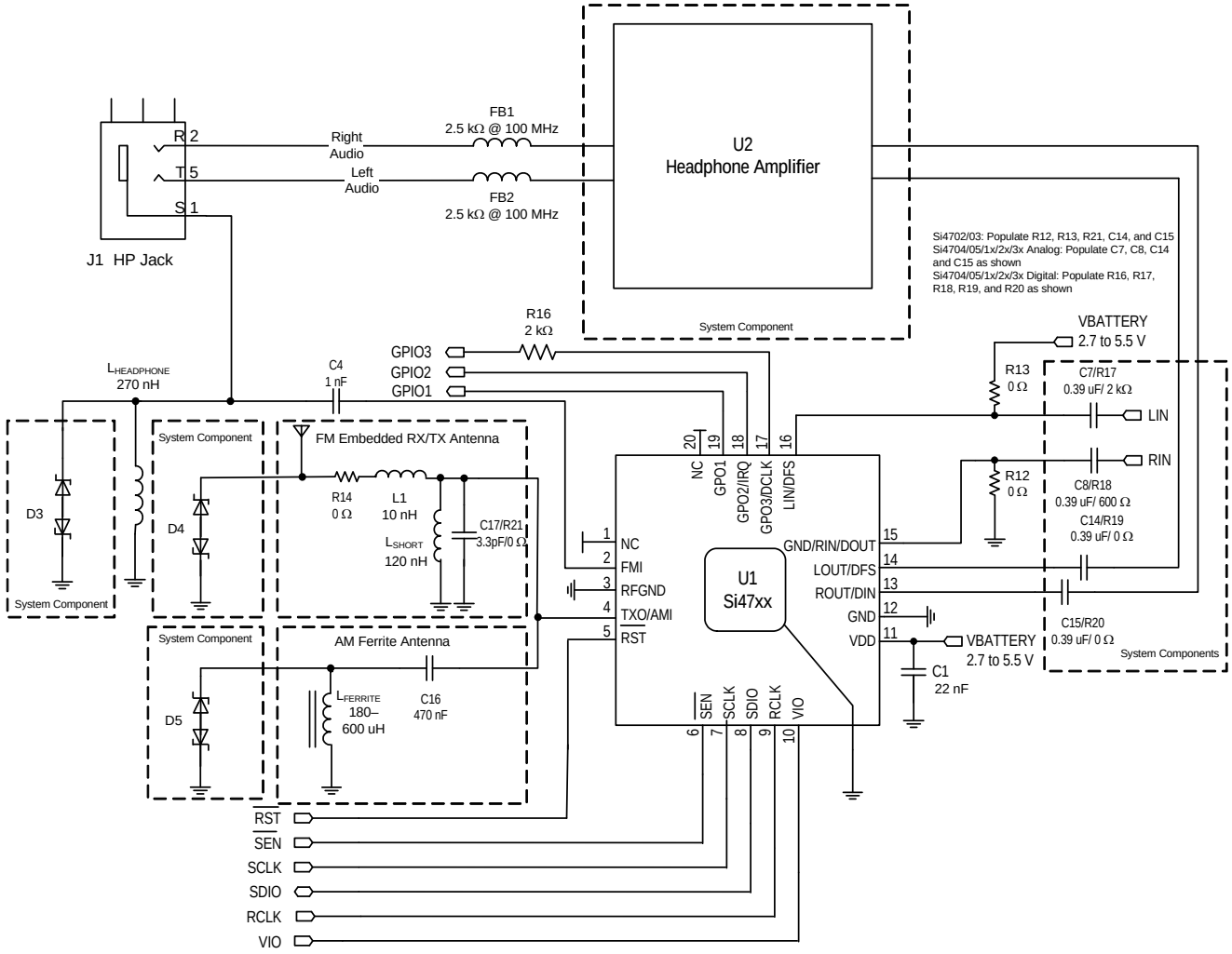



**Figure 12. Universal AM/FM RX/FM TX Application Schematic**

Following the schematic and layout recommendations detailed in “AN383: Universal Antenna Selection and Layout Guidelines” will result in optimal performance with the minimal application schematic shown in Figure 12. “Universal AM/FM RX/FM TX Application Schematic”. System components are those that are likely to be present for any tuner or transmitter design.

## 4.1. Universal AM/FM RX/FM TX Bill of Materials

The bill of materials for the expanded application schematic shown in Figure 12 is provided in Table 13. Refer to the individual device layout guides and antenna interface guides for a discussion of the purpose of each component.

**Table 13. Bill of Materials**

| Designator | Description | Note |
|---|---|---|
| C1 | Supply bypass capacitor, 22 nF, 10%, Z5U/X7R, 0402 | |
| U1 | Silicon Laboratories Si47xx, 3 mm x 3 mm, 20 pin, QFN | |
| R12, R13, R19, R20, R21 | 0 Ω jumper, 0402 | R12, R13, and R21 for Si4702/03 Only |
| C16 | AM antenna ac coupling capacitor, 470 nF, 20%, Z5U/X7R | AM Ferrite Antenna |
| LFERRITE | AM Ferrite loop stick, 180–600 µH | AM Ferrite Antenna |
| FB1,FB2 | Ferrite bead, 2.5 kΩ @ 100 MHZ, 0603, Murata BLM18BD252SN1D | Headphone Antenna |
| LHEADPHONE | Headphone antenna matching inductor, 270 nH, 0603, Q>15, Murata LQW18ANR27J00D | Headphone Antenna |
| LSHORT | Embedded antenna matching inductor, 120 nH, 0603, Q>30, Murata LQW18ANR12J00D | Embedded Antenna |
| R14 | Embedded antenna jumper, 2.2 Ω, 0402 | Optional |
| C2 | Supply bypass capacitor, 22 nF, 10%, Z5U/X7R, 0402 | Optional |
| C3 | Supply bypass capacitor, 100 nF, 10%, Z5U/X7R, 0402 | Optional |
| C5, C6 | Headphone amp output shunt capacitor, 100 pF, 10%, Z5U/X7R, 0402 | Optional |
| R7-R11 | Current limiting resistor, 20 Ω–2 kΩ, 0402 | Optional |
| C12, C13 | Crystal load capacitor, 22 pF, 5%, COG | Optional |
| X1 | Crystal, Epson FC-135 | Optional |
| C7, C8 | Si47xx input ac coupling capacitor, 0.39 µF, X7R/X5R, 0402 | System Component |
| D1-D5 | ESD Diode, SOT23-3, California Micro Devices CM1214-01ST | System Component |
| C11 | Supply bypass capacitor, 100 nF, 10%, Z5U/X7R, 0402 | Headphone Amplifier |
| C4 | Headphone antenna ac coupling capacitor, 1 nF, 10%, Z5U/X7R, 0402 | Headphone Antenna |
| C9, C10 | Headphone amp output ac coupling capacitor, 125 uF, X7R, 0805 | Headphone Amplifier |
| C14, C15 | Headphone amp input ac coupling capacitor, 0.39 µF, X7R/X5R, 0402 | Headphone Amplifier |
| R1,R2,R3,R4 | Headphone amp feedback/gain resistor, 20 kΩ, 0402 | Headphone Amplifier |
| R5, R6 | Headphone amp bleed resistor, 100 kΩ, 0402 | Headphone Amplifier |
| U2 | Headphone amplifier, National Semiconductor, LM4910MA | Headphone Amplifier |
| R16, R17 | Current limiting resistor, 2 kΩ, 0402 | System Component |
| R18 | Current limiting resistor, 600 Ω, 0402 | System Component |
| L1 | VCO filter inductor, 10 nH, 0603, Q>30, Murata, LQW18ANR01J00D | Optional |
| C17 | VCO filter capacitor, 3.3 pF, 0402, COG, Venkel, C0402COG2503R3JN | Optional |

# 5. Functional Description

## 5.1. Overview

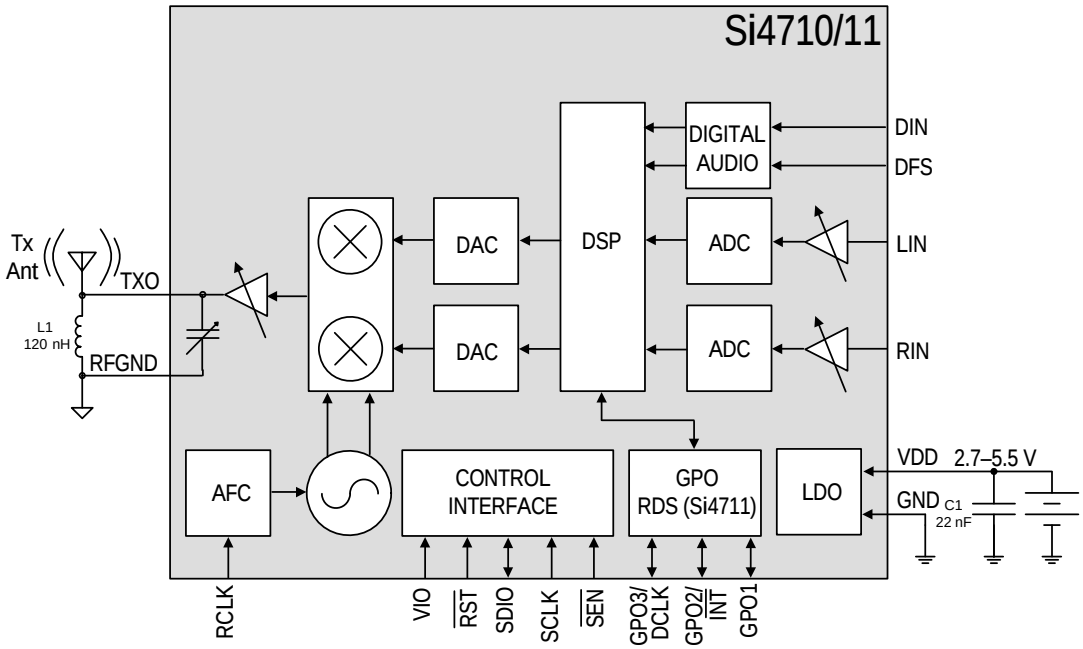



**Figure 13. Functional Block Diagram**

The Si4710/11 is the first 100% CMOS FM radio transmitter with integrated receive functionality to measure received signal strength. The device leverages Silicon Labs' highly successful and proven Si4700/01 FM receiver patent family and offers unmatched integration and performance, allowing FM transmit to be added to any portable device with a single chip. The Si4710/11 offers industry-leading size, performance, low power consumption, flexibility, and ease of use.

The Si4710/11's digital integration reduces the required external components of traditional offerings, resulting in a solution requiring only an external inductor and bypass capacitor, and PCB space of approximately 15 $mm^2$. This increases the device reliability and simplifies the design and manufacturing for companies adopting this technology.

The Si4710/11 performs FM modulation in the digital domain to achieve high fidelity, optimal performance versus power consumption, and flexibility of design. The onboard DSP provides modulation adjustment and audio dynamic range control for optimum sound quality.

The Si4711 supports the European Radio Data System (RDS) and the US Radio Broadcast Data System (RBDS) including all the symbol encoding, block synchronization, and error correction functions. Using this feature, the Si4711 enables data such as artist name and song title to be transmitted to an RDS/RBDS receiver.

The transmit output (TXO) connects directly to the transmit antenna with only one external inductor to provide harmonic filtering. The output is programmable over a 10 dB voltage range in 1 dB steps. The TXO output pin can also be configured for loop antenna support. Users are responsible for complying with local regulations on RF transmission (FCC, ETSI, ARIB, etc.).

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including $I^2S$ and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si4710/11 supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

The Si4710/11 includes a low-noise stereo line input

(LIN/RIN) with programmable attenuation. To ensure optimal audio performance, the Si4710/11 has a transmit line input property that allows the user to specify the peak amplitude of the analog input required to reach maximum deviation level. The deviation levels of the audio, pilot, and RDS/RBDS signals can be independently programmed to customize FM transmitter designs. The Si4710/11 has a programmable low audio level and high audio level indicators that allows the user to selectively enable and disable the carrier based on the presence of audio content. In addition, the device provides an overmodulation indicator to allow the user to dynamically set the maximum deviation level. The Si4710/11 has a programmable audio dynamic range control that can be used to reduce the dynamic range of the audio input signal and increase the volume at the receiver. These features can dramatically improve the end user's listening experience.

The Si4710/11 is reset by applying a logic low on the RST pin. This causes all register values to be reset to their default values. The digital input/output interface supply ($V_{IO}$) provides voltage to the RST, SEN, SDIO, RCLK, DIN, DFS, and DCLK pins and can be connected to the audio baseband processor's supply voltage to save power and remove the need for voltage level translators. RCLK is not required for register operation.

The Si4710/11 reference clock is programmable, supporting many RCLK inputs as shown in Table 9.

The Si4710/11 are part of a family of broadcast audio solutions offered in standard, 3 x 3 mm 20-pin QFN packages. All solutions are layout compatible, allowing a single PCB to accommodate various feature offerings.

The Si4710/11 includes line inputs to the on-chip analog-to-digital converters (ADC), a programmable reference clock input, and a configurable digital audio interface. The chip supports $I^2C$-compliant 2-wire, 8-bit SPI, and a 3-wire control interface.

## 5.2. FM Transmitter

The transmitter (TX) integrates a stereo audio ADC to convert analog audio signals to high fidelity digital signals. Alternatively, digital audio signals can be applied to the Si4710/11 directly to reduce power consumption by eliminating the need to convert audio baseband signals to analog and back again to digital. Digital signal processing is used to perform the stereo MPX encoding and FM modulation to a low digital IF. Transmit baseband filters suppress out-of-channel noise and images from the digital low-IF signal. A quadrature single-sideband mixer up-converts the digital IF signal to RF, and internal RF filters suppress noise and harmonics to support the harmonic emission requirements of cellular phones, GPS, WLAN, and other wireless standards.

The TXO output has over 10 dB of output level control, programmable in approximately 1 dB steps. This large output range enables a variety of antennas to be used for transmit, such as a monopole stub antenna or a loop antenna. The 1 dB step size provides fine adjustment of the output voltage.

The TXO output requires only one external 120 nH inductor. The inductor is used to resonate the antenna and is automatically calibrated within the integrated circuit to provide the optimum output level and frequency response for supported transmit frequencies. Users are responsible for adjusting their system's radiated power levels to comply with local regulations on RF transmission (FCC, ETSI, ARIB, etc.).

## 5.3. Digital Audio Interface

The digital audio interface operates in slave mode and supports 3 different audio data formats:

1. $I^2S$
2. Left-Justified
3. DSP Mode

### 5.3.1. Audio Data Formats

In $I^2S$ mode, the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The Left Channel is transferred first when the DFS is low, and the Right Channel is transferred when the DFS is high.

In Left-Justified mode, the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The Left Channel is transferred first when the DFS is high, and the Right Channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1 DCLK period. The Left Channel is transferred first, followed right away by the Right Channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word.

The number of audio bits can be configured for 8, 16, 20, or 24 bits.

### 5.3.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor. The sampling rate is selected using the DIGITAL_INPUT_SAMPLE_RATE property.

The device supports DCLK frequencies above 1 MHz. After powerup the DIGITAL_INPUT_SAMPLE_RATE property defaults to 0 (disabled). After DCLK is supplied, the DIGITAL_INPUT_SAMPLE_RATE property should be set to the desired audio sample rate such as 32, 40, 44.1, or 48 kHz. The DIGITAL_INPUT_SAMPLE_RATE property must be set to 0 before DCLK is removed or the DCLK frequency drops below 1 MHz. A device reset is required if this requirement is not followed.

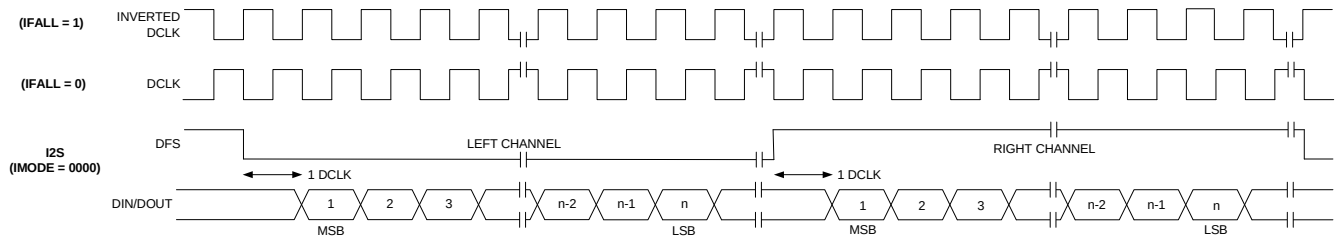



**Figure 14. I$^2$S Digital Audio Format**

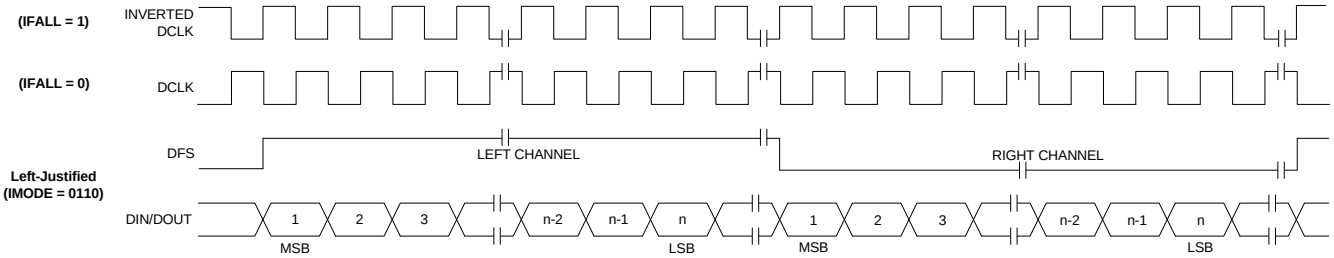



**Figure 15. Left-Justified Digital Audio Format**

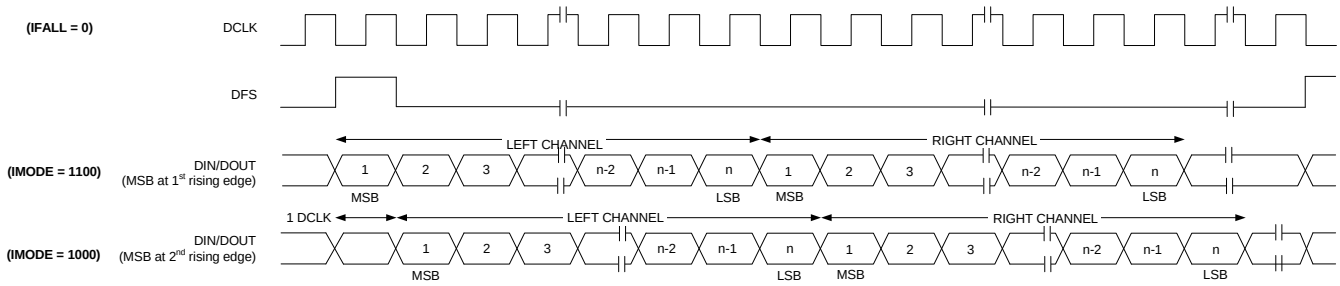



**Figure 16. DSP Digital Audio Format**

## 5.4. Line Input

The Si4710/11 provides left and right channel line inputs (LIN and RIN). The inputs are high-impedance and low-capacitance, suited to receiving line level signals from external audio baseband processors. Both line inputs are low-noise inputs with programmable attenuation. Passive and active anti-aliasing filters are incorporated to prevent high frequencies from aliasing into the audio band and degrading performance.

To ensure optimal audio performance, the Si4710/11 has a TX_LINE_INPUT_LEVEL property that allows the user to specify the peak amplitude of the analog input (LILEVEL[9:0]) required to reach the maximum deviation level programmed in the audio deviation property, TX_AUDIO_DEVIATION. A corresponding line input attenuation code, LIATTEN[1:0], is also selected by the expected peak amplitude level. Table 14 shows the line attenuation codes.

**Table 14. Line Attenuation Codes**

| LIATTEN[1:0] | Peak Input Voltage [mV] | RIN/LIN Input Resistance [kΩ] |
|---|---|---|
| 00 | 190 | 396 |
| 01 | 301 | 100 |
| 10 | 416 | 74 |
| 11 | 636 | 60 |

The line attenuation code is chosen by picking the lowest Peak Input Voltage in Table 14 that is just above the expected peak input voltage coming from the audio baseband processor. For example, if the expected peak input voltage from the audio baseband processor is 400 mV, the user chooses LIATTEN[1:0] = 10 since the Peak Input Voltage of 416 mV associated with LIATTEN[1:0] = 10 is just greater than the expected peak input voltage of 400 mV. The user also enters 400 mV into the LILEVEL[9:0] to associate this input level to the maximum frequency deviation level programmed into the audio deviation property. Note that selecting a particular value of LIATTEN[1:0] changes the input resistance of the LIN and RIN pins. This feature is used for cases where the expected peak input level exceeds the maximum input level of the LIN and RIN pins.

The maximum analog input level is 636 mVpK. If the analog input level from the audio baseband processor exceeds this voltage, series resistors must be inserted in front of the LIN and RIN pins to attenuate the voltage such that it is within the allowable operating range. For example, if the audio baseband's expected peak amplitude is 900 mV and the $V_{IO}$ supply voltage is 1.8 V, the designer can use 30 kΩ series resistors in front of the LIN and RIN pins and select LIATTEN[1:0] = 11. The resulting expected peak input voltage at the LIN/RIN pins is 600 mV, since this is just a voltage divider between the LIN/RIN input resistance (see Table 14, 60 kΩ for this example) and the external resistor. Note that the Peak Input Voltage corresponding to the chosen LIATTEN[1:0] code still needs to satisfy the condition of being just greater than the attenuated voltage. In this example, a line attenuation code of LIATTEN[1:0] = 11 has a Peak Input Voltage of 636 mV, which is just greater than the expected peak attenuated voltage of 600 mV. Also, the expected peak attenuated voltage is entered into the LILEVEL[9:0] parameter. Again, in this example, 600 mV is entered into LILVEVEL[9:0]. This example shows one possible solution, but many other solutions exist. The optimal solution is to apply the largest possible voltage to the LIN and RIN pins for signal-to-noise considerations; however, practical resistor values may limit the choices.

Note that the TX_LINE_INPUT_LEVEL parameter will affect the high-pass filter characteristics of the ac-coupling capacitors and the resistance of the audio inputs.

The Si4710/11 has a programmable low audio level and high audio level indicators that allows the user to selectively enable and disable the carrier based on the presence of audio content. The TX_ASQ_LEVEL_LOW and TX_ASQ_LEVEL_HIGH parameters set the low level and high level thresholds in dBFS, respectively. The time required for the audio level to be below the low threshold is set with the TX_ASQ_DURATION_LOW parameter, and similarly, the time required for the audio level to be above the high threshold is set with the TX_ASQ_DURATION_HIGH parameter.

## 5.5. Audio Dynamic Range Control

The Si4710/11 includes digital audio dynamic range control with programmable gain, threshold, attack rate, and release rate. The total dynamic range reduction is set by the gain value and the audio output compression above the threshold is equal to Threshold/(Gain + Threshold) in dB. The gain specified cannot be larger than the absolute value of the threshold. This feature can also be disabled if audio compression is not desired.

The audio dynamic range control can be used to reduce the dynamic range of the audio signal, which improves the listening experience on the FM receiver. Audio dynamic range reduction increases the transmit volume by decreasing the peak amplitudes of audio signals and increasing the root mean square content of the audio signal. In other words, it amplifies signals below a threshold by a fixed gain and compresses audio signals above a threshold by the ratio of Threshold/(Gain + Threshold). Figure 17 shows an example transfer function of an audio dynamic range controller with the threshold set at –40 dBFS and a Gain = 20 dB relative to an uncompressed transfer function.

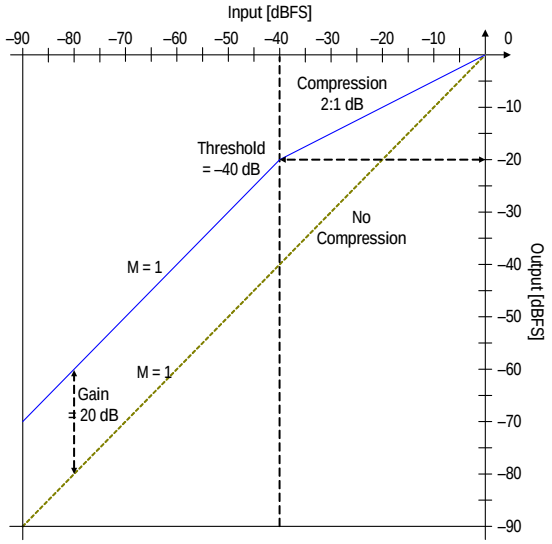



**Figure 17. Audio Dynamic Range Transfer Function**

For input signals below the threshold of –40 dBFS, the output signal is amplified or gained up by 20 dB relative to an uncompressed signal. Audio inputs above the threshold are compressed by a 2 to 1 dB ratio, meaning that every 2 dB increase in audio input level above the threshold results in an audio output increase of 1 dB. In this example, the input dynamic range of 90 dB is reduced to an output dynamic range of 70 dB.

Figure 18 shows the time domain characteristics of the audio dynamic range controller. The attack rate sets the speed with which the audio dynamic range controller responds to changes in the input level, and the release rate sets the speed with which the audio dynamic range controller returns to no compression once the audio input level drops below the threshold.

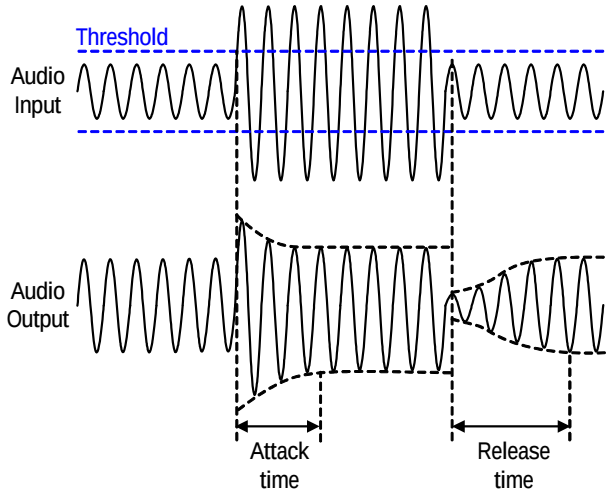



**Figure 18. Time Domain Characteristics of the Audio Dynamic Range Controller**

## 5.6. Audio Limiter

The Si4710/11 also includes a digital audio limiter. The audio limiter prevents over-modulation of the FM transmit output by dynamically attenuating peaks in the audio input signal that exceed a programmable threshold. The limiter threshold is set to the programmed audio deviation + ten percent. The threshold ensures that the output signal audio deviation does not exceed the programmed levels, avoiding audible artifacts or distortion in the target FM receiver, and complying with FCC or ETSI regulatory standards.

The limiter performs as a peak detector with an attack rate set to one audio sample, resulting in an almost immediate attenuation of the input peak. The recover rate is programmable to the customer's preference, and is set by default to 5 ms. This is the recommended setting to avoid audible pumping or popping. Please refer to "AN332: Universal Programming Guide."

## 5.7. Pre-Emphasis and De-Emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter that attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The pre-emphasis time constant is programmable to 50 or 75 µs and is set by using the TX_PREEMPHASIS property.

## 5.8. RDS/RBDS Processor (Si4711 Only)

The Si4711 implements an RDS/RBDS* processor for symbol encoding, block synchronization, and error correction. Digital data can be transmitted with the Si4711 RDS/RBDS encoding feature.

RDS transmission is supported with three different modes. The first mode is the simplest mode and requires no additional user support except for pre-loading the desired RDS PI and PTY codes and up to 12 8-byte PS character strings. The Si4711 will transmit the PI code and rotate through the transmission of the PS character strings with no further control required from outside the device. The second mode allows for more complicated transmissions. The PI and PTY codes are written to the device as in mode 1. The remaining blocks (B, C, and D) are written to a 252 byte buffer. This buffer can hold 42 sets of BCD blocks. The Si4711 creates RDS groups by creating block A from the PI code, concatenating blocks BCD from the buffer, and rotating through the buffer. The BCD buffer is circular; so, the pattern is repeated until the buffer is changed. Finally, the third mode allows the outside controller to burst data into the BCD buffer, which emulates a FIFO. The data does not repeat, but, when the buffer is nearly empty, the Si4711 signals the outside device to initiate another data burst. This mode permits the outside device to use any RDS functionality (including open data applications) that it wants.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

## 5.9. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to upconvert the low intermediate frequency to RF. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during transmission.

The tuning frequency can be directly programmed with commands. For example, to tune to 98.1 MHz, the user writes the TX_TUNE_FREQ command with an argument = 9810.

The Si4710/11 supports channel spacing of 50, 100, or 200 kHz.

## 5.10. Reference Clock

The Si4710/11 reference clock is programmable, supporting RCLK frequencies from 31.130 kHz to 40 MHz. The RCLK frequency divided by an integer number (the prescaler value) must fall in the range of 31,130 to 34,406 Hz. Therefore, the range of RCLK frequencies is not continuous below frequencies of 311.3 kHz. The default RCLK frequency is 32.768 kHz. Please refer to "AN332: Universal Programming Guide" for using other RCLK frequencies.

## 5.11. Control Interface

A serial port slave interface is provided; this allows an external controller to send commands to the Si4710/11 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, SPI mode, or 3-wire mode. The Si4710/11 selects the bus mode by sampling the state of the GPO1 and GPO2/$\overline{\text{INT}}$ pins on the rising edge of $\overline{\text{RST}}$. The GPO1 pin includes an internal pull-up resistor that is connected while $\overline{\text{RST}}$ is low, and the GPO2/$\overline{\text{INT}}$ pin includes an internal pull-down resistor that is connected while $\overline{\text{RST}}$ is low. Therefore, it is only necessary for the user to actively drive pins that differ from these states.

**Table 15. Bus Mode Select on Rising Edge of RST**

| Bus Mode | GPO1 | GPO2/INT |
|---|---|---|
| 2-Wire | 1 | 0 |
| SPI | 1 | 1 (must drive) |
| 3-Wire | 0 (must drive) | 0 |

After the rising edge of RST, the pins, GPO1 and GPO2/INT, are used as general-purpose output (O) pins as described in Section "5.12. GPO Outputs". In any bus mode, commands may only be sent after $V_{IO}$ and $V_{DD}$ supplies are applied.

### 5.11.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of RST.

2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a seven bit device address followed by a read/write bit (read = 1, write = 0). The Si4710/11 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4710/11 responds to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the seven-bit device address is 0010001. When SEN = 1, the address is 1100011.

For write operations, the user then sends an eight bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4710/11 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to eight data bytes in a single two-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4710/11 has acknowledged the control byte, it drives an eight-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction ends. The user may read up to 16 data bytes in a single two-wire transaction. These bytes contain the response data from the Si4710/11.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 5, "2-Wire Control Interface Characteristics[1,2,3]," on page 7, Figure 2, "2-Wire Control Interface Read and Write Timing Parameters," on page 8, and Figure 3, "2-Wire Control Interface Read and Write Timing Diagram," on page 8.

### 5.11.2. SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

SPI bus mode uses the SCLK, SDIO, and SEN pins for read/write operations. For reads, the user can choose to receive data from the device on either SDIO or GPO1. A transaction begins when the user drives SEN low. The user then pulses SCLK eight times while driving an 8-bit control byte (MSB first) serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of these values:

0x48 = write eight command/argument bytes (user drives write data on SDIO)

0x80 = read status byte (device drives read data on SDIO)

0xA0 = read status byte (device drives read data on GPO1)

0xC0 = read 16 response bytes (device drives read data on SDIO)

0xE0 = read 16 response bytes (device drives read data on GPO1)

When writing a command, after the control byte has been written, the user must drive exactly eight data bytes (a command byte and seven argument bytes) on SDIO. The data will be captured by the device on the rising edges of SCLK. After all eight data bytes have been written, the user raises SEN after the last falling edge of SCLK to end the transaction.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high). In SPI mode, this is done by sending control byte 0x80 or 0xA0, followed by reading a single byte on SDIO or GPO1. The Si4710/11 changes the state of SDIO or GPO1 after the falling edges of SCLK. Data should be captured by the user on the rising edges of SCLK. After the status byte has been read, the user raises SEN after the last falling edge of SCLK to end the transaction.

When reading a response, the user must read exactly 16 data bytes after sending the control byte. It is recommended that the user keep SEN low until all bytes

have transferred. However, it will not disrupt the protocol if SEN temporarily goes high at any time, as long as the user does not change the state of SCLK while SEN is high. After 16 bytes have been read, the user raises SEN after the last falling edge of SCLK to end the transaction.

At the end of any SPI transaction, the user must drive SEN high after the final falling edge of SCLK. At any time during a transaction, if SEN is sampled high by the device on a rising edge of SCLK, the transaction will be aborted. When SEN is high, SCLK may toggle without affecting the device.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 10.

#### 5.11.3. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

3-wire bus mode uses the SCLK, SDIO and SEN pins. A transaction begins when the system controller drives SEN low. Next, the system controller drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word is comprised of a three bit chip address (A7:A5 = 101b), a read/write bit (write = 0, read = 1), the chip address (A4 = 0), and a four bit register address (A3:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turnaround. Next, the Si4710/11 drives the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9, Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

## 5.12. GPO Outputs

The Si4710/11 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-Z. The GPO pins are multiplexed with the bus mode pins or DCLK depending on the application schematic of the transmitter. GPO2/INT can be configured to provide interrupts.

## 5.13. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset and place it in powerdown mode.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry and keep the bus active. For more information concerning Reset, Powerup, Powerdown, and Initialization, refer to “AN332: Universal Programming Guide”.

## 5.14. Programming with Commands

To ease development time and offer maximum customization, the Si4710/11 provides a simple yet powerful software interface to program the transmitter. The device is programmed using commands, arguments, properties, and responses.

To perform an action, the user writes a command byte and associated arguments causing the chip to execute the given command. Commands control actions, such as powering up the device, shutting down the device, or tuning to a station. Arguments are specific to a given command and are used to modify the command. For example, after the TX_TUNE_FREQ command, arguments are required to set the tune frequency. A complete list of commands is available in Table 16, “Si471x Command Summary,” on page 28.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are TX_PREEMPHASIS and GPO_CONFIGURE. A complete list of properties is available in Table 17, “Si471x Property Summary,” on page 29.

Responses provide the user information and are echoed after a command and associated arguments are issued. At a minimum, all commands provide a one-byte status update indicating interrupt and clear-to-send status information. For a detailed description of using the commands and properties of the Si4710/11, see “AN332: Universal Programming Guide.”

# 6. Commands and Properties

**Table 16. Si471x Command Summary**

| Cmd | Name | Description |
|---|---|---|
| 0x01 | POWER_UP | Power up device and mode selection. Modes include FM transmit and analog/digital audio interface configuration. |
| 0x10 | GET_REV | Returns revision information on the device. |
| 0x11 | POWER_DOWN | Power down device. |
| 0x12 | SET_PROPERTY | Sets the value of a property. |
| 0x13 | GET_PROPERTY | Retrieves a property's value. |
| 0x14 | GET_INT_STATUS | Read interrupt status bits. |
| 0x15 | PATCH_ARGS | Reserved command used for patch file downloads. |
| 0x16 | PATCH_DATA | Reserved command used for patch file downloads. |
| 0x30 | TX_TUNE_FREQ | Tunes to given transmit frequency. |
| 0x31 | TX_TUNE_POWER | Sets the output power level and tunes the antenna capacitor |
| 0x33 | TX_TUNE_STATUS | Queries the status of a previously sent TX Tune Freq, TX Tune Power, or TX Tune Measure command. |
| 0x34 | TX_ASQ_STATUS | Queries the TX status and input audio signal metrics. |
| 0x35 | TX_RDS_BUFF | **Si4711 Only**. Queries the status of the RDS Group Buffer and loads new data into buffer. |
| 0x36 | TX_RDS_PS | **Si4711 Only**. Set up default PS strings. |
| 0x80 | GPO_CTL | Configures GPO3 as output or Hi-Z. |
| 0x81 | GPO_SET | Sets GPO3 output level (low or high). |

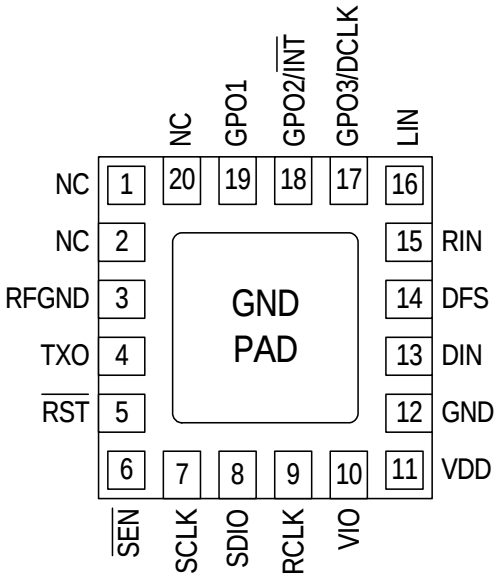
**Table 17. Si471x Property Summary**

| Prop | Name | Description | Default |
|---|---|---|---|
| 0x0001 | GPO_IEN | Enables interrupt sources. | 0x0000 |
| 0x0101 | DIGITAL_INPUT _FORMAT | Configures the digital input format. | 0x0000 |
| 0x0103 | DIGITAL_INPUT _SAMPLE_RATE | Configures the digital input sample rate in 10 Hz steps. Default is 0. | 0x0000 |
| 0x0201 | REFCLK_FREQ | Sets frequency of the reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz. | 0x8000 |
| 0x0202 | REFCLK_PRESCALE | Sets the prescaler value for the reference clock. | 0x0001 |
| 0x2100 | TX_COMPONENT_ENABLE | Enable transmit multiplex signal components. Default has pilot and L-R enabled. | 0x0003 |
| 0x2101 | TX_AUDIO_DEVIATION | Configures audio frequency deviation level. Units are in 10 Hz increments. Default is 6285 (68.25 kHz). | 0x1AA9 |
| 0x2102 | TX_PILOT_DEVIATION | Configures pilot tone frequency deviation level. Units are in 10 Hz increments. Default is 675 (6.75 kHz) | 0x02A3 |
| 0x2103 | TX_RDS_DEVIATION | **Si4711 Only.** Configures the RDS/RBDS frequency deviation level. Units are in 10 Hz increments. Default is 2 kHz. | 0x00C8 |
| 0x2104 | TX_LINE_INPUT_LEVEL | Configures maximum analog line input level to the LIN/RIN pins to reach the maximum deviation level programmed into the audio deviation property TX Audio Deviation. Default is 636 $mV_{PK}$. | 0x327C |
| 0x2105 | TX_LINE_INPUT_MUTE | Sets line input mute. L and R inputs may be independently muted. Default is not muted. | 0x0000 |
| 0x2106 | TX_PREEMPHASIS | Configures pre-emphasis time constant. Default is 0 (75 µS). | 0x0000 |
| 0x2107 | TX_PILOT_FREQUENCY | Configures the frequency of the stereo pilot. Default is 19000 Hz. | 0x4A38 |
| 0x2200 | TX_ACOMP_ENABLE | Enables audio dynamic range control. Default is 0 (disabled). | 0x0002 |
| 0x2201 | TX_ACOMP_THRESHOLD | Sets the threshold level for audio dynamic range control. Default is –40 dB. | 0xFFD8 |
| 0x2202 | TX_ACOMP_ATTACK_TIME | Sets the attack time for audio dynamic range control. Default is 0 (0.5 ms). | 0x0000 |
| 0x2203 | TX_ACOMP_RELEASE_TIME | Sets the release time for audio dynamic range control. Default is 4 (1000 ms). | 0x0004 |
| 0x2204 | TX_ACOMP_GAIN | Sets the gain for audio dynamic range control. Default is 15 dB. | 0x000F |
| 0x2205 | TX_LIMITER_RELEASE_TIME | Sets the limiter release time. Default is 102 (5.01 ms) | 0x0066 |
| 0x2300 | TX_ASQ_INTERRUPT_SOURCE | Configures measurements related to signal quality metrics. Default is none selected. | 0x0000 |
| 0x2301 | TX_ASQ_LEVEL_LOW | Configures low audio input level detection threshold. This threshold can be used to detect silence on the incoming audio. | 0x0000 |

**Table 17. Si471x Property Summary (Continued)**

| Prop | Name | Description | Default |
|---|---|---|---|
| 0x2302 | TX_ASQ_DURATION_LOW | Configures the duration which the input audio level must be below the low threshold in order to detect a low audio condition. | 0x0000 |
| 0x2303 | TX_ASQ_LEVEL_HIGH | Configures high audio input level detection threshold. This threshold can be used to detect activity on the incoming audio. | 0x0000 |
| 0x2304 | TX_ASQ_DURATION_HIGH | Configures the duration which the input audio level must be above the high threshold in order to detect a high audio condition. | 0x0000 |
| 0x2C00 | TX_RDS_INTERRUPT_SOURCE | **Si4711 Only.** Configure RDS interrupt sources. Default is none selected. | 0x0000 |
| 0x2C01 | TX_RDS_PI | **Si4711 Only.** Sets transmit RDS program identifier. | 0x40A7 |
| 0x2C02 | TX_RDS_PS_MIX | **Si4711 Only.** Configures mix of RDS PS Group with RDS Group Buffer. | 0x0003 |
| 0x2C03 | TX_RDS_PS_MISC | **Si4711 Only.** Miscellaneous bits to transmit along with RDS_PS Groups. | 0x1008 |
| 0x2C04 | TX_RDS_PS_REPEAT_COUNT | **Si4711 Only.** Number of times to repeat transmission of a PS message before transmitting the next PS message. | 0x0003 |
| 0x2C05 | TX_RDS_PS_MESSAGE_COUNT | **Si4711 Only.** Number of PS messages in use. | 0x0001 |
| 0x2C06 | TX_RDS_PS_AF | **Si4711 Only.** RDS Program Service Alternate Frequency. This provides the ability to inform the receiver of a single alternate frequency using AF Method A coding and is transmitted along with the RDS_PS Groups. | 0xE0E0 |
| 0x2C07 | TX_RDS_FIFO_SIZE | **Si4711 Only.** Number of blocks reserved for the FIFO. Note that the value written must be one larger than the desired FIFO size. | 0x0000 |

## 7. Pin Descriptions: Si4710/11-GM




| Pin Number(s) | Name | Description |
|---|---|---|
| 1, 2, 20 | NC | No connect. Leave floating. |
| 3 | RFGND | RF ground. Connect to ground plane on PCB. |
| 4 | TXO | FM transmit output connection to transmit antenna. |
| 5 | RST | Device reset (active low) input. |
| 6 | SEN | Serial enable input (active low). |
| 7 | SCLK | Serial clock input. |
| 8 | SDIO | Serial data input/output. |
| 9 | RCLK | External reference oscillator input. |
| 10 | $V_{IO}$ | I/O supply voltage. |
| 11 | $V_{DD}$ | Supply voltage. May be connected directly to battery. |
| 13 | DIN | Digital input data. |
| 14 | DFS | Digital frame synchronization input. |
| 15 | RIN | Right audio line input. |
| 16 | LIN | Left audio line input. |
| 17 | GPO3/DCLK | General purpose output/digital bit synchronous clock input. |
| 18 | GPO2/$\overline{INT}$ | General purpose output/interrupt request. |
| 19 | GPO1 | General purpose output. |
| 12, GND PAD | GND | Ground. Connect to ground plane on PCB. |

## 8. Ordering Guide

| Part Number* | Description | Package Type | Operating Temperature |
|---|---|---|---|
| Si4710-B30-GM | Portable broadcast FM transmitter | QFN<br>Pb-free | –20 to 85 °C |
| Si4711-B30-GM | Portable broadcast FM transmitter with RDS/RBDS encoder | QFN<br>Pb-free | –20 to 85 °C |
| ***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel. | | | |

# 9. Package Markings (Top Marks)

## 9.1. Si4710 Top Mark

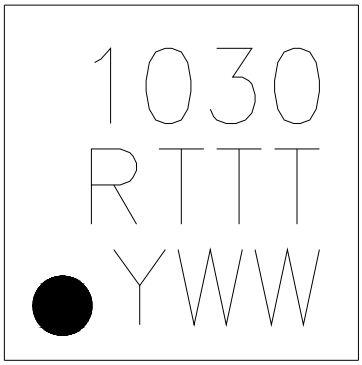



**Figure 19. Si4710 Top Mark**

## 9.2. Si4711 Top Mark

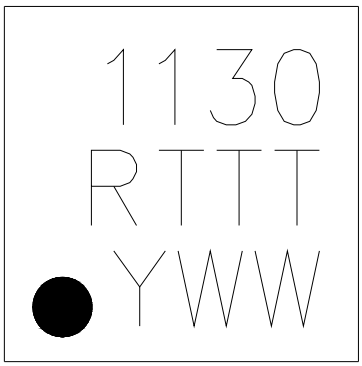



**Figure 20. Si4711 Top Mark**

## 9.3. Top Mark Explanation

| | | |
|---|---|---|
| **Mark Method:** | YAG Laser | |
| **Line 1 Marking:** | Part Number | 10 = Si4710<br>11 = Si4711 |
| | Firmware Revision | 30 = Firmware Revision 30 |
| **Line 2 Marking:** | R = Die Revision | B = Revision B Die |
| | TTT = Internal Code | Internal tracking code. |
| **Line 3 Marking:** | Circle = 0.5 mm Diameter (Bottom-Left Justified) | Pin 1 Identifier |
| | Y = Year<br>WW = Workweek | Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date. |

## 10. Package Outline: Si4710/11-GM

Figure 21 illustrates the package details for the Si4710/11. Table 18 lists the values for the dimensions shown in the illustration.

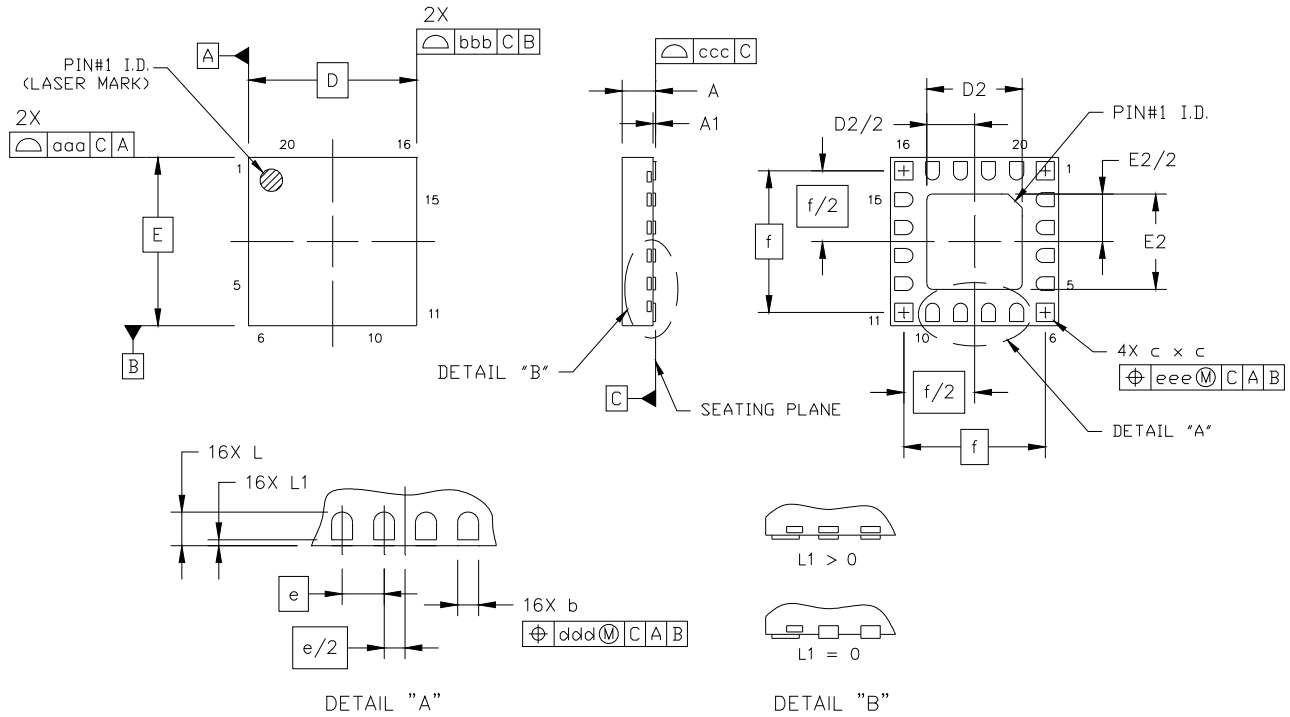



**Figure 21. 20-Pin Quad Flat No-Lead (QFN)**

**Table 18. Package Dimensions**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| c | 0.27 | 0.32 | 0.37 |
| D | 3.00 BSC | | |
| D2 | 1.65 | 1.70 | 1.75 |
| e | 0.50 BSC | | |
| E | 3.00 BSC | | |
| E2 | 1.65 | 1.70 | 1.75 |

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| f | 2.53 BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| L1 | 0.00 | — | 0.10 |
| aaa | — | — | 0.05 |
| bbb | — | — | 0.05 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| eee | — | — | 0.10 |

**Notes:**

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

## 11. PCB Land Pattern: Si4710/11-GM

Figure 22 illustrates the PCB land pattern details for the Si4710/11-GM. Table 19 lists the values for the dimensions shown in the illustration.

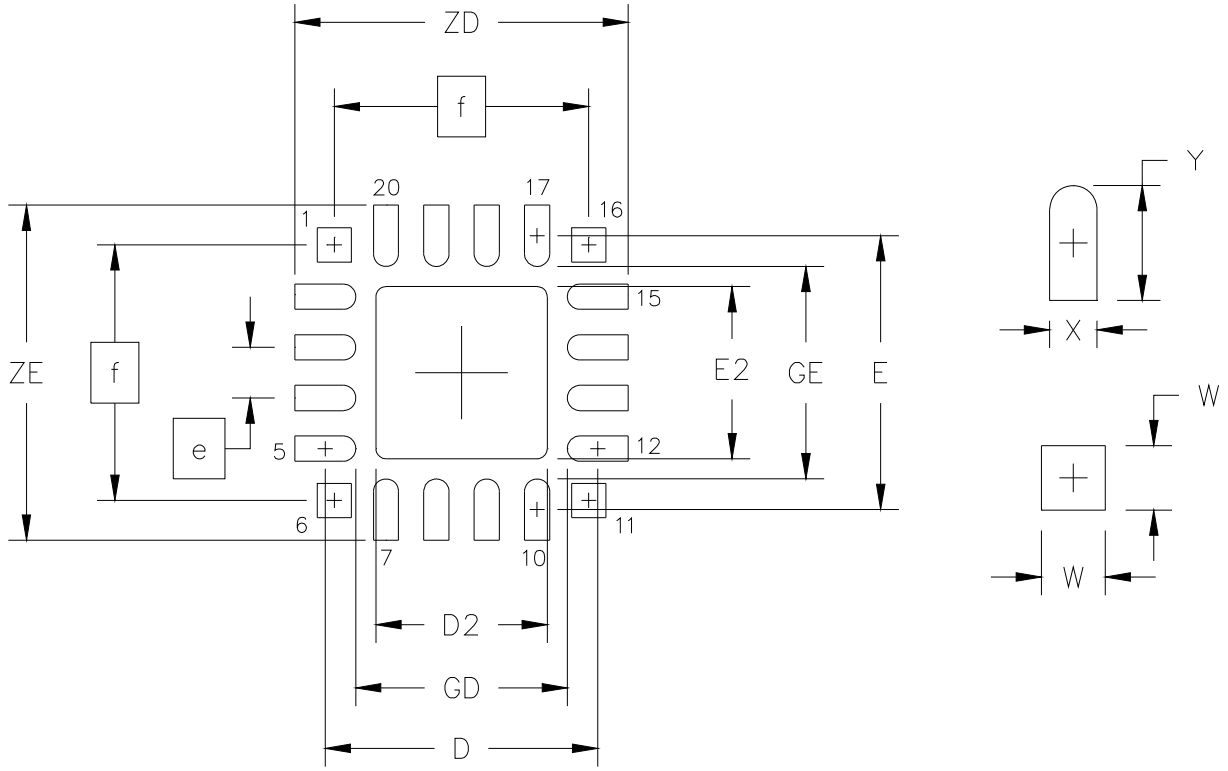



**Figure 22. PCB Land Pattern**

**Table 19. PCB Land Pattern Dimensions**

| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| D | 2.71 REF | |
| D2 | 1.60 | 1.80 |
| e | 0.50 BSC | |
| E | 2.71 REF | |
| E2 | 1.60 | 1.80 |
| f | 2.53 BSC | |
| GD | 2.10 | — |

| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| GE | 2.10 | — |
| W | — | 0.34 |
| X | — | 0.28 |
| Y | 0.61 REF | |
| ZE | — | 3.31 |
| ZD | — | 3.31 |

**Notes: General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing is per the ANSI Y14.5M-1994 specification.
3. This land pattern design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.

**Note: Solder Mask Design**

1. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

**Notes: Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component standoff.

**Notes: Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

## 12. Additional Reference Resources

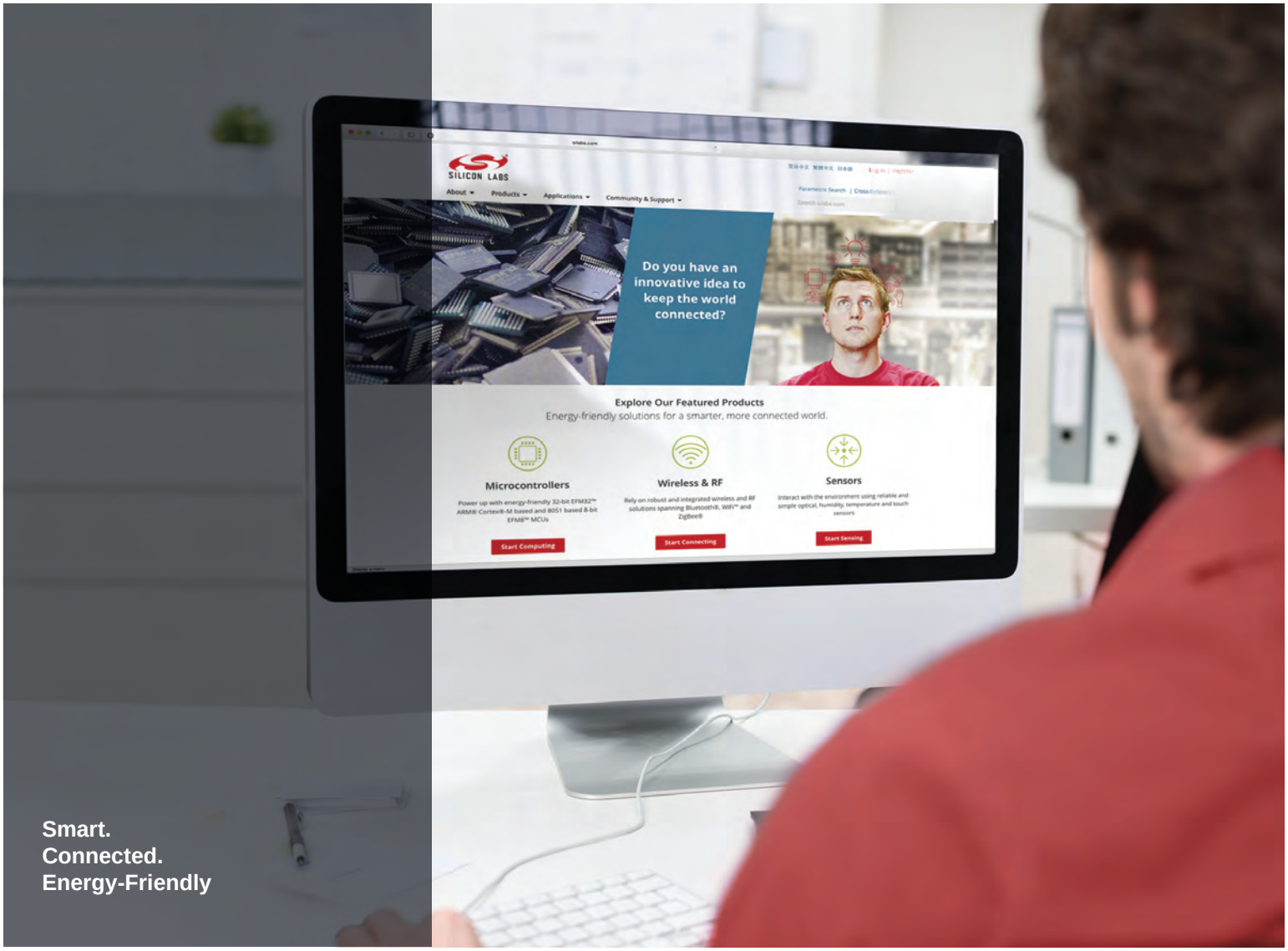
- Si47xx-Evaluation Board User's Guide
- AN309: Si4710/11/12/13 Evaluation Board Quick-Start Guide
- AN332: Universal Programming Guide
- AN383: Universal Antenna Selection and Layout Guidelines
- AN388: Universal Evaluation Board Test Procedure
- Si4710/11/12/13 Customer Support Site: http://www.mysilabs.com
  This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, send mysilabs user name and request for access to fminfo@silabs.com.

## NOTES:

# DOCUMENT CHANGE LIST

## Revision 0.5 to Revision 1.1

- Updated Table 9 on pages 12 and 13
- Corrected typo in Section 5.3.2 on page 21.
- Updated references to new application notes throughout document.
- Updated Table 3 on page 5.
- Updated production test condition in Table 9 on page 12.

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