



**ULTRA-LOW JITTER DUAL 2 × 2  
CROSSPOINT SWITCH w/ CML OUTPUTS  
AND INTERNAL I/O TERMINATION**

**Precision Edge®  
SY58024U**

## FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - >10.7Gbps data throughput
  - <60ps  $t_r/t_f$  times
  - <350ps  $t_{pd}$  (IN-to-Q)
  - <20ps skew
- **Low jitter:**
  - <10ps<sub>pp</sub> total jitter (clock)
  - <1ps<sub>RMS</sub> random jitter (data)
  - <10ps<sub>pp</sub> deterministic jitter (data)
- **Crosstalk induced jitter: <0.7ps<sub>RMS</sub>**
- **Unique, patent-pending input isolation minimizes adjacent channel crosstalk**
- **Accepts an input signal as low as 100mV**
- **Unique, patent-pending input termination and VT pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML**
- **Fully differential inputs/outputs**
- **50Ω source terminated CML outputs**
- **Power supply 2.5V ±5% and 3.3V ±10%**
- **Industrial –40°C to +85°C temperature range**
- **Available in 32-pin (5mm × 5mm) MLF® package**

## APPLICATIONS

- Gigabit Ethernet data/clock routing
- SONET data/clocking routing
- Switch fabric clock routing
- Redundant switchover
- Backplane redundancy



Precision Edge®

## DESCRIPTION

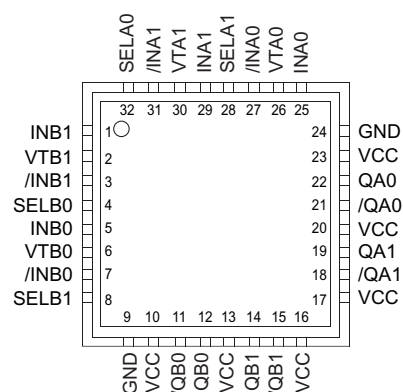
The SY58024U is a 2.5V/3.3V precision, high-speed, fully differential dual CML crosspoint switch. The SY58024U is optimized to provide two identical output copies with less than 20ps of skew and ultra-low jitter. The SY58024U can process clock signals as fast as 6GHz or data patterns up to 10.7Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the SY58024U to directly interface to LVPECL, LVDS, and CML differential signal (AC- or DC-coupled) without any level-shifting or termination resistor networks in the signal path. The CML outputs features a 400mV typical swing into 50Ω loads, and provides an extremely fast rise/fall time guaranteed to be less than 60ps.

The SY58024U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require high-speed single channel CML switches, consider the SY58023U. The SY58024U is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's website at: [www.micrel.com](http://www.micrel.com).

## PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information<sup>(1)</sup>

| Part Number                    | Package Type | Operating Range | Package Marking                          | Lead Finish    |
|--------------------------------|--------------|-----------------|------------------------------------------|----------------|
| SY58024UMI                     | MLF-32       | Industrial      | SY58024U                                 | Sn-Pb          |
| SY58024UMITR <sup>(2)</sup>    | MLF-32       | Industrial      | SY58024U                                 | Sn-Pb          |
| SY58024UMG <sup>(3)</sup>      | MLF-32       | Industrial      | SY58024U with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY58024UMGTR <sup>(2, 3)</sup> | MLF-32       | Industrial      | SY58024U with Pb-Free bar-line indicator | Pb-Free NiPdAu |

## Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

## PIN DESCRIPTION

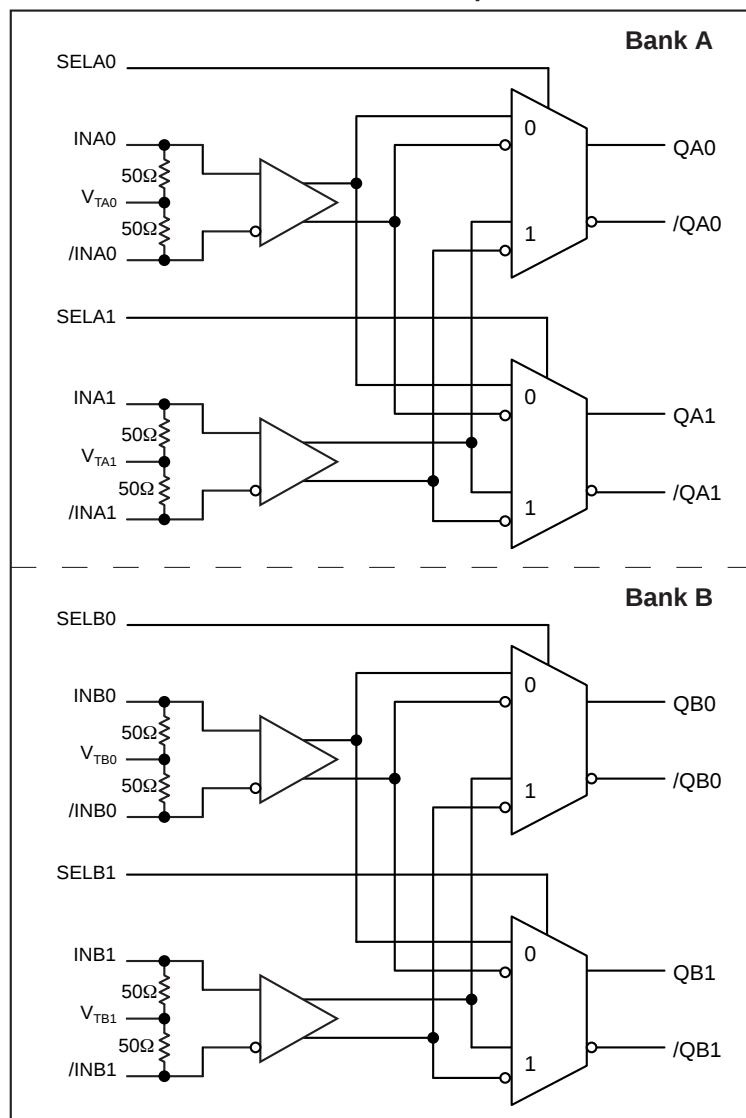
| Pin Number                             | Pin Name                                                   | Pin Function                                                                                                                                                                                                                                                                                                 |
|----------------------------------------|------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25, 27<br>29, 31,<br>1, 3,<br>5, 7     | INA0, /INA0,<br>INA1, /INA1,<br>INB1, /INB1<br>INB0, /INB0 | Differential Signal: Each pin of this pair internally terminates with $50\Omega$ to the VT pin. The input will default to an indeterminate state if left open. See "Input Interface Application" section.                                                                                                    |
| 26, 30<br>2, 6                         | VTA0, VTA1,<br>VTB1, VTB0                                  | Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See "Input Interface Application" section.                                                                            |
| 32, 28,<br>8, 4                        | SELA0, SELA1,<br>SELB1, SELB0                              | Select Input: TTL/CMOS select input controls that selects inputs IN0, or IN1, for their respective banks A and B. Each input is internally connected to a $25k\Omega$ pull-up resistor and will default to a logic high state if left open.                                                                  |
| 9, 24                                  | GND,<br>Exposed Pad                                        | Ground. Exposed pad must be connected to a ground plane that is the same potential as the device ground pins.                                                                                                                                                                                                |
| 10, 13, 16,<br>17, 20, 23              | VCC                                                        | Positive Power Supply: Bypass with $0.1\mu\text{F}$   $0.01\mu\text{F}$ low ESR capacitors as close to the $V_{CC}$ pins as possible.                                                                                                                                                                        |
| 11, 12,<br>15, 14<br>18, 19,<br>21, 22 | /QB0, QB0,<br>/QB1, QB1,<br>/QA1, QA1,<br>/QA0, QA0        | CML Differential Output Pairs: Differential buffered output copy of the selected input signal. The CML single-ended output swing is typically 400mV into $50\Omega$ or $100\Omega$ across the pair. Unused output pairs may be left floating with no impact on jitter. See "CML Output Termination" section. |

## TRUTH TABLE

| SELA0 | SELA1 | QA0  | QA1  | SELB0 | SELB1 | QB0  | QB1  |
|-------|-------|------|------|-------|-------|------|------|
| 0     | 0     | INA0 | INA0 | 0     | 0     | INB0 | INB0 |
| 0     | 1     | INA0 | INA1 | 0     | 1     | INB1 | INB1 |
| 1     | 0     | INA1 | INA0 | 1     | 0     | INB1 | INB0 |
| 1     | 1     | INA1 | INA1 | 1     | 1     | INB1 | INB1 |

## FUNCTIONAL BLOCK DIAGRAM

SY58024U Dual 2 × 2 Crosspoint Switch



**Absolute Maximum Ratings<sup>(1)</sup>**

|                                       |                                    |
|---------------------------------------|------------------------------------|
| Supply Voltage ( $V_{CC}$ )           | –0.5V to +4.0V                     |
| Input Voltage ( $V_{IN}$ )            | –0.5V to $V_{CC}$                  |
| CML Output Voltage ( $V_{OUT}$ )      | $V_{CC} - 1.0V$ to $V_{CC} + 0.5V$ |
| Current ( $V_T$ )                     |                                    |
| Source or Sink Current on VT pin      | ±100mA                             |
| Input Current ( $V_T$ )               |                                    |
| Source or Sink Current on IN, /IN     | ±50mA                              |
| Lead Temperature (soldering, 20 sec.) | 260°C                              |
| Storage Temperature ( $T_S$ )         | –65°C to +150°C                    |

**Operating Ratings<sup>(2)</sup>**

|                                           |                   |
|-------------------------------------------|-------------------|
| Supply Voltage ( $V_{CC}$ )               | +2.375V to +3.60V |
| Ambient Temperature ( $T_A$ )             | –40°C to +85°C    |
| Package Thermal Resistance <sup>(3)</sup> |                   |
| MLF® ( $\theta_{JA}$ )                    |                   |
| Still-Air                                 | 35°C/W            |
| 500lfpm                                   | 28°C/W            |
| MLF® ( $\psi_{JB}$ )                      |                   |
| Junction-to-board resistance              | 20°C/W            |

**DC ELECTRICAL CHARACTERISTICS<sup>(4)</sup>** $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

| Symbol         | Parameter                | Condition                                                                                      | Min            | Typ        | Max            | Units |
|----------------|--------------------------|------------------------------------------------------------------------------------------------|----------------|------------|----------------|-------|
| $V_{CC}$       | Power Supply Voltage     | 2.5V nominal<br>3.3V nominal                                                                   | 2.375<br>3.0   | 2.5<br>3.3 | 2.625<br>3.60  | V     |
| $I_{CC}$       | Power Supply Current     | $V_{CC} = \text{max.}$ , current through internal<br>50Ω source termination resistor included. |                | 200        | 250            | mA    |
| $V_{IH}$       | Input HIGH Voltage       | IN, /IN, Note 5                                                                                | $V_{CC} - 1.6$ |            | $V_{CC}$       | V     |
| $V_{IL}$       | Input LOW Voltage        | IN, /IN                                                                                        | 0              |            | $V_{IH} - 0.1$ | V     |
| $V_{IN}$       | Input Voltage Swing      | IN, /IN, see Figure 1a.                                                                        | 0.1            |            | 1.7            | V     |
| $V_{DIFF\_IN}$ | Differential Input Swing | IN, /IN, see Figure 1b.                                                                        | 0.2            |            |                | V     |
| $R_{IN}$       | IN-to- $V_T$ Resistance  |                                                                                                | 40             | 50         | 60             | Ω     |
| IN to $V_T$    |                          |                                                                                                |                |            | 1.28           | V     |

**LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS<sup>(4)</sup>** $V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ 

| Symbol   | Parameter          | Condition | Min  | Typ | Max | Units |
|----------|--------------------|-----------|------|-----|-----|-------|
| $V_{IH}$ | Input HIGH Voltage |           | 2.0  |     |     | V     |
| $V_{IL}$ | Input LOW Voltage  |           |      |     | 0.8 | V     |
| $I_{IH}$ | Input HIGH Current |           |      |     | 40  | μA    |
| $I_{IL}$ | Input LOW Current  |           | –300 |     |     | μA    |

**Notes:**

1. Permanent device damage may occur if ratings in the "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB.  $\theta_{JA}$  uses 4-layer in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5.  $V_{IH}$  (min) not lower than 1.2V.

**CML OUTPUT DC ELECTRICAL CHARACTERISTICS<sup>(6)</sup>**

$V_{CC} = +3.3V \pm 10\%$  or  $+2.5V \pm 5\%$ ;  $R_L = 100\Omega$  across each pair;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

| Symbol          | Parameter                  | Condition                        | Min              | Typ | Max      | Units    |
|-----------------|----------------------------|----------------------------------|------------------|-----|----------|----------|
| $V_{OH}$        | Output HIGH Voltage        | Q0, /Q0; Q1, /Q1                 | $V_{CC} - 0.020$ |     | $V_{CC}$ | V        |
| $V_{OUT}$       | Output Voltage Swing       | Q0, /Q0; Q1, /Q1; see Figure 1a. | 325              | 400 | 500      | mV       |
| $V_{DIFF\_OUT}$ | Differential Voltage Swing | Q0, /Q0; Q1, /Q1; see Figure 1b. | 650              | 800 | 1000     | mV       |
| $R_{OUT}$       | Output Source Impedance    | Q0, /Q0; Q1, /Q1                 | 40               | 50  | 60       | $\Omega$ |

**Notes:**

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**AC ELECTRICAL CHARACTERISTICS<sup>(7)</sup>**

$V_{CC} = +2.5V \pm 5\%$  or  $+3.3V \pm 10\%$ ;  $R_L = 100\Omega$  across each output pair;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

| Symbol       | Parameter                                 | Condition                                        | Min  | Typ | Max | Units             |
|--------------|-------------------------------------------|--------------------------------------------------|------|-----|-----|-------------------|
| $f_{MAX}$    | Maximum Operating Frequency               | $V_{IN} \geq 100mV$ ; $V_{OUT} \geq 200mV$ Clock | 6    |     |     | GHz               |
|              |                                           | NRZ Data                                         | 10.7 |     |     | Gbps              |
| $t_{pd}$     | Propagation Delay                         | IN-to-Q                                          | 200  |     | 350 | ps                |
|              |                                           | SEL-to-Q                                         | 100  |     | 400 | ps                |
| $t_{SKEW}$   | Channel-to-Channel Skew (Within Bank)     | <b>Note 8</b>                                    |      |     | 20  | ps                |
|              | Part-to-Part Skew                         | <b>Note 9</b>                                    |      |     | 75  | ps                |
| $t_{JITTER}$ | Clock Cycle-to-Cycle Jitter               | <b>Note 10</b>                                   |      |     | 1   | ps <sub>RMS</sub> |
|              |                                           | Total Jitter                                     |      |     | 10  | ps <sub>pp</sub>  |
|              | Data Random Jitter                        | <b>Note 12</b>                                   |      |     | 1   | ps <sub>RMS</sub> |
|              |                                           | Deterministic Jitter                             |      |     | 10  | ps <sub>pp</sub>  |
|              | Crosstalk Induced Jitter Adjacent Channel | <b>Note 14</b>                                   |      |     | 0.7 | ps <sub>RMS</sub> |
| $t_r, t_f$   | Output Rise/Fall Time                     | 20% to 80% at full swing.                        | 25   |     | 60  | ps                |

**Notes:**

- High frequency AC-parameters are guaranteed by design and characterization.
- Skew is measured between outputs of the same bank under identical transitions.
- Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
- Total jitter definition: With an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.
- Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps–3.2Gbps.
- Deterministic jitter is measured at 2.5Gbps–3.2Gbps with both K28.5 and  $2^{23}-1$  PRBS pattern.
- Crosstalk induced jitter is defined as the added jitter that results from signals applied to two adjacent channels. It is measured at the output while applying similar, differential clock frequencies that are asynchronous with respect to each other at inputs.

## SINGLE-ENDED AND DIFFERENTIAL SWINGS

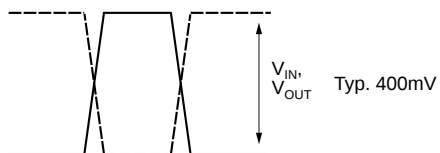


Figure 1a. Single-Ended Voltage Swing

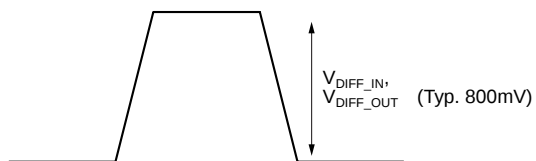


Figure 1b. Differential Voltage Swing

## TIMING DIAGRAM

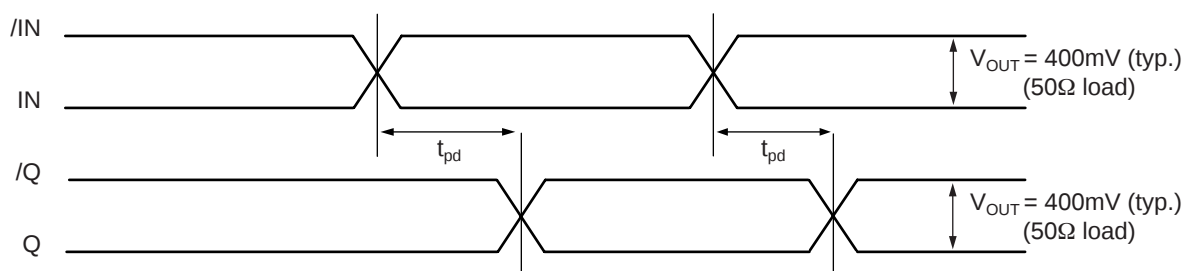


Figure 2a. AC Timing Diagram IN-to-Q

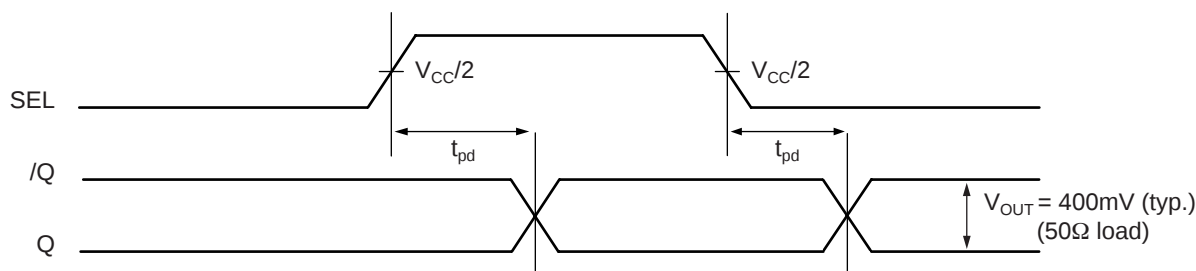
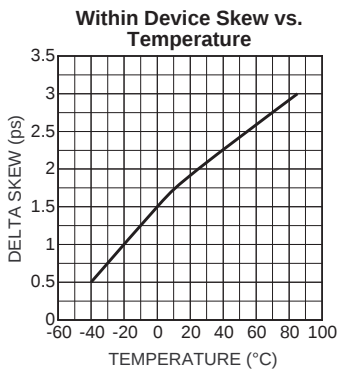
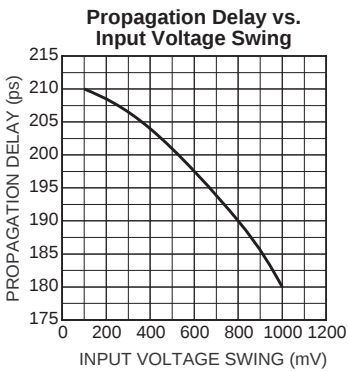
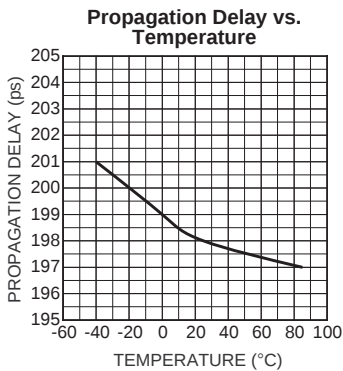
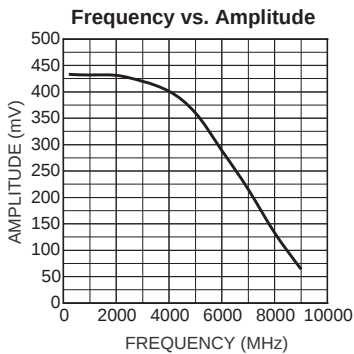
IN0,  $\overline{IN}1$  = LOW,  $\overline{IN}0$ , IN1 = HIGH

Figure 2b. AC Timing Diagram SEL-to-Q

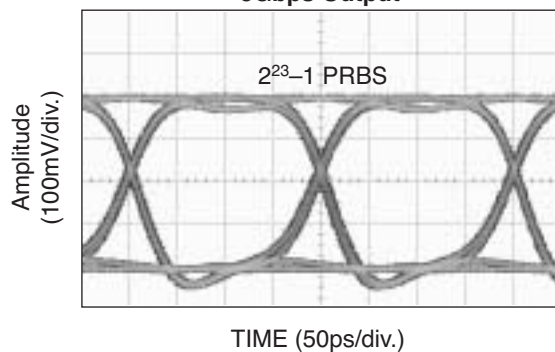
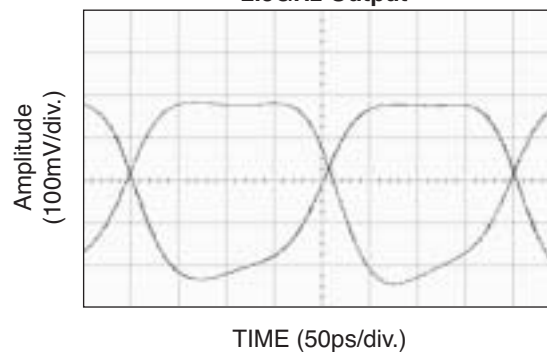
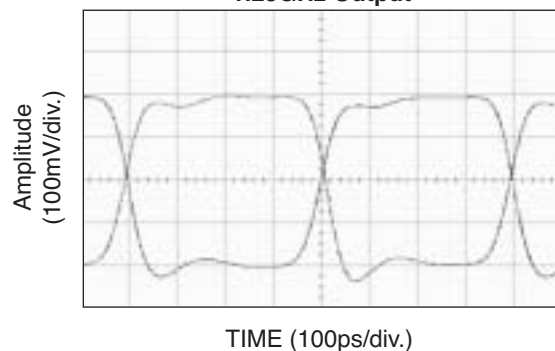
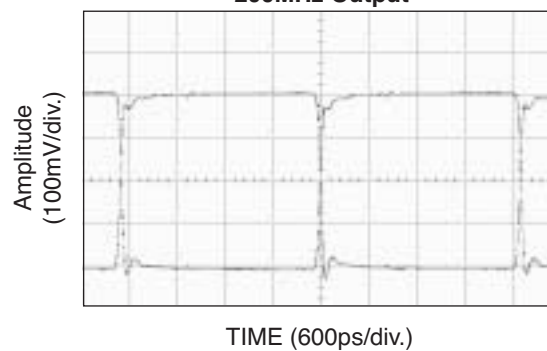
TYPICAL OPERATING CHARACTERISTICS

V<sub>CC</sub> = 2.5V, V<sub>IN</sub> = 100mV, T<sub>A</sub> = 25°C, unless otherwise noted.



**FUNCTIONAL CHARACTERISTICS**

$V_{CC} = 2.5V$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**5Gbps Output****2.5GHz Output****1.25GHz Output****200MHz Output**

## INPUT STAGE

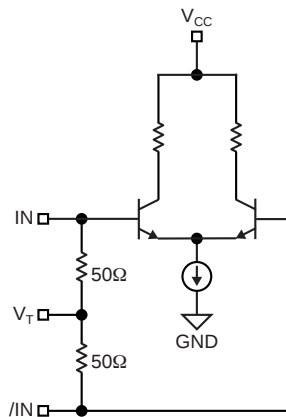
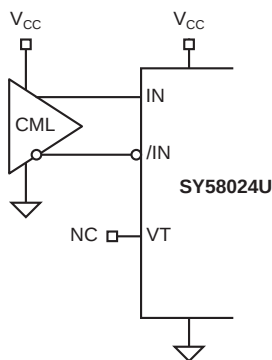
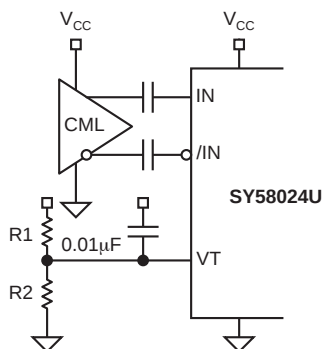
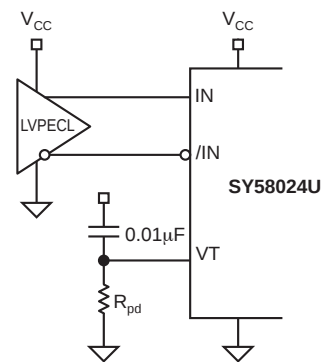
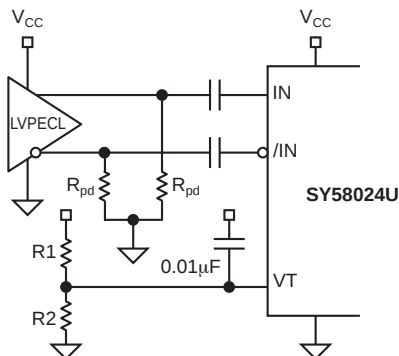
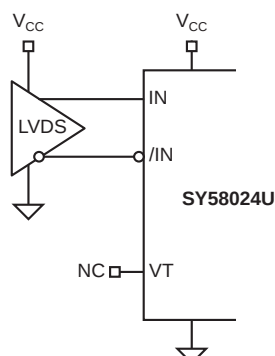


Figure 3. Simplified Differential Input Buffer

## INPUT INTERFACE APPLICATIONS

Figure 4a. DC-Coupled CML  
Input InterfaceOption: may connect  $V_T$  to  $V_{CC}$ For 2.5V,  $R_1 = 1\text{k}\Omega$ ,  $R_2 = 1.1\text{k}\Omega$ .  
For 3.3V,  $R_1 = 649\Omega$ ,  $R_2 = 1\text{k}\Omega$ .Figure 4b. AC-Coupled CML  
Input InterfaceFor 2.5V,  $R_{pd} = 19\Omega$ .  
For 3.3V,  $R_{pd} = 50\Omega$ .Figure 4c. DC-Coupled LVPECL  
Input InterfaceFor 2.5V,  $R_{pd} = 50\Omega$ ,  $R_1 = 1\text{k}\Omega$ ,  $R_2 = 1.1\text{k}\Omega$ .  
For 3.3V,  $R_{pd} = 100\Omega$ ,  $R_1 = 649\Omega$ ,  $R_2 = 1\text{k}\Omega$ .Figure 4d. AC-Coupled LVPECL  
Input InterfaceFigure 4e. LVDS  
Input Interface

CML OUTPUT TERMINATION

Figures 5 and Figure 6 illustrates how to terminate a CML output using both the AC-coupled and DC-coupled configuration. All outputs of the SY58024U are 50Ω with a 16mA current source.

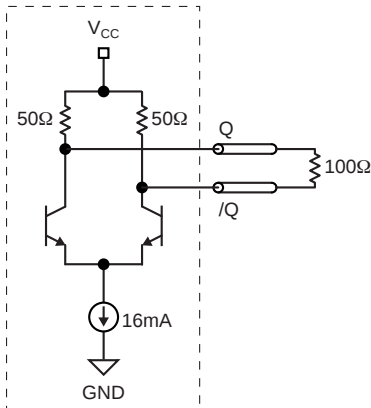


Figure 5. CML  
DC-Coupled Termination

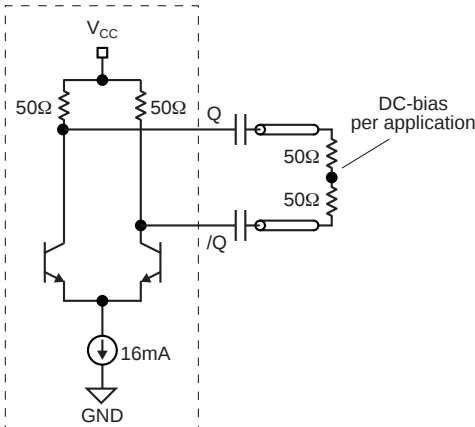


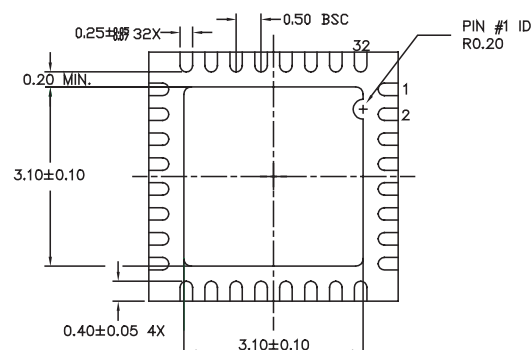
Figure 6. CML  
AC-Coupled Termination

RELATED PRODUCT AND SUPPORT DOCUMENTATION

| Part Number | Function                                                                               | Data Sheet Link                                                                                                                     |
|-------------|----------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| SY58023U    | Ultra-low Jitter 2x2 Crosspoint Switch w/CML Outputs and Internal I/O Termination      | <a href="http://www.micrel.com/product-info/products/SY58023U.shtml">http://www.micrel.com/product-info/products/SY58023U.shtml</a> |
| SY58024U    | Ultra-low Jitter Dual 2x2 Crosspoint Switch w/CML Outputs and Internal I/O Termination | <a href="http://www.micrel.com/product-info/products/sy58024u.shtml">http://www.micrel.com/product-info/products/sy58024u.shtml</a> |
|             | 32-MLF Manufacturing Guidelines Exposed Pad Application Note                           | <a href="http://www.amkor.com/products/notes_papers/MLF_AppNote.pdf">www.amkor.com/products/notes_papers/MLF_AppNote.pdf</a>        |
|             | HBW Solutions                                                                          | <a href="http://www.micrel.com/product-info/as/solutions.shtml">http://www.micrel.com/product-info/as/solutions.shtml</a>           |

Top view of a square component. The overall width is 5.0 BSC and the overall height is 5.0 BSC. A horizontal dashed line and a vertical dashed line intersect at the center. The width is divided into two equal sections of 32. The height is divided into two equal sections of 32. Two pins are located on the left edge, labeled 1 and 2. Pin 1 is at the top-left corner, and Pin 2 is at the bottom-left corner. A dimension line indicates the distance from the left edge to the center of Pin 1 is 0.20 DIA. TYP. The text "PIN #1 ID" is written above the dimension line.

TOP VIEW

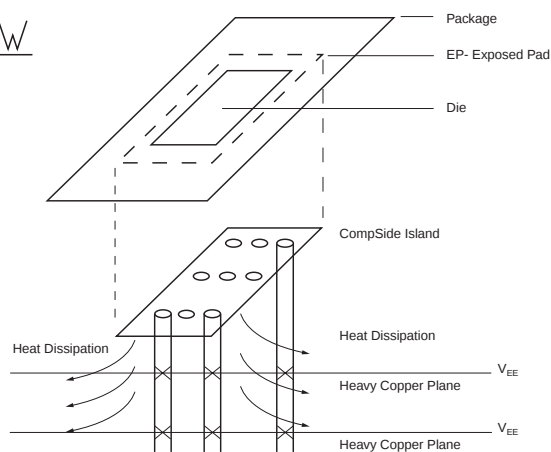


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/TNK MARKED.



**PCB Thermal Consideration for 32-Pin MLF® Package**  
(Always solder, or equivalent, the exposed pad to the PCB)

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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## Данный компонент на территории Российской Федерации

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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