



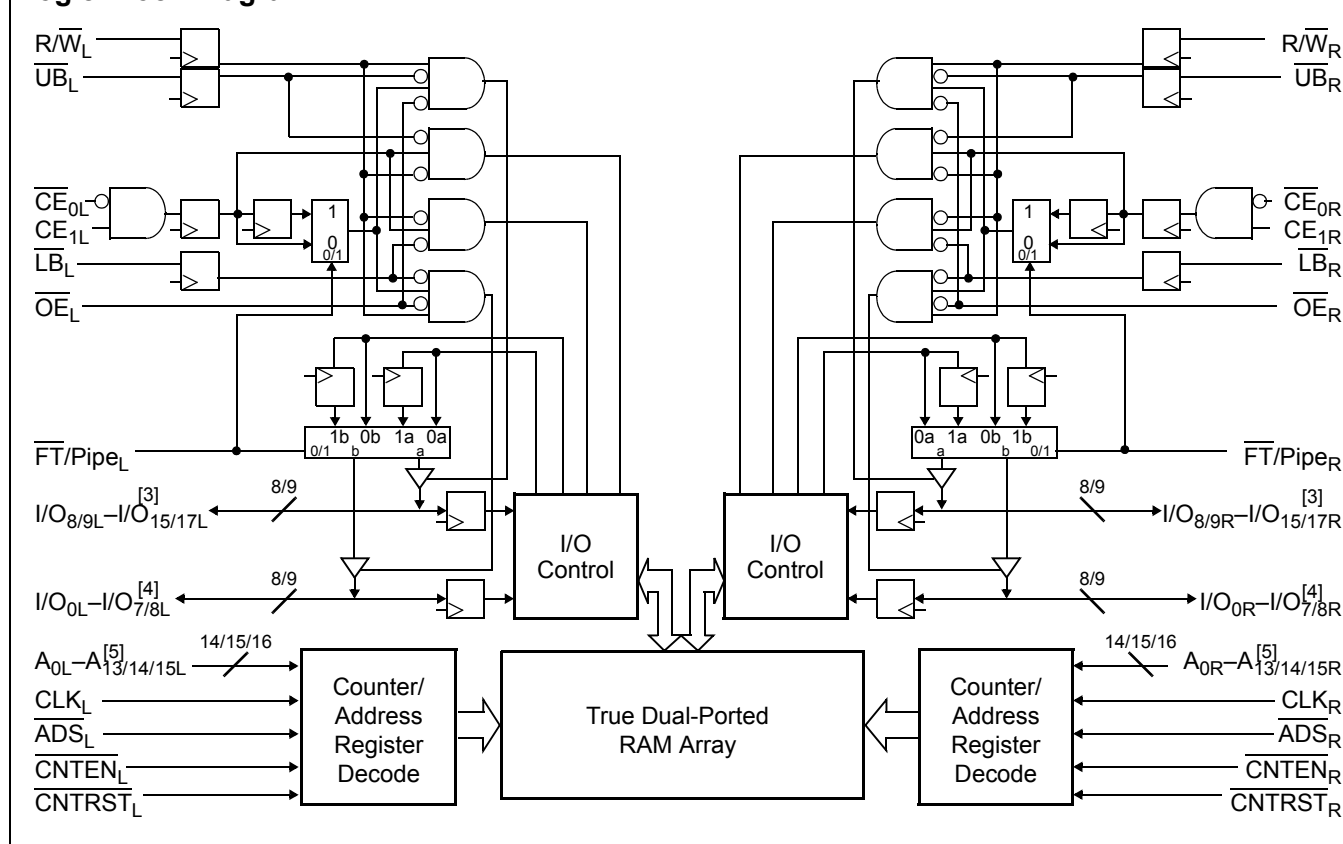
CY7C09269V/79V/89V
CY7C09369V/79V/89V

3.3V 16K/32K/64K x 16/18 Synchronous Dual-Port Static RAM

Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- 6 Flow-Through/Pipelined devices
 - 16K x 16/18 organization (CY7C09269V/369V)
 - 32K x 16/18 organization (CY7C09279V/379V)
 - 64K x 16/18 organization (CY7C09289V/389V)
- 3 Modes
 - Flow-Through
 - Pipelined
 - Burst
- Pipelined output mode on both ports allows fast 100-MHz operation
- 0.35-micron CMOS for optimum speed/power
- High-speed clock to data access 6.5^[1, 2]/7.5^[2]/9/12 ns (max.)
- 3.3V low operating power
 - Active = 115 mA (typical)
 - Standby = 10 μ A (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally
 - Shorten cycle times
 - Minimize bus noise
 - Supported in Flow-Through and Pipelined modes
- Dual Chip Enables for easy depth expansion
- Upper and Lower Byte Controls for Bus Matching
- Automatic power-down
- Commercial and Industrial temperature ranges
- Pb-Free 100-pin TQFP Package Available

Logic Block Diagram



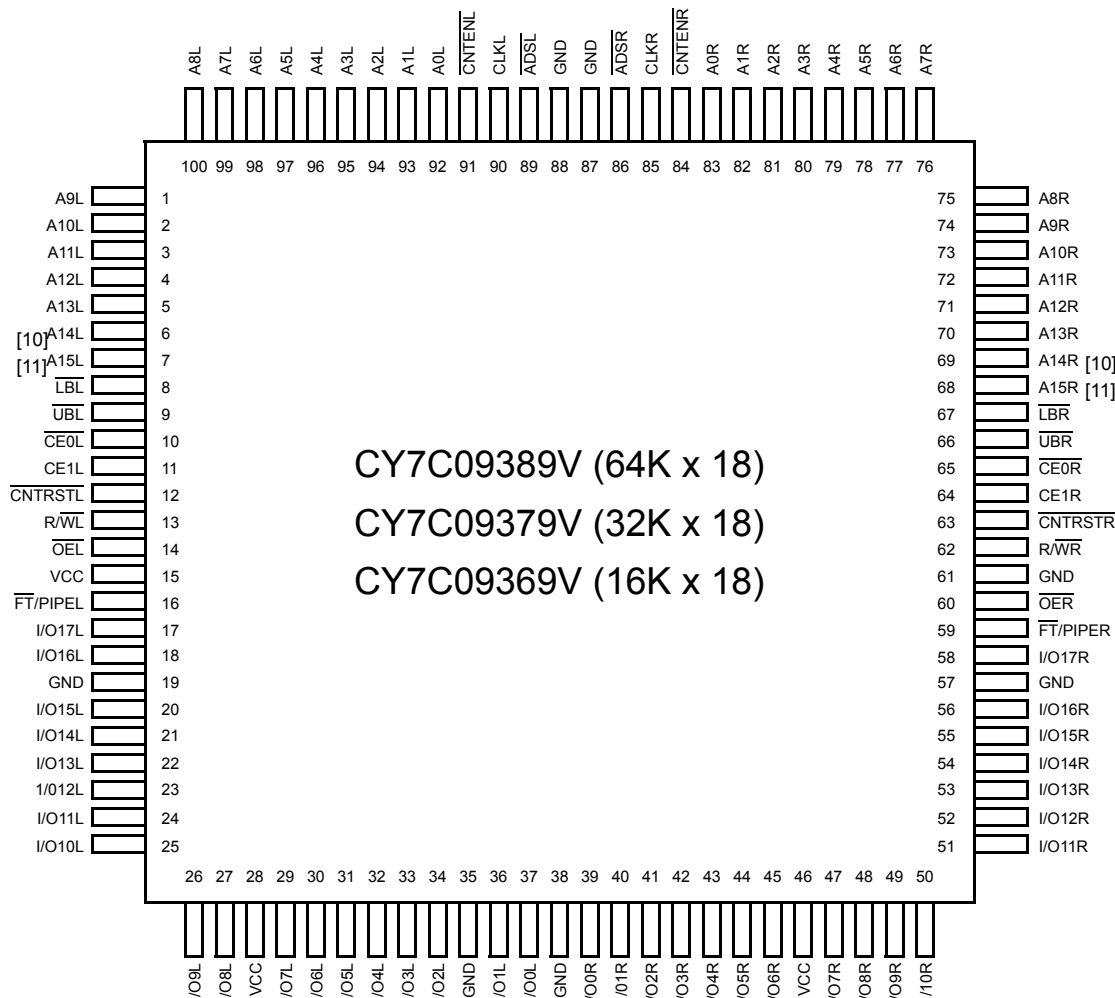
Notes:

1. Call for availability.
2. See page 6 for Load Conditions.
3. I/O₈-I/O₁₅ for x16 devices; I/O₉-I/O₁₇ for x18 devices.
4. I/O₀-I/O₇ for x16 devices; I/O₀-I/O₈ for x18 devices.
5. A₀-A₁₃ for 16K; A₀-A₁₄ for 32K; A₀-A₁₅ for 64K devices.



Pin Configurations (continued)

100-Pin TQFP (Top View)



Selection Guide

	CY7C09269V/79V/89V CY7C09369V/79V/89V -6^[1, 2]	CY7C09269V/79V/89V CY7C09369V/79V/89V -7^[2]	CY7C09269V/79V/89V CY7C09369V/79V/89V -9	CY7C09269V/79V/89V CY7C09369V/79V/89V -12
f _{MAX2} (MHz) (Pipelined)	100	83	67	50
Max. Access Time (ns) (Clock to Data, Pipelined)	6.5	7.5	9	12
Typical Operating Current I _{CC} (mA)	175	155	135	115
Typical Standby Current for I _{SB1} (mA) (Both Ports TTL Level)	25	25	20	20
Typical Standby Current for I _{SB3} (μA) (Both Ports CMOS Level)	10 μA	10 μA	10 μA	10 μA

Notes:

10. This pin is NC for CY7C09369V.

11. This pin is NC for CY7C09369V and CY7C09379V.

Pin Definitions

Left Port	Right Port	Description
$A_{0L}-A_{15L}$	$A_{0R}-A_{15R}$	Address Inputs (A_0-A_{14} for 32K, A_0-A_{13} for 16K devices).
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Input. Used as an address qualifier. This signal should be asserted LOW to access the part using an externally supplied address. Asserting this signal LOW also loads the burst counter with the address present on the address pins.
$\overline{CE}_{0L}, CE_{1L}$	$\overline{CE}_{0R}, CE_{1R}$	Chip Enable Input. To select either the left or right port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).
CLK_L	CLK_R	Clock Signal. This input can be free running or strobed. Maximum clock input rate is f_{MAX} .
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable Input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. CNTEN is disabled if ADS or CNTRST are asserted LOW.
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset Input. Asserting this signal LOW resets the burst address counter of its respective port to zero. CNTRST is not disabled by asserting ADS or CNTEN.
$I/O_{0L}-I/O_{17L}$	$I/O_{0R}-I/O_{17R}$	Data Bus Input/Output ($I/O_0-I/O_{15}$ for x16 devices).
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select Input. Asserting this signal LOW enables read and write operations to the lower byte. ($I/O_0-I/O_8$ for x18, $I/O_0-I/O_7$ for x16) of the memory array. For read operations both the LB and OE signals must be asserted to drive output data on the lower byte of the data pins.
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select Input. Same function as $\overline{LB}$, but to the upper byte ($I/O_{8/9L}-I/O_{15/17L}$).
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable Input. This signal must be asserted LOW to enable the I/O data pins during read operations.
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable Input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipelined Select Input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH.
GND		Ground Input.
NC		No Connect.
V_{CC}		Power Input.

Maximum Ratings^[12]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with
Power Applied..... -55°C to $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential -0.5V to $+4.6\text{V}$

DC Voltage Applied to
Outputs in High Z State..... -0.5V to $V_{CC}+0.5\text{V}$

DC Input Voltage..... -0.5V to $V_{CC}+0.5\text{V}$

Note:

12. The voltage on any input or I/O pin can not exceed the power pin during power-up.

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... $>1100\text{V}$

Latch-Up Current..... $>200\text{mA}$

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$3.3\text{V} \pm 300\text{ mV}$
Industrial	-40°C to $+85^{\circ}\text{C}$	$3.3\text{V} \pm 300\text{ mV}$

Electrical Characteristics Over the Operating Range

Parameter	Description		CY7C09269V/79V/89V CY7C09369V/79V/89V												Unit	
			-6 ^[1, 2]			-7 ^[2]			-9			-12				
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V _{OH}	Output HIGH Voltage (V _{CC} = Min. I _{OH} = -4.0 mA)		2.4			2.4			2.4			2.4			V	
V _{OL}	Output LOW Voltage (V _{CC} = Min. I _{OH} = +4.0 mA)				0.4			0.4			0.4			0.4		V
V _{IH}	Input HIGH Voltage		2.0			2.0			2.0					2.0		V
V _{IL}	Input LOW Voltage				0.8			0.8			0.8			0.8		V
I _{OZ}	Output Leakage Current		-10		10	-10		10	-10		10	-10		10	-10	10
I _{CC}	Operating Current (V _{CC} = Max, I _{OUT} = 0 mA) Outputs Disabled			175	320		155	275		135	230		115	180	mA	
							275	390		185	300				mA	
I _{SB1}	Standby Current (Both Ports TTL Level) ^[13] CE _L & CE _R ≥ V _{IH} , f = f _{MAX}			25	95	25	85	20	75	20	70	mA				
						85	120	35	85			mA				
I _{SB2}	Standby Current (One Port TTL Level) ^[13] CE _L CE _R ≥ V _{IH} , f = f _{MAX}			115	175	105	165	95	155	85	140	mA				
						165	210	105	165			mA				
I _{SB3}	Standby Current (Both Ports CMOS Level) ^[13] CE _L & CE _R ≥ V _{CC} - 0.2V, f = 0			10	250	10	250	10	250	10	250	10	250	μA		
						10	250	10	250			μA				
I _{SB4}	Standby Current (One Port CMOS Level) ^[13] CE _L CE _R ≥ V _{IH} , f = f _{MAX}			105	135	95	125	85	115	75	100	mA				
						125	170	95	125			mA				

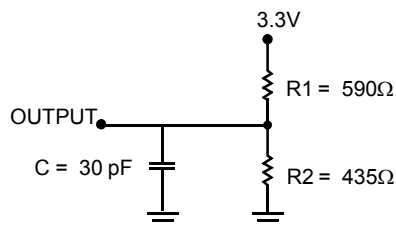
Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	10	pF
C _{OUT}	Output Capacitance		10	pF

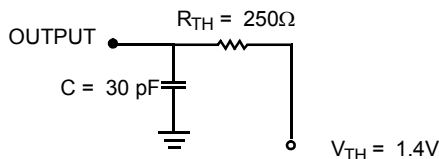
Note:

13. $\overline{CE}_L$ and $\overline{CE}_R$ are internal signals. To select either the left or right port, both $\overline{CE}_0$ and CE_1 must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).

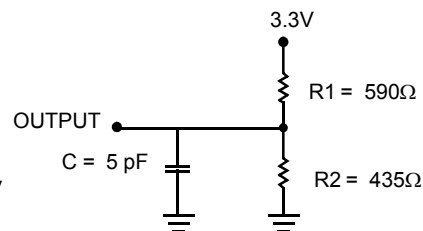
AC Test Loads



(a) Normal Load (Load 1)

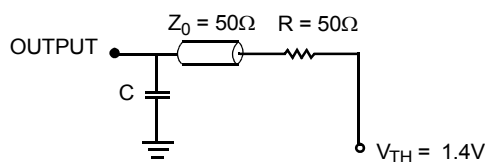


(b) Thévenin Equivalent (Load 1)

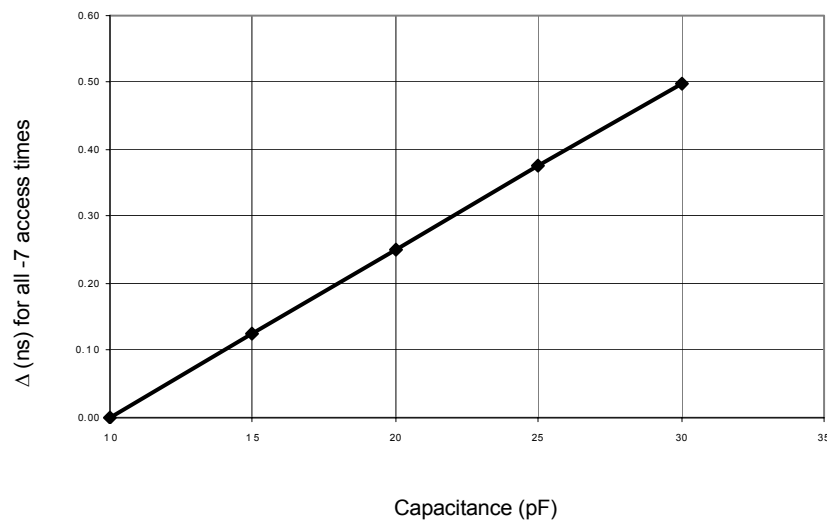
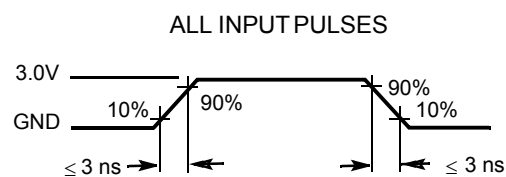


(c) Three-State Delay (Load 2)
(Used for t_{CKLZ} , t_{OLZ} , & t_{OHZ}
including scope and jig)

AC Test Loads (Applicable to -6 and -7 only)^[14]



(a) Load 1 (-6 and -7 only)



(b) Load Derating Curve

Note:

14. Test Conditions: C = 10 pF.

Switching Characteristics Over the Operating Range

Parameter	Description	CY7C09269V/79V/89V CY7C09369V/79V/89V								Unit
		-6 ^[1, 2]		-7 ^[2]		-9		-12		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX1}	f _{Max} Flow-Through		53		45		40		33	MHz
f _{MAX2}	f _{Max} Pipelined		100		83		67		50	MHz
t _{CYC1}	Clock Cycle Time - Flow-Through	19		22		25		30		ns
t _{CYC2}	Clock Cycle Time - Pipelined	10		12		15		20		ns
t _{CH1}	Clock HIGH Time - Flow-Through	6.5		7.5		12		12		ns
t _{CL1}	Clock LOW Time - Flow-Through	6.5		7.5		12		12		ns
t _{CH2}	Clock HIGH Time - Pipelined	4		5		6		8		ns
t _{CL2}	Clock LOW Time - Pipelined	4		5		6		8		ns
t _R	Clock Rise Time		3		3		3		3	ns
t _F	Clock Fall Time		3		3		3		3	ns
t _{SA}	Address Set-Up Time	3.5		4		4		4		ns
t _{HA}	Address Hold Time	0		0		1		1		ns
t _{SC}	Chip Enable Set-Up Time	3.5		4		4		4		ns
t _{HC}	Chip Enable Hold Time	0		0		1		1		ns
t _{SW}	R/ $\overline{W}$ Set-Up Time	3.5		4		4		4		ns
t _{HW}	R/ $\overline{W}$ Hold Time	0		0		1		1		ns
t _{SD}	Input Data Set-Up Time	3.5		4		4		4		ns
t _{HD}	Input Data Hold Time	0		0		1		1		ns
t _{SAD}	$\overline{ADS}$ Set-Up Time	3.5		4		4		4		ns
t _{HAD}	$\overline{ADS}$ Hold Time	0		0		1		1		ns
t _{SCN}	$\overline{CNTEN}$ Set-Up Time	3.5		4.5		5		5		ns
t _{HCN}	$\overline{CNTEN}$ Hold Time	0		0		1		1		ns
t _{SRST}	$\overline{CNTRST}$ Set-Up Time	3.5		4		4		4		ns
t _{HRST}	$\overline{CNTRST}$ Hold Time	0		0		1		1		ns
t _{OE}	Output Enable to Data Valid		8		9		10		12	ns
t _{OLZ} ^[15,16]	$\overline{OE}$ to Low Z	2		2		2		2		ns
t _{OHZ} ^[15,16]	$\overline{OE}$ to High Z	1	7	1	7	1	7	1	7	ns
t _{CD1}	Clock to Data Valid - Flow-Through		15		18		20		25	ns
t _{CD2}	Clock to Data Valid - Pipelined		6.5		7.5		9		12	ns
t _{DC}	Data Output Hold After Clock HIGH	2		2		2		2		ns
t _{CKZ} ^[15,16]	Clock HIGH to Output High Z	2	9	2	9	2	9	2	9	ns
t _{CKZ} ^[15,16]	Clock HIGH to Output Low Z	2		2		2		2		ns
Port to Port Delays										
t _{CWDD}	Write Port Clock HIGH to Read Data Delay		30		35		40		40	ns
t _{CCS}	Clock to Clock Set-Up Time		9		10		15		15	ns

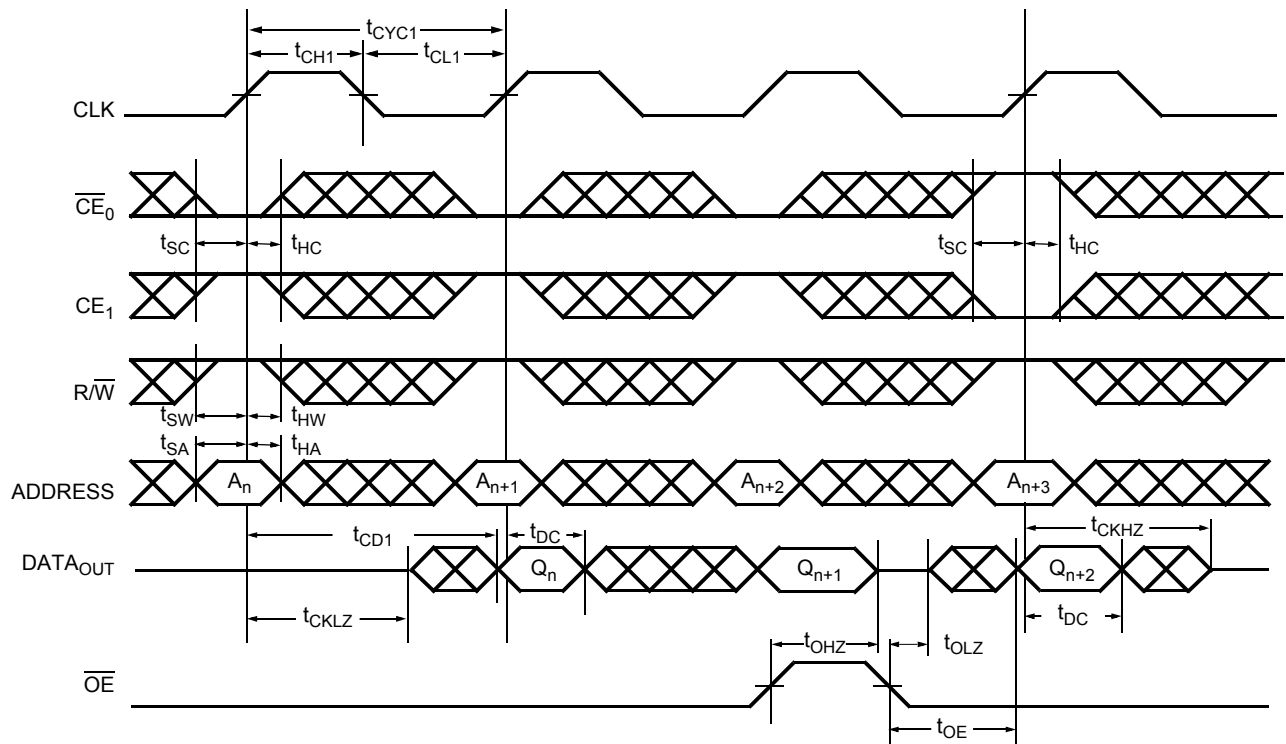
Notes:

15. Test conditions used are Load 2.

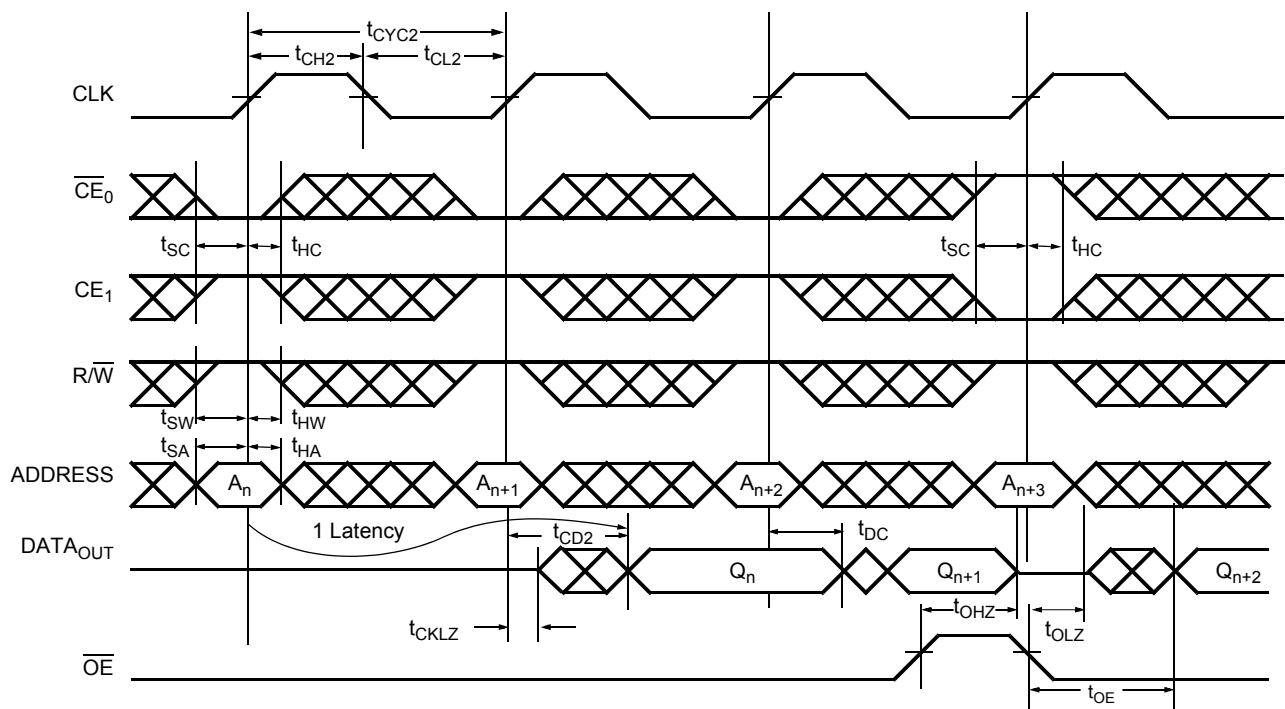
16. This parameter is guaranteed by design, but it is not production tested.

Switching Waveforms

Read Cycle for Flow-Through Output ($\overline{\text{FT}}/\text{PIPE} = V_{\text{IL}}$)^[17, 18, 19, 20]



Read Cycle for Pipelined Operation ($\overline{\text{FT}}/\text{PIPE} = V_{\text{IH}}$)^[17, 18, 19, 20]



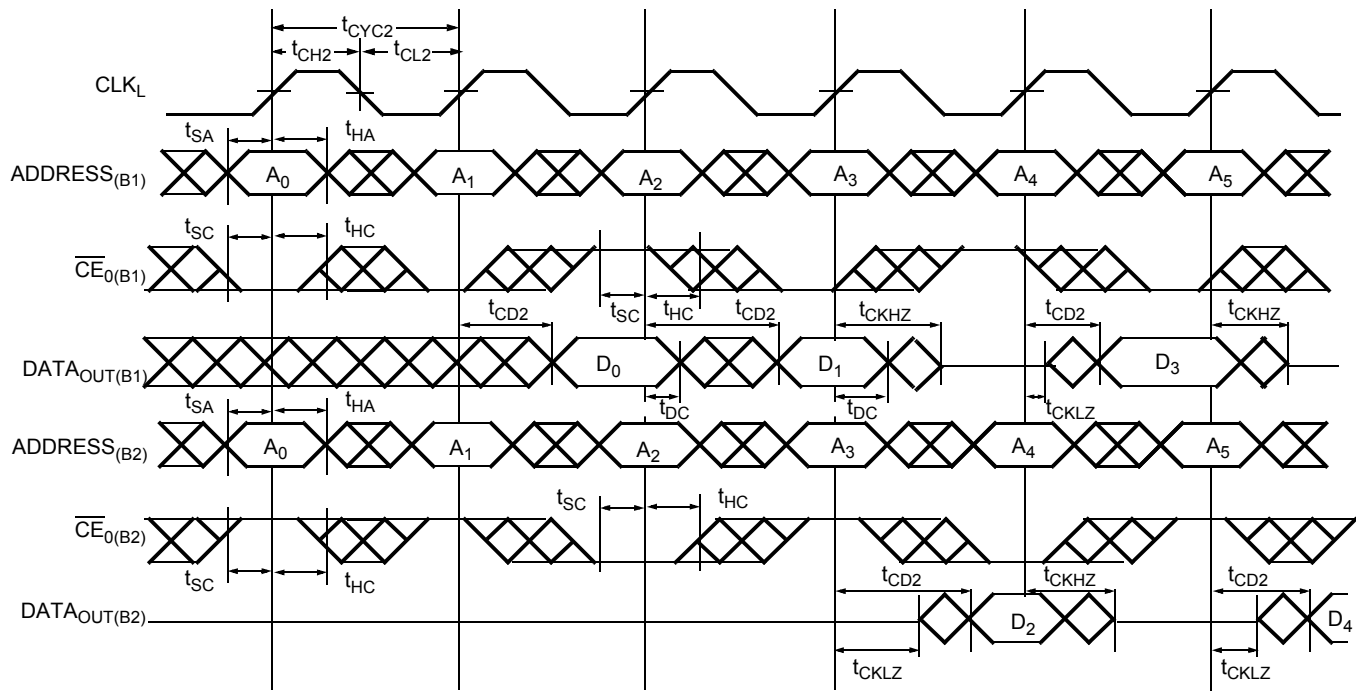
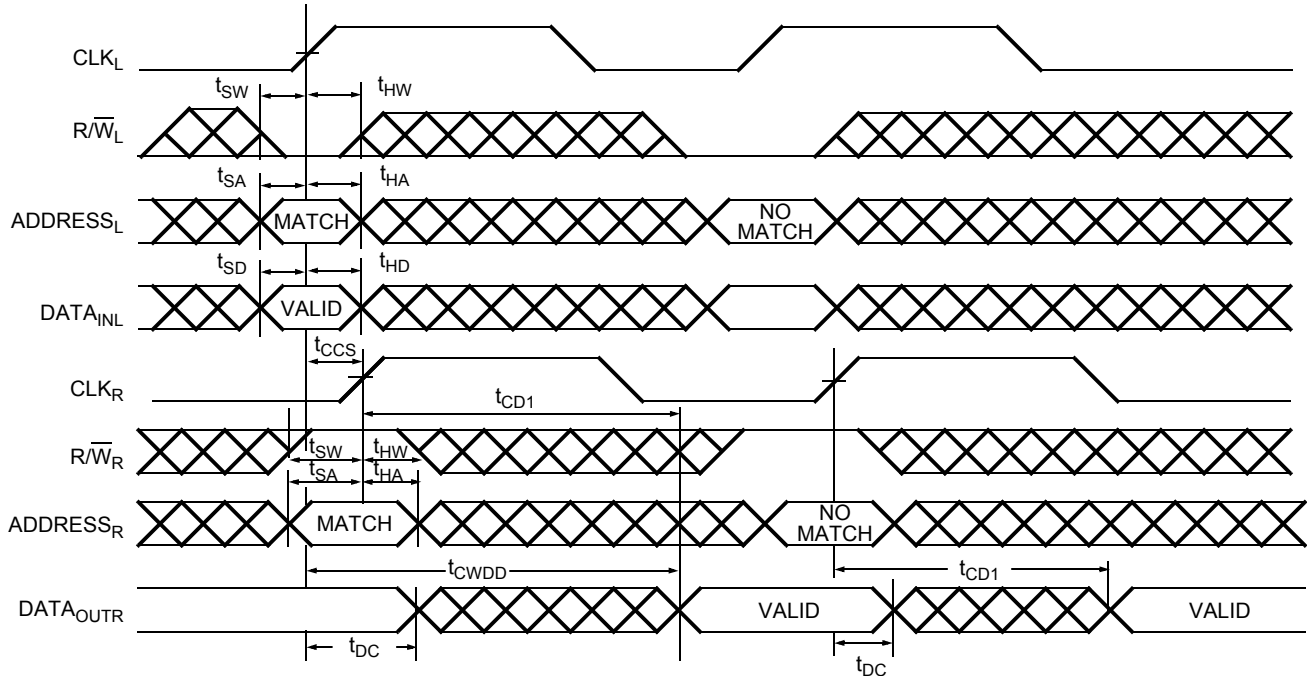
Notes:

17. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.

18. $\text{ADS} = V_{\text{IL}}$, CNTEN and $\text{CNTRST} = V_{\text{IH}}$.

19. The output is disabled (high-impedance state) by $\overline{\text{CE}}_0 = V_{\text{IH}}$ or $\text{CE}_1 = V_{\text{IL}}$ following the next rising edge of the clock.

20. Addresses do not have to be accessed sequentially since $\text{ADS} = V_{\text{IL}}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)
Bank Select Pipelined Read^[21, 22]

Left Port Write to Flow-Through Right Port Read^[23, 24, 25, 26]

Notes:

21. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this datasheet.

ADDRESS_(B1) = ADDRESS_(B2).

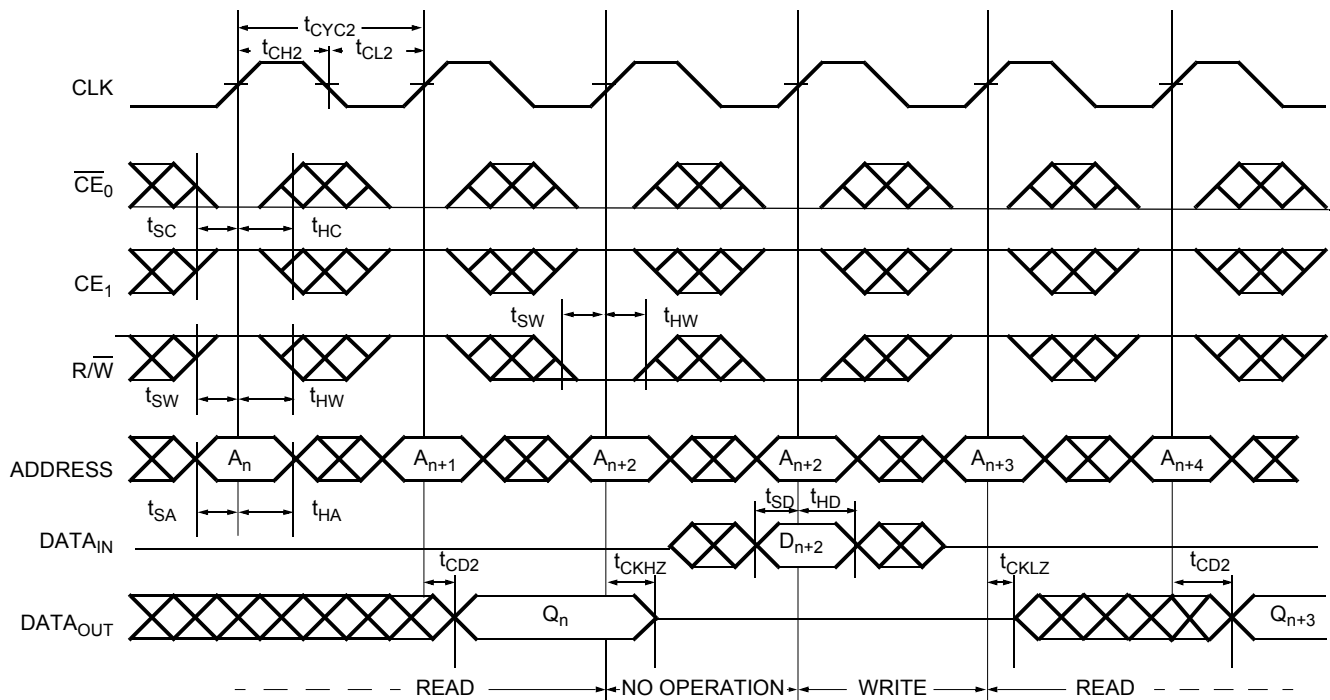
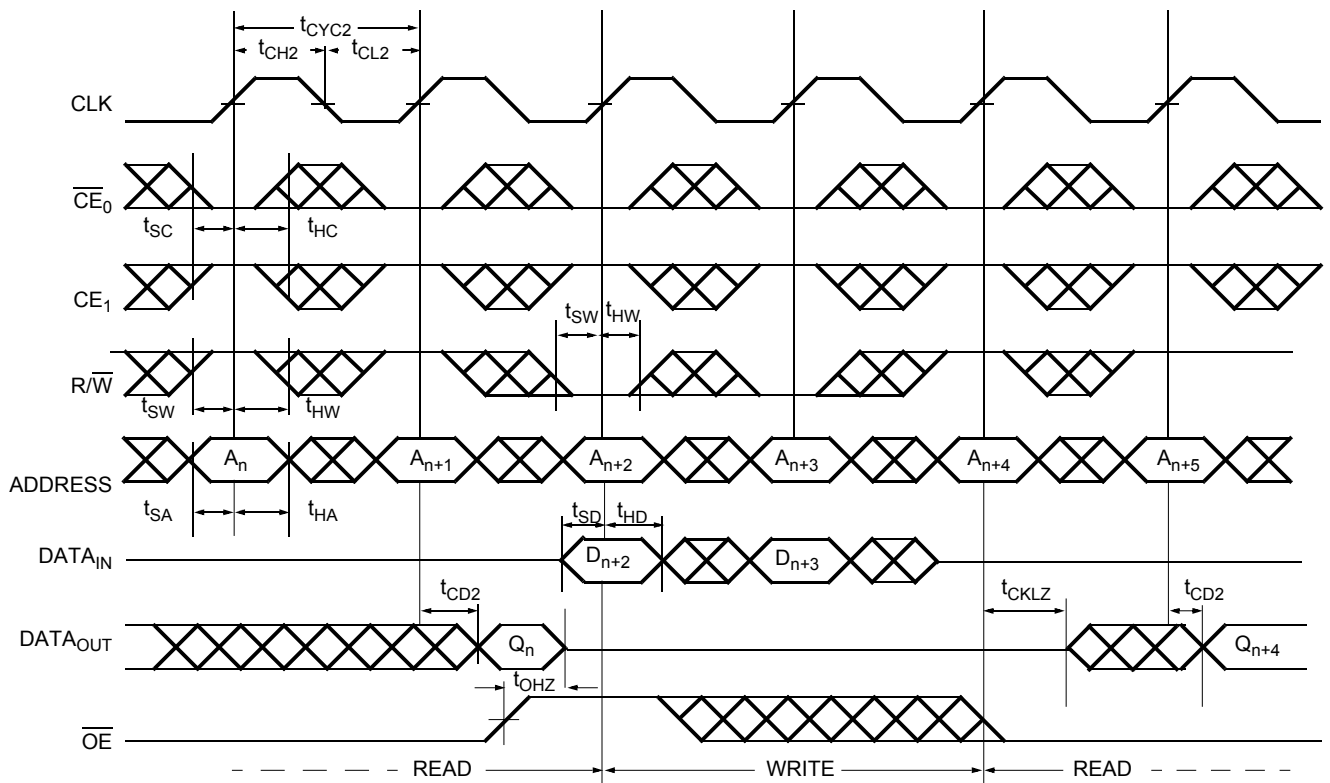
22. UB, LB, OE and ADS = V_{IL}; CE_{1(B1)}, CE_{1(B2)}, R/W, CNTEN, and CNTRST = V_{IH}.

23. The same waveforms apply for a right port write to flow-through left port read.

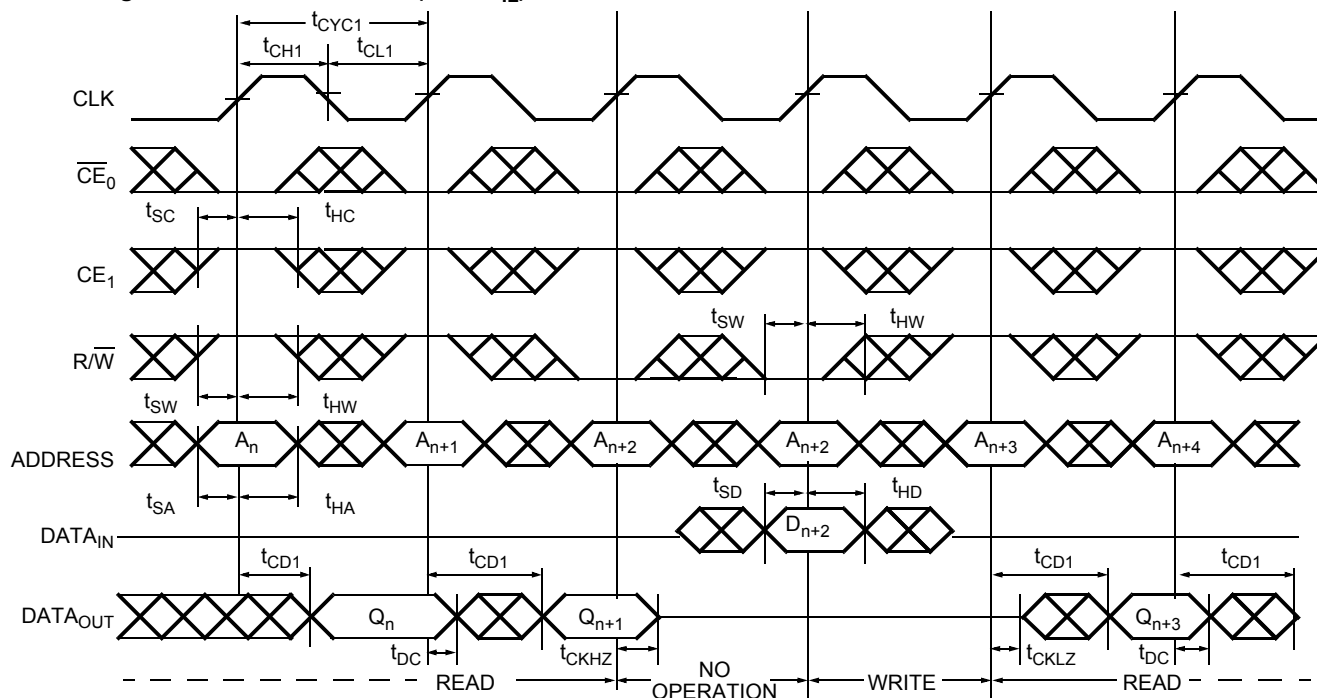
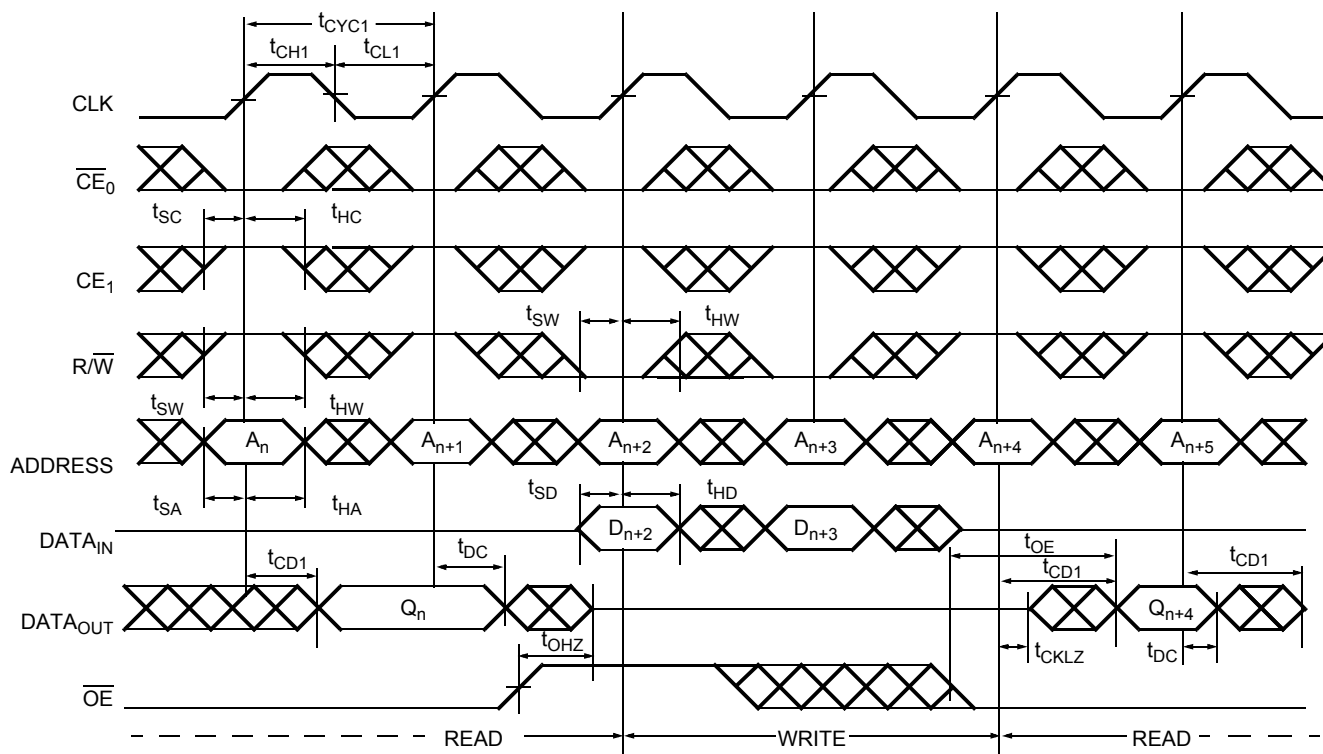
24. CE₀, UB, LB, and ADS = V_{IL}; CE₁, CNTEN, and CNTRST = V_{IH}.

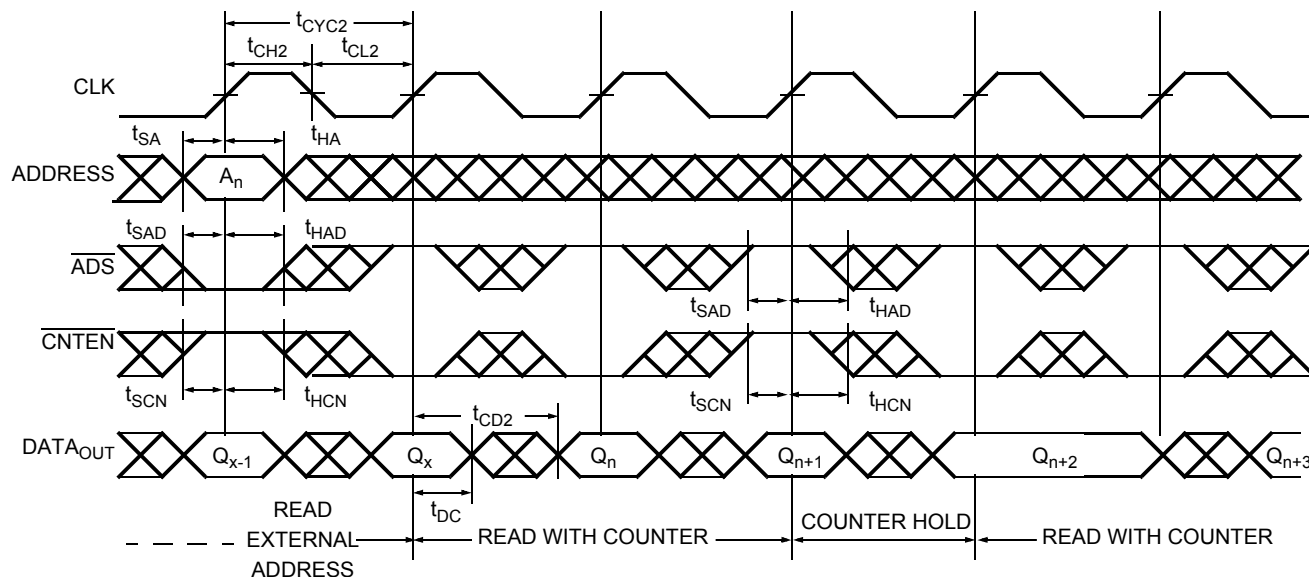
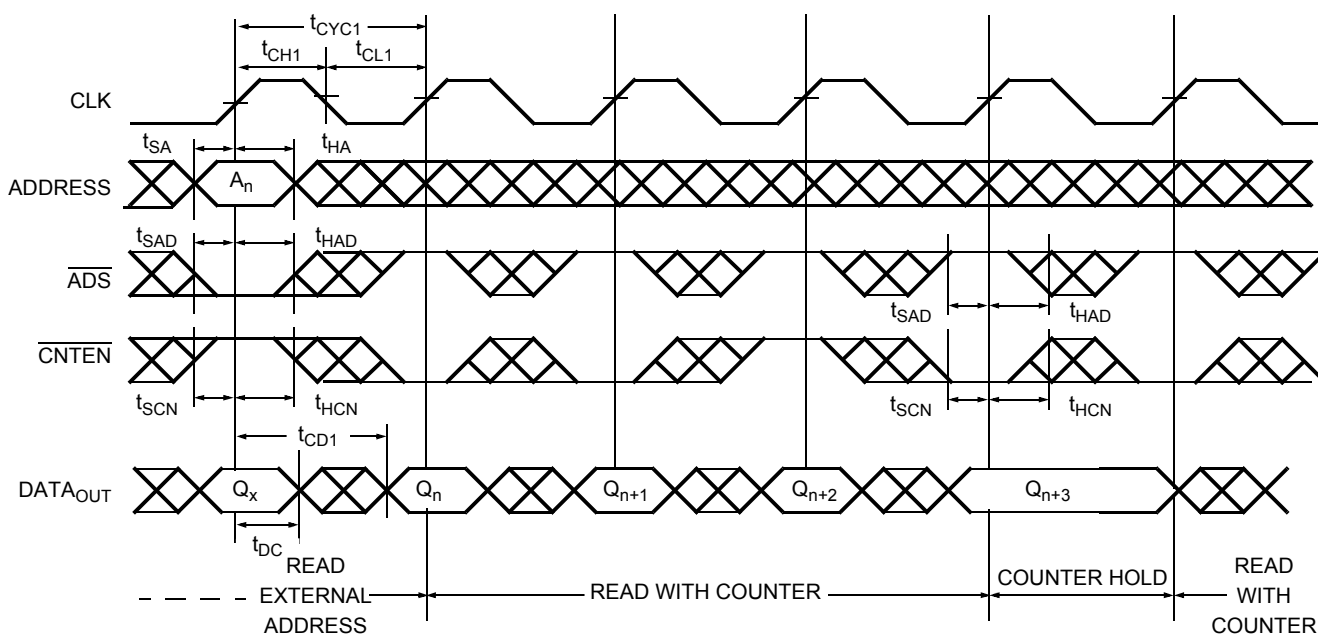
25. OE = V_{IL} for the Right Port, which is being read from. OE = V_{IH} for the Left Port, which is being written to.

26. If t_{CCS} ≤ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS} > maximum specified, then data is not valid until t_{CCS} + t_{CD1}. t_{CWDD} does not apply in this case.

Switching Waveforms (continued)
Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$) [20, 27, 28, 29]

Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled) [20, 27, 28, 29]

Notes:

27. Output state (High, LOW, or high impedance) is determined by the previous cycle control signals.
28. $\overline{CE}_0$ and $\overline{ADS} = V_{IL}$; CE_1 , $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
29. During "No Operation", data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

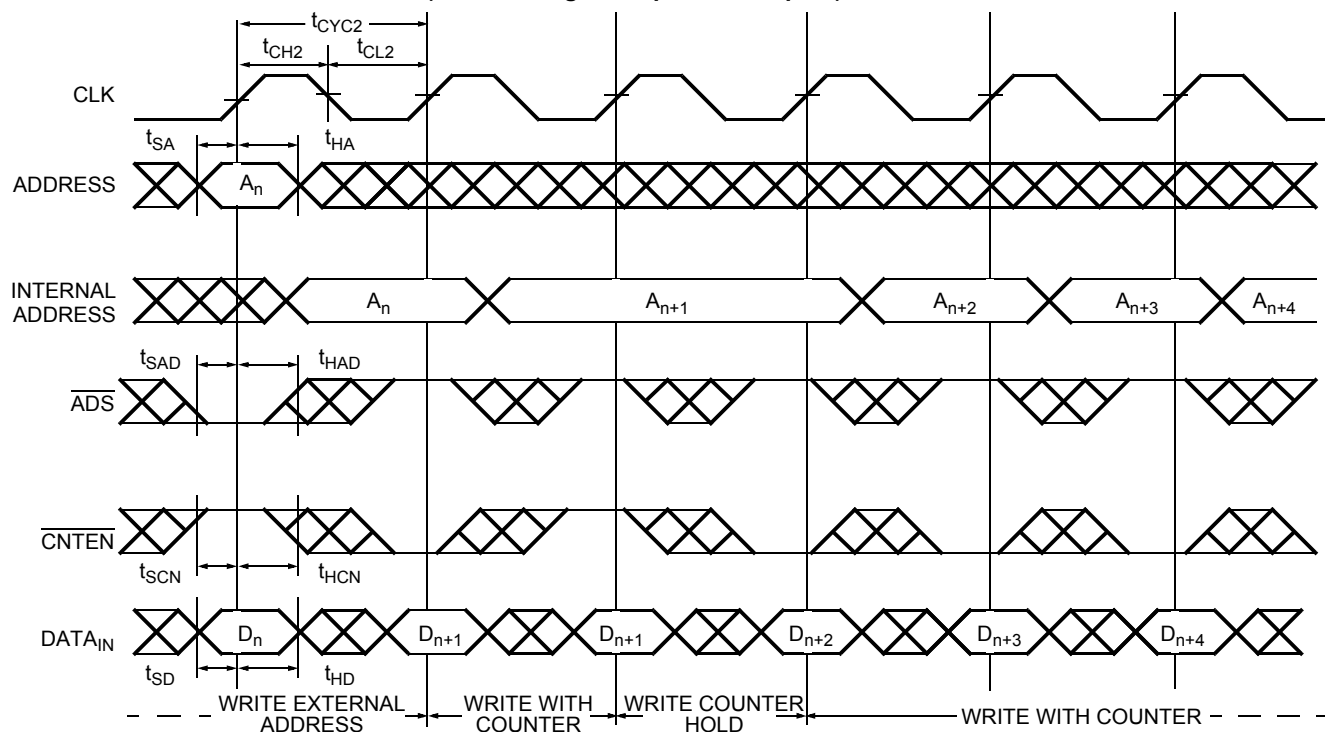
Switching Waveforms (continued)
Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)^[18, 20, 28, 29]

Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)^[18, 20, 27, 28, 29]


Switching Waveforms (continued)
Pipelined Read with Address Counter Advance^[30]

Flow-Through Read with Address Counter Advance^[30]

Note:

30. $\overline{CE_0}$ and $\overline{OE} = V_{IL}$; CE_1 , $R/\overline{W}$ and $\overline{CNTRST} = V_{IH}$.

Switching Waveforms (continued)

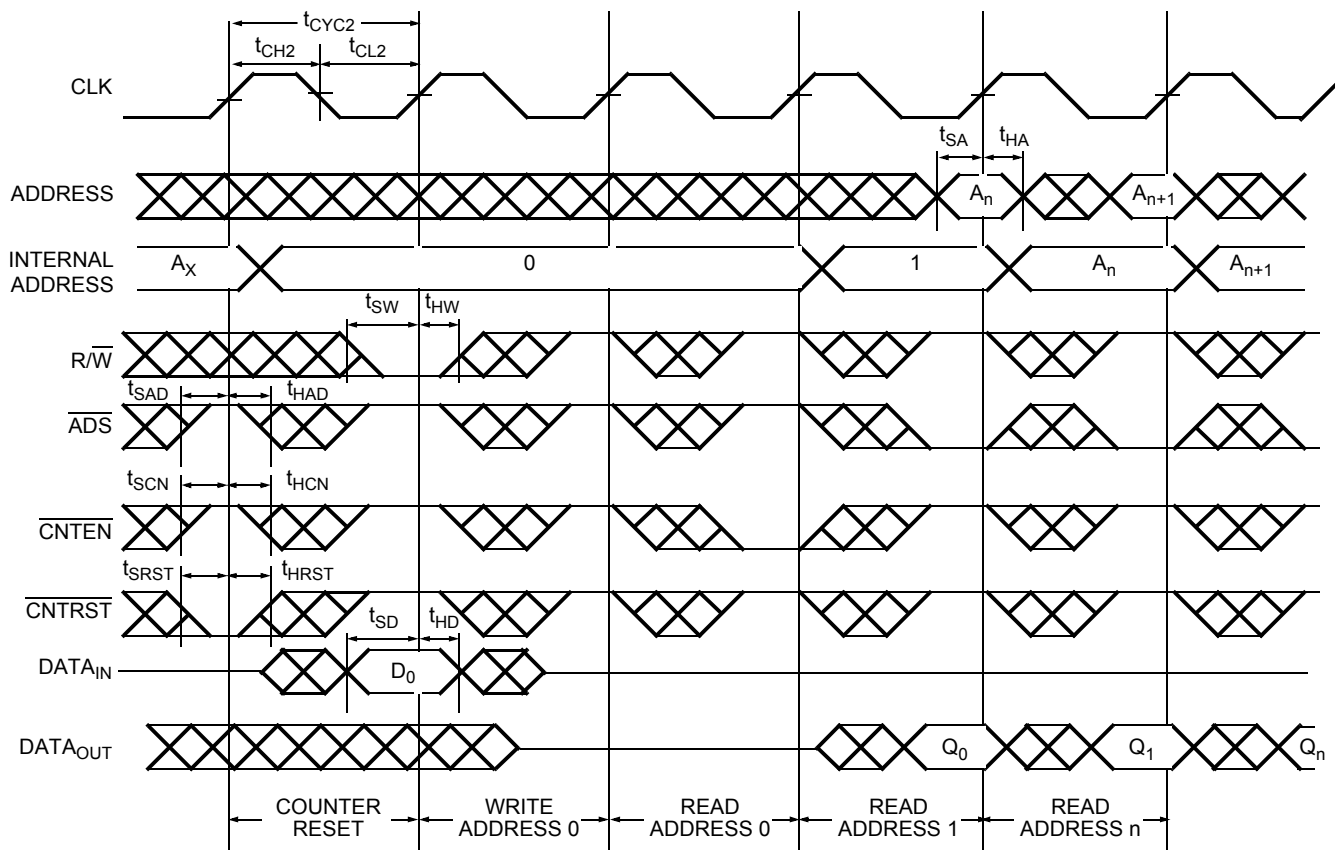
Write with Address Counter Advance (Flow-Through or Pipelined Outputs)^[31, 32]



Notes:

31. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{R/\overline{W}} = V_{IL}$; $\overline{CE_1}$ and $\overline{CNTRST} = V_{IH}$.

32. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.

Switching Waveforms (continued)
Counter Reset (Pipelined Outputs)^[20, 27, 33, 34]

Notes:

33. $\overline{CE_0}$, $\overline{UB}$, and $\overline{LB} = V_{IL}$; $CE_1 = V_{IH}$.

34. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

Read/Write and Enable Operation^[35, 36, 37]

Inputs					Outputs	Operation
OE	CLK	CE ₀	CE ₁	R/W	I/O ₀ –I/O ₁₇	
X		H	X	X	High-Z	Deselected ^[38]
X		X	L	X	High-Z	Deselected ^[38]
X		L	H	L	D _{IN}	Write
L		L	H	H	D _{OUT}	Read ^[35]
H	X	L	H	X	High-Z	Outputs Disabled

Address Counter Control Operation^[35, 39, 40, 41]

Address	Previous Address	CLK	ADS	CNTEN	CNTRST	I/O	Mode	Operation
X	X		X	X	L	D _{out(0)}	Reset	Counter Reset to Address 0
A _n	X		L	X	H	D _{out(n)}	Load	Address Load into Counter
X	A _n		H	H	H	D _{out(n)}	Hold	External Address Blocked—Counter Disabled
X	A _n		H	L	H	D _{out(n+1)}	Increment	Counter Enabled—Internal Address Generation

Notes:

35. "X" = "Don't Care", "H" = V_{IH}, "L" = V_{IL}.

36. ADS, CNTEN, CNTRST = "Don't Care".

37. OE is an asynchronous input signal.

38. When CE changes state in the pipelined mode, deselection and read happen in the following clock cycle.

39. CE₀ and OE = V_{IL}; CE₁ and R/W = V_{IH}.

40. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.

41. Counter operation is independent of CE₀ and CE₁.

Ordering Information

16K x16 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5 ^[1, 2]	CY7C09269V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09269V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5 ^[2]	CY7C09269V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09269V-7AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
9	CY7C09269V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09269V-9AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
	CY7C09269V-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09269V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09269V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

32K x16 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5 ^[1, 2]	CY7C09279V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09279V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5 ^[2]	CY7C09279V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09279V-7AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
9	CY7C09279V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09279V-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09279V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09279V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

64K x16 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5 ^[1, 2]	CY7C09289V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09289V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5 ^[2]	CY7C09289V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09289V-7AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
9	CY7C09289V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09289V-9AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
	CY7C09289V-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C09289V-9AXI	A100	100-Pin Pb-Free Thin Quad Flat Pack	Industrial
12	CY7C09289V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09289V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

16K x18 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5 ^[1, 2]	CY7C09369V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09369V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5 ^[2]	CY7C09369V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09269V-7AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
	CY7C09369V-7AI	A100	100-Pin Thin Quad Flat Pack	Industrial
9	CY7C09369V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09369V-9AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
	CY7C09369V-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09369V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09369V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

32K x18 3.3V Synchronous Dual-Port SRAM

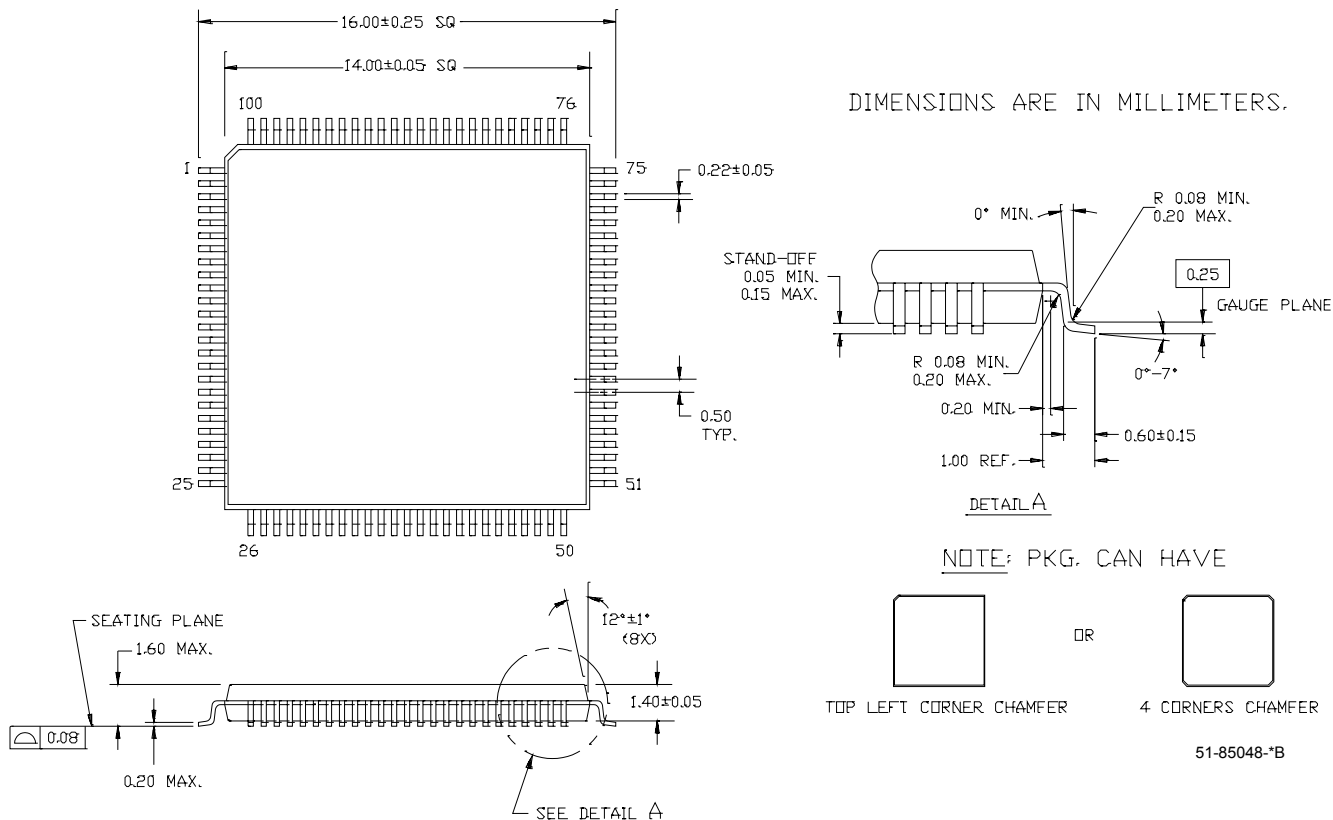
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5 ^[1, 2]	CY7C09379V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09379V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5 ^[2]	CY7C09379V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
9	CY7C09379V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09379V-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09379V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09379V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

64K x18 3.3V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5 ^[1, 2]	CY7C09389V-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09389V-6AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
7.5 ^[2]	CY7C09389V-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09389v-7AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
9	CY7C09389V-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09389V-9AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
	CY7C09389V-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C09389V-9AXI	A100	100-Pin Pb-Free Thin Quad Flat Pack	Industrial
12	CY7C09389V-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09389V-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

Package Diagram

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100 100-Pin Pb-Free Thin Plastic Quad Flat Pack (TQFP) A100



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Document History Page

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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110215	12/18/01	SZV	Change from Spec number: 38-00668 to 38-06056
*A	122306	12/27/02	RBI	Power up requirements added to Maximum Ratings Information
*B	344354	See ECN	PCX	Added Pb-Free Part Ordering Information

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