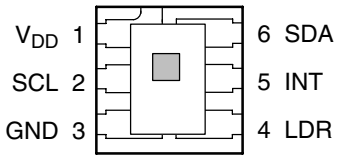
Features

- **Proximity Detection with an Integrated LED Driver in a Single Device**
- **Register Set- and Pin-Compatible with the TSL2x71 Series**
- **Proximity Detection**
  - **Reduced Proximity Count Variation**
  - **Programmable Offset Control Register**
  - **Saturation Indicator**
  - **Programmable Analog Gain and Integration Time**
  - **Current Sink Driver for External IR LED**
  - **16,000:1 Dynamic Range**
- **Maskable Proximity Interrupt**
  - **Programmable Upper and Lower Thresholds with Persistence Filter**
- **Power Management**
  - **Low Power 2.2 μA Sleep State with User-Selectable Sleep-After-Interrupt Mode**
  - **90 μA Wait State with Programmable Wait Time from 2.7 ms to > 8 seconds**
- **I^2C Fast Mode Compatible Interface**
  - **Data Rates up to 400 kbit/s**
  - **Input Voltage Levels Compatible with V_{DD} or 1.8-V Bus**
- **Small 2 mm × 2 mm Dual Flat No-Lead (FN) Package**

PACKAGE FN
DUAL FLAT NO-LEAD
(TOP VIEW)



Not Actual Size

Applications

- **Mobile Handset Touchscreen Control and Automatic Speakerphone Enable**
- **Mechanical Switch Replacement**
- **Printer Paper Alignment**

End Products and Market Segments

- **Mobile Handsets, Tablets, Laptops, and HDTVs**
- **White Goods**
- **Toys**
- **Digital Signage**
- **Printers**

Description

The TSL2672 family of devices provides proximity detection when coupled with an external IR LED. The devices incorporate a constant-current LED sink driver to pulse the external IR LED and achieve very low average power consumption using the low-power wait state with programmable wait time between proximity measurements. In addition, the devices are register-set and pin-compatible with the TSL2671 series and include a number of new and improved features, such as improved signal-to-noise and measurement accuracy. A proximity offset register allows compensation for optical system crosstalk between the IR LED and the sensor. To prevent false measurements, a proximity saturation bit indicates that the internal analog circuitry saturated. Interrupts have been enhanced with the addition of a sleep-after-interrupt feature that also allows for single-cycle operation.

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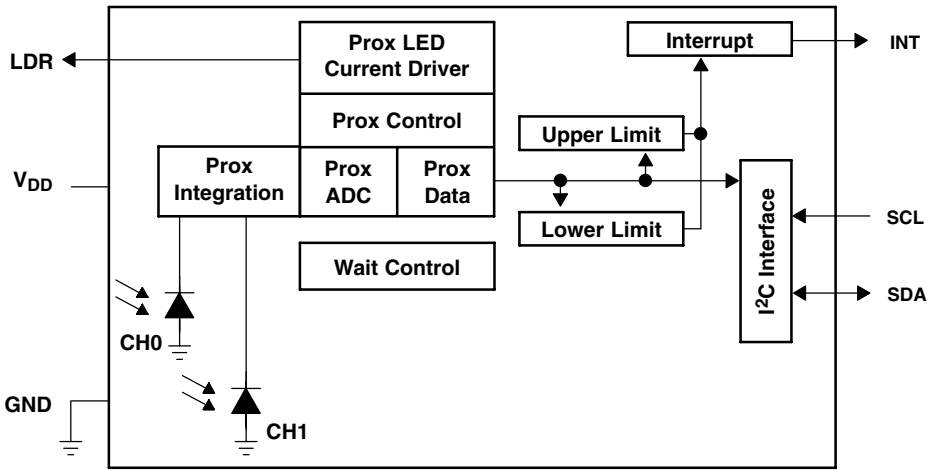
Functional Block Diagram



Detailed Description

Proximity detection requires only a single external LED. This external LED is driven by an internal LED current driver, which pulses the LED with current for approximately 7 microseconds. The number of pulses, from 1 to 255, and the current level, from 1.9 mA to 120 mA, can be programmed and together provide a 16,000:1 contiguous dynamic range. Because the driver is a constant current sink, no external current limiting resistor is required to protect the LED.

In addition to the internal LED current driver, the TSL2672 proximity detector provides on-chip photodiodes, oscillator, integrating amplifier, ADC, state machine controller, programmable interrupt and I^2C interface to provide a complete proximity detection solution.

Each device has two photodiodes; a channel 0 photodiode (CH0), which is responsive to both visible and infrared light, and a channel 1 photodiode (CH1), which is primarily responsive to only infrared light. The user selects the appropriate diode for their application.

The integrating amplifier and ADC converts the selected photodiode current into a digital value providing up to 16 bits of resolution. Upon completion of a proximity conversion cycle, the result is transferred to the proximity data registers where it is available to be read.

Communication with the device is accomplished over a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more noise-immune when compared to an analog interface.

The device provides a separate pin for level-style interrupts to simplify and improve system efficiency by eliminating the need to poll for proximity data. When interrupts are enabled, an interrupt is generated when the proximity data either exceeds an upper threshold or is less than a lower threshold. Once generated, the interrupt remains asserted until cleared by the controlling firmware. In addition, a programmable interrupt persistence filter allows the user to determine the number of consecutive out-of-range measurements necessary to trigger an interrupt.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
GND	3		Power supply ground. All voltages are referenced to GND.
INT	5	O	Interrupt — open drain (active low).
LDR	4	O	LED driver for proximity emitter — open drain.
SCL	2	I	I^2C serial clock input terminal — clock signal for I^2C serial data.
SDA	6	I/O	I^2C serial data I/O terminal — serial data I/O for I^2C .
V_{DD}	1		Supply voltage.

Available Options

DEVICE	ADDRESS	PACKAGE – LEADS	INTERFACE DESCRIPTION	ORDERING NUMBER
TSL26721	0x39	FN–6	I^2C Vbus = V_{DD} Interface	TSL26721FN
TSL26723	0x39	FN–6	I^2C Vbus = 1.8 V Interface	TSL26723FN
TSL26725†	0x29	FN–6	I^2C Vbus = V_{DD} Interface	TSL26725FN
TSL26727†	0x29	FN–6	I^2C Vbus = 1.8 V Interface	TSL26727FN

† Contact TAOS for availability.

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (Note 1) . . . . . 3.8 V
Input terminal voltage . . . . . –0.5 V to 3.8 V
Output terminal voltage (except LDR) . . . . . –0.5 V to 3.8 V
Output terminal voltage (LDR) . . . . . 5 V
Output terminal current (except LDR) . . . . . –1 mA to 20 mA
Storage temperature range, T_{stg} . . . . . –40°C to 85°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (TSL26721 & TSL26725) (I^2C V_{bus} = V_{DD})		2.4	3	3.6	V
Supply voltage, V_{DD} (TSL26723 & TSL26727) (I^2C V_{bus} = 1.8 V)		2.7	3	3.6	V
LED driver voltage, V_{LDR}	LDR pulse on	0		3.6	V
	LDR pulse off	0		4.8	
Operating free-air temperature, T_A		–30		70	°C

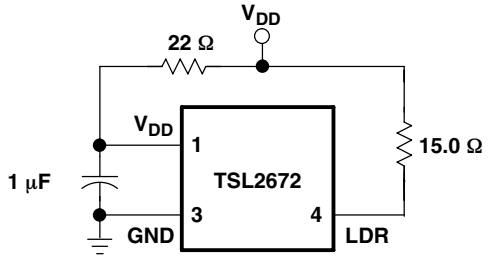
Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Active — LDR pulse off		200	250	µA
		Wait state		90		
		Sleep state — no I^2C activity		2.2	4	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		–5		5	µA
I_{LEAK}	Leakage current, LDR pin		–5		5	µA
V_{IH}	SCL, SDA input high voltage	TSL26721, TSL26725	0.7 V_{DD}			V
		TSL26723, TSL26727	1.25			
V_{IL}	SCL, SDA input low voltage	TSL26721, TSL26725			0.3 V_{DD}	V
		TSL26723, TSL26727			0.54	

Proximity Characteristics, V_{DD} = 3 V, T_A = 25°C, PGAIN = 1×, PEN = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply current	LDR pulse on			3		mA
	ADC conversion time step size	PTIME = 0xFF		2.58	2.73	2.9	ms
	ADC number of integration steps (Note 1)			1		256	steps
	ADC counts per step (Note 1)	PTIME = 0xFF		0		1023	counts
	ADC count value	λ_p = 850 nm, E_e = 263.4 µW/cm², PTIME = 0xFB, PPULSE = 4	CH0 diode	1500	2000	2500	counts
			CH1 diode	900	1200	1500	
	ADC output responsivity	λ_p = 850 nm, PTIME = 0xFB, PPULSE = 1	CH0 diode		1.90		counts/ µW/cm²
			CH1 diode		1.14		
	Gain scaling, relative to 1× gain setting	PGAIN = 2×			2		×
		PGAIN = 4×			4		
		PGAIN = 8×			8		
	Noise (Notes 1, 2, 3)	E_e = 0, PTIME = 0xFB, PPULSE = 4 (Note 6)	CH0 diode		0.5		% FS
			CH1 diode		0.5		
	LED pulse count (Note 1)			0		255	pulses
	LED pulse period				16.0		µs
	LED pulse width — LED on time				7.3		µs
	LED drive current	I_{SINK} sink current @ 1.6 V, LDR pin	120 mA: PDRIVE = 0 & PDL = 0	87	116	145	mA
			60 mA: PDRIVE = 1 & PDL = 0		58		
			30 mA: PDRIVE = 2 & PDL = 0		29		
			15 mA: PDRIVE = 3 & PDL = 0		14.5		
			15 mA: PDRIVE = 0 & PDL = 1		12.9		
			7.5 mA: PDRIVE = 1 & PDL = 1		6.4		
			3.8 mA: PDRIVE = 2 & PDL = 1		3.2		
			1.9 mA: PDRIVE = 3 & PDL = 1		1.6		
	Maximum operating distance (Notes 1, 4, 5)	PDRIVE = 0 and PDL = 0 (116 mA), PPULSE = 64 Emitter: λ_p = 850 nm, 20° half angle, and 60 mW/sr Object: 16 × 20-inch, 90% reflective Kodak Gray Card (white surface) Optics: Open view (no glass, no optical attenuation)		18			inches

NOTES: 1. Parameter is ensured by design or characterization and is not tested.
2. Proximity noise is defined as one standard deviation of 600 samples.
3. Proximity noise typically increases as $\sqrt{PPULSE}$
4. Greater operating distances are achievable with appropriate optical system design considerations. See available TAOS application notes for additional information.
5. Maximum operating distance is dependent upon emitter and the reflective properties of the object's surface.
6. Proximity noise test was done using the following circuit:



Wait Characteristics, V_{DD} = 3 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CHANNEL	MIN	TYP	MAX	UNIT
Wait step size	WTIME = 0xFF		2.58	2.73	2.9	ms
Wait number of integration steps (Note 1)			1		256	steps

NOTE 1: Parameter ensured by design and is not tested.

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER†		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0			µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

† Specified by design and characterization; not production tested.

PARAMETER MEASUREMENT INFORMATION

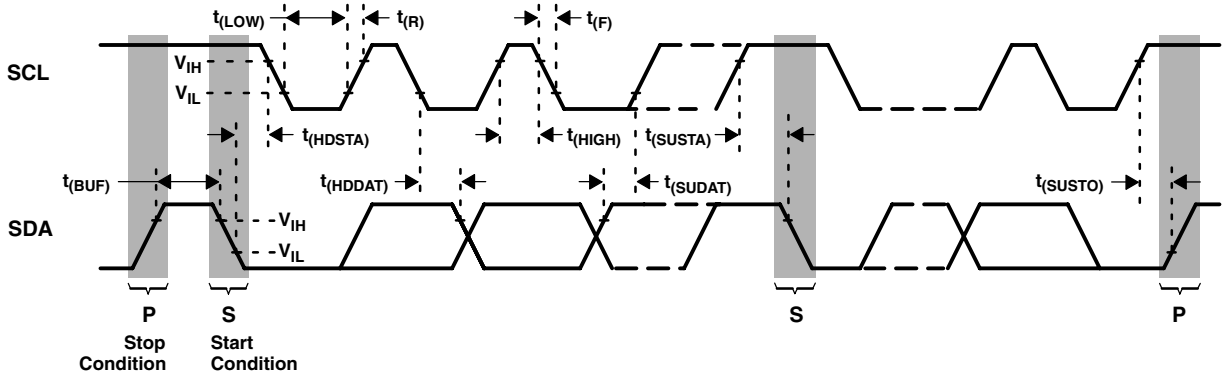


Figure 1. Timing Diagrams

TYPICAL CHARACTERISTICS

SPECTRAL RESPONSIVITY

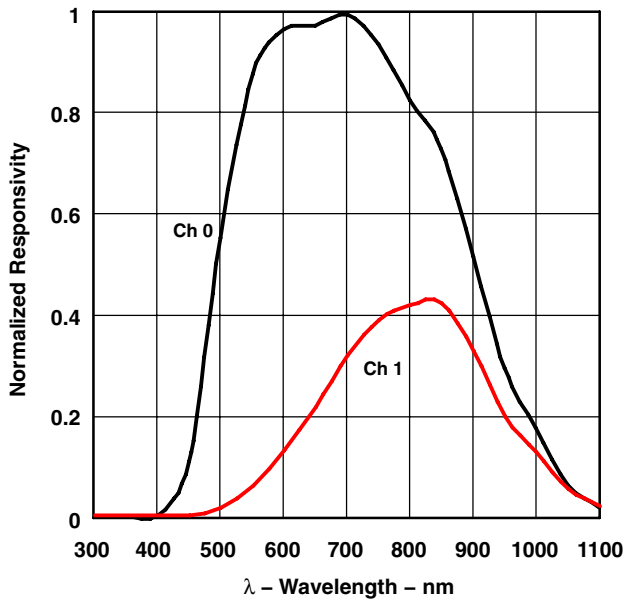


Figure 2

NORMALIZED RESPONSIVITY vs. ANGULAR DISPLACEMENT

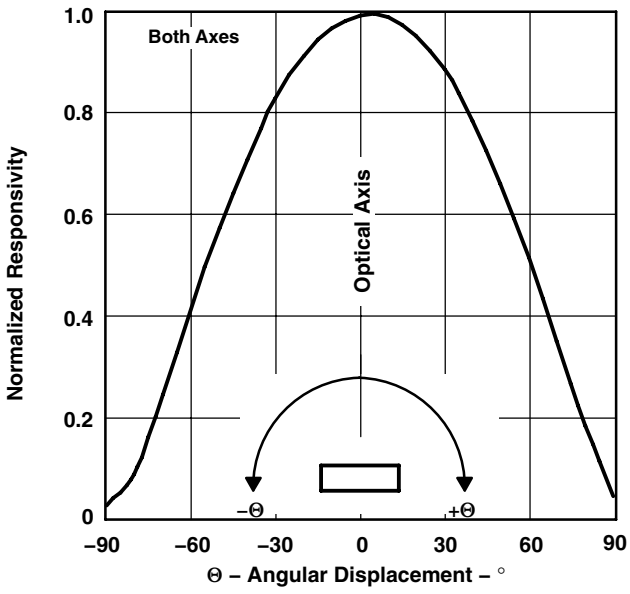


Figure 3

TYPICAL LDR CURRENT vs. VOLTAGE

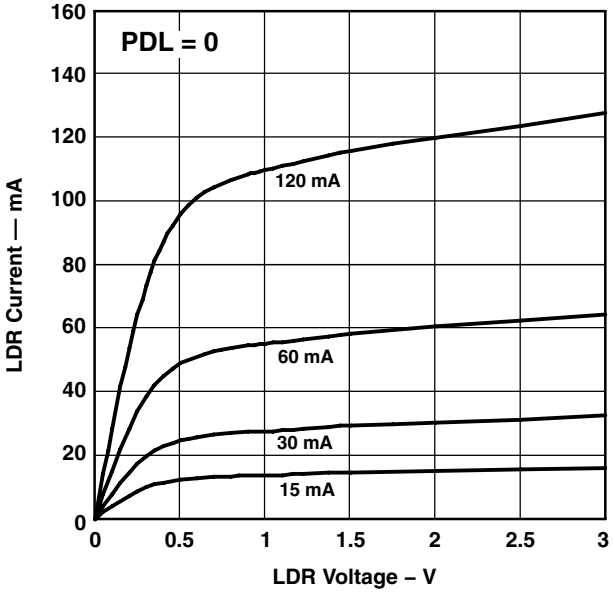


Figure 4

TYPICAL LDR CURRENT vs. VOLTAGE

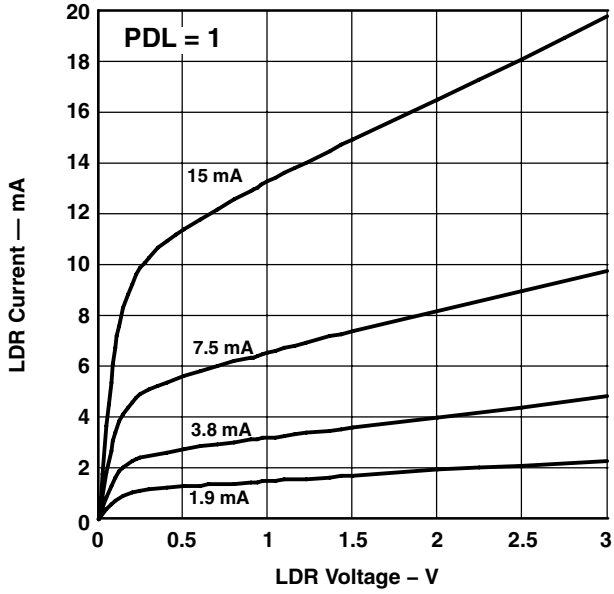


Figure 5

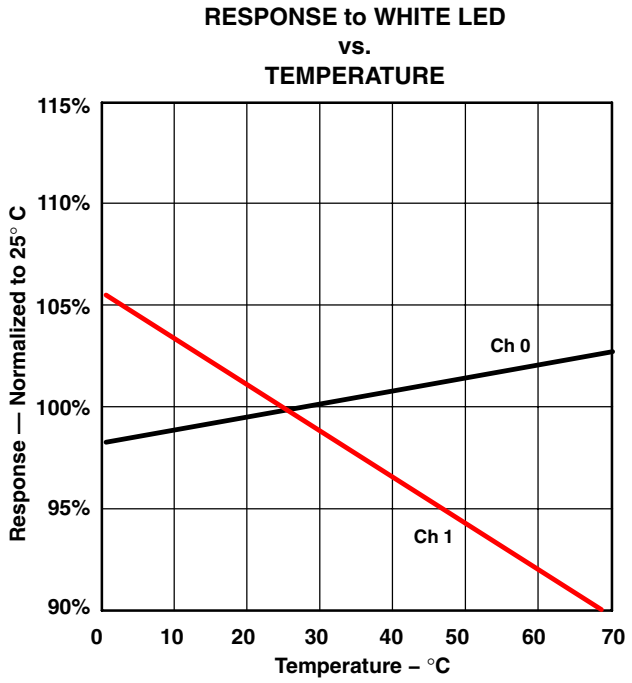


Figure 6

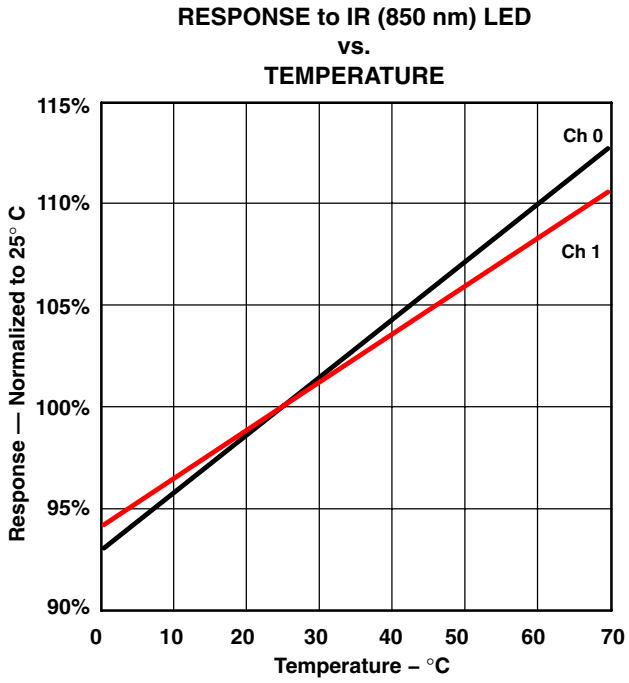


Figure 7

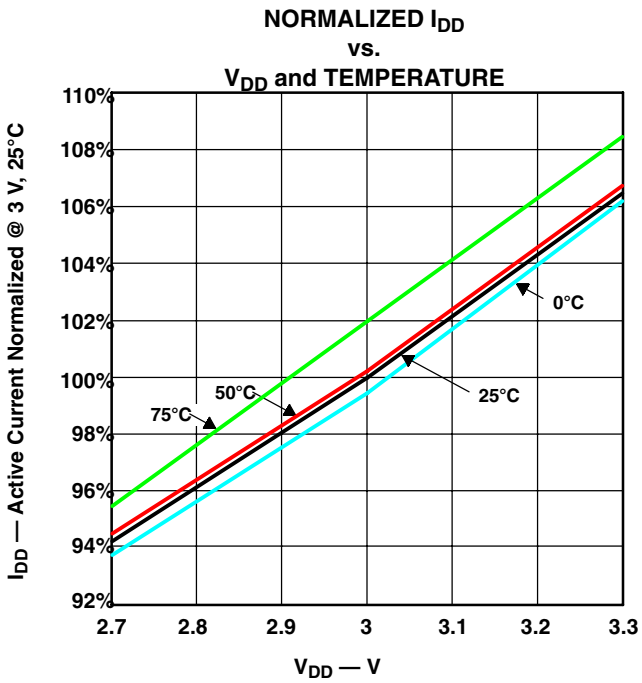


Figure 8

PRINCIPLES OF OPERATION

System States

An internal state machine provides system control of the proximity detection and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I^2C bus, the device transitions to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until the proximity function is enabled. Once enabled, the device will execute the Prox and Wait states in sequence as indicated in Figure 9. Upon completion and return to Idle, the device will automatically begin a new prox-wait cycle as long as PON and PEN remain enabled.

If the Prox function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I^2C command is received. See the Interrupts section for additional information.

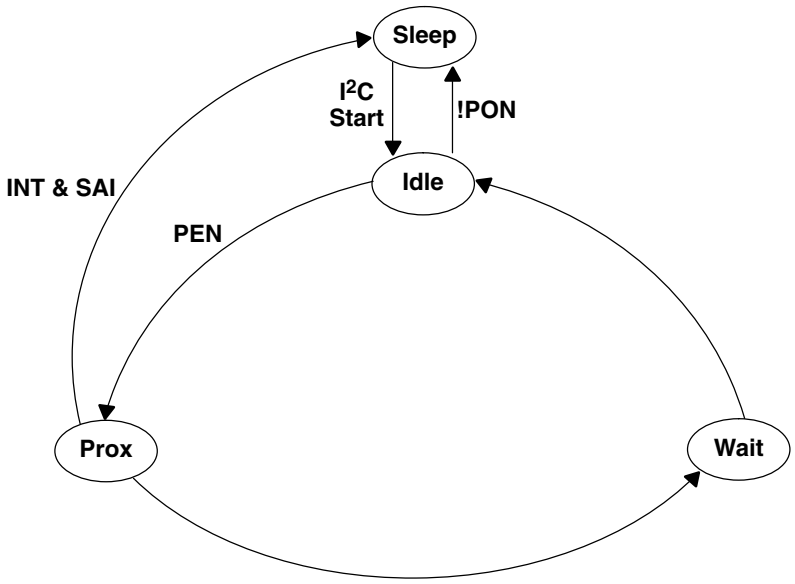


Figure 9. Simplified State Diagram

Proximity Detection

Proximity detection is accomplished by measuring the amount of light energy, generally from an IR LED, reflected off an object to determine its distance. The proximity light source, which is external to the TSL2672 device, is driven by the integrated proximity LED current driver as shown in Figure 10.

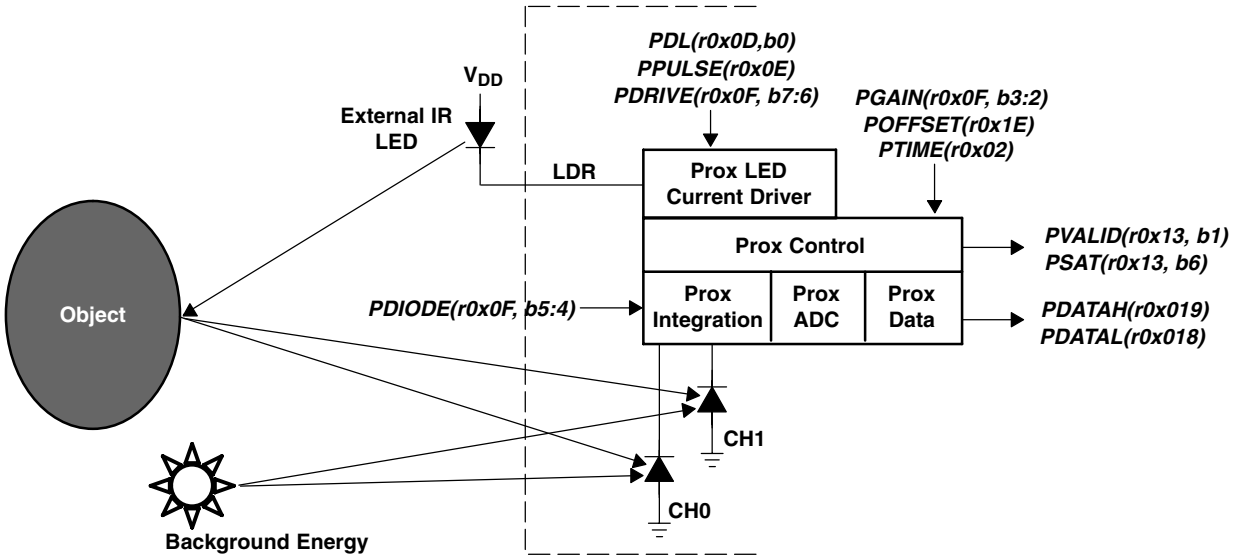


Figure 10. Proximity Detection

The LED current driver, output on the LDR terminal, provides a regulated current sink that eliminates the need for an external current limiting resistor. The combination of proximity LED drive strength (PDRIVE) and proximity drive level (PDL) determine the drive current. PDRIVE sets the drive current to 120 mA, 60 mA, 30 mA, or 15 mA when PDL is not asserted. However, when PDL is asserted, the drive current is reduced by a factor of about 8 at V_{LDR} = 1.6 V. To drive an external light source with more than 120 mA or to minimize on-chip ground bounce, LDR can be used to drive an external p-type transistor, which in turn drives the light source.

Referring to the Detailed State Machine figure, the LED current driver pulses the external IR LED as shown in Figure 11 during the Prox Accum state. Figure 11 also illustrates that the LED On pulse has a fixed width of 7.3 μs and period of 16.0 μs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

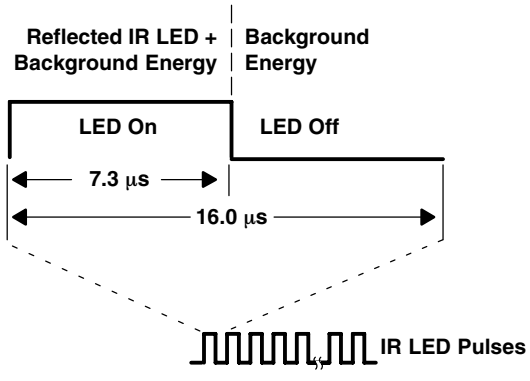


Figure 11. Proximity LED Current Driver Waveform

Figure 10 illustrates light rays emitting from an external IR LED, reflecting off an object, and being absorbed by the CH0 and CH1 photodiodes. The proximity diode selector (PDIODE) determines which of the two photodiodes is used for a given proximity measurement. Note that neither photodiode is selected when the device first powers up, so PDIODE must be set for proximity detection to work.

Referring again to Figure 11, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the external IR LED energy to accumulate from pulse to pulse. The proximity gain (PGAIN) determines the integration rate, which can be programmed to 1×, 2×, 4×, or 8× gain. At power up, PGAIN defaults to 1× gain, which is recommended for most applications. For reference, PGAIN equal to 8× is comparable to the TSL2771 1× gain setting. During LED On time integration, the proximity saturation bit in the Status register (0x13) will be set if the integrator saturates. This condition can occur if the proximity gain is set too high for the lighting conditions, such as in the presence of bright sunlight. Once asserted, PSAT will remain set until a special function proximity interrupt clear command is received from the host (see command register).

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which is programmable from 1 to 256 2.73-ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.73-ms ADC conversion time (0xFF).

In many practical proximity applications, a number of optical system and environmental conditions can produce an offset in the proximity measurement result. To counter these effects, a proximity offset (POFFSET) is provided which allows the proximity data to be shifted positive or negative. Additional information on the use of the proximity offset feature is provided in available TAOS application notes.

Once the first proximity cycle has completed, the proximity valid (PVALID) bit in the Status register will be set and remain set until the proximity detection function is disabled (PEN).

For additional information on using the proximity detection function behind glass and for optical system design guidance, please see available TAOS application notes.

Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for proximity values outside a user-defined range. While the interrupt function is always enabled and its status is available in the Status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) field in the Enable register (0x00).

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired proximity range. An interrupt can be generated when the proximity data (PDATA) is less than the proximity interrupt low threshold (PILTx) or is greater than the proximity interrupt high threshold (PIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides an interrupt persistence feature. The persistence filter allows the user to specify the number of consecutive out-of-range proximity occurrences before an interrupt is generated. The persistence filter register (0x0C) allows the user to set the proximity persistence filter (PPERS) values. See the persistence filter register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see Command register).

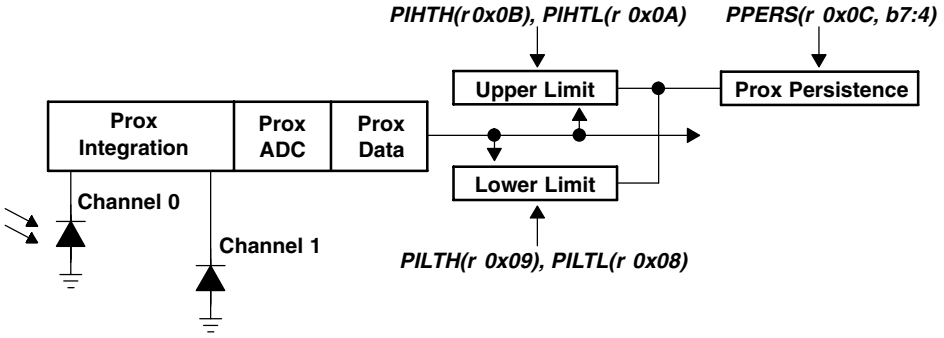


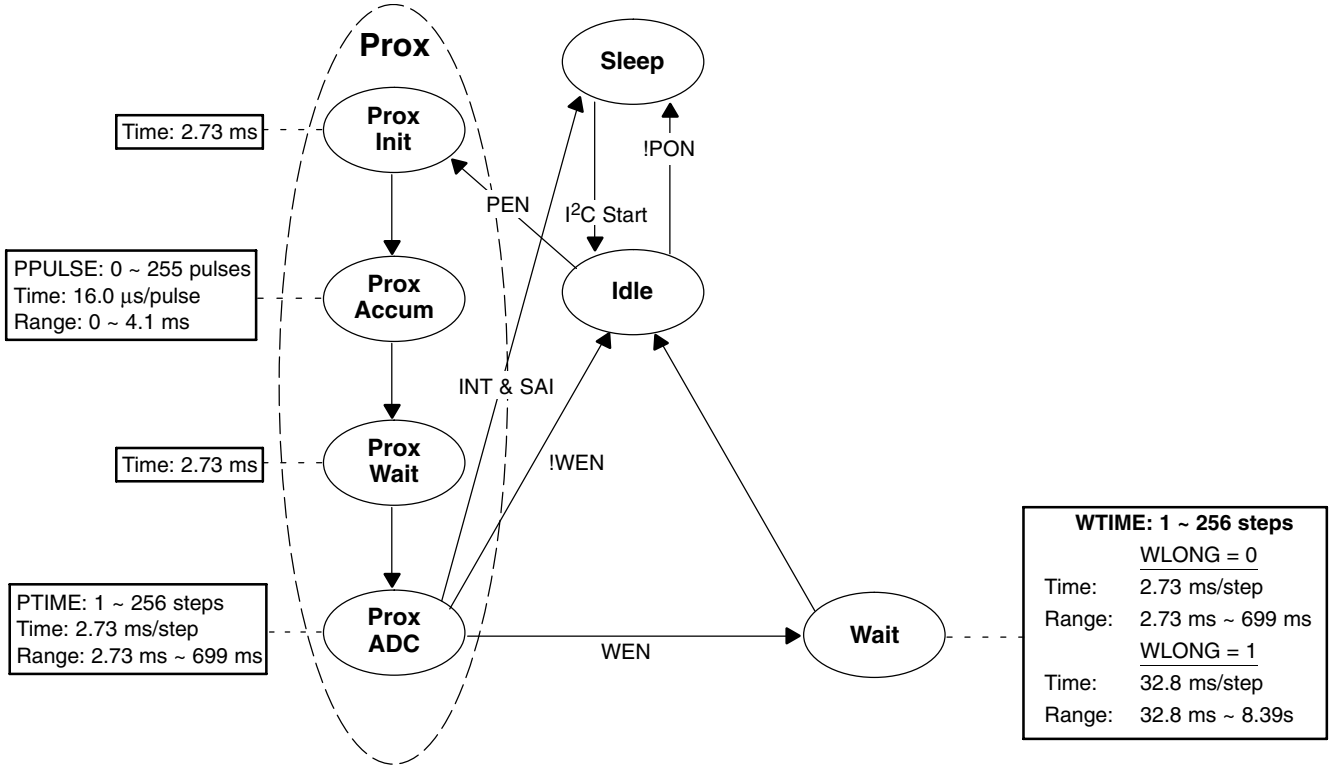
Figure 12. Programmable Interrupt

System Timing

The system state machine shown in Figure 9 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing.

When the proximity detection feature is enabled (PEN), the state machine transitions through the Prox Init, Prox Accum, Prox Wait, and Prox ADC states. The Prox Init and Prox Wait times are a fixed 2.73 ms, whereas the Prox Accum time is determined by the number of proximity LED pulses (PPULSE) and the Prox ADC time is determined by the integration time (PTIME). The formulas to determine the Prox Accum and Prox ADC times are given in the associated boxes in Figure 12. If an interrupt is generated as a result of the proximity cycle, it will be asserted at the end of the Prox ADC state and transition to the Sleep state if SAI is enabled.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 13.



Note: PON, PEN, WEN, and SAI are fields in the Enable register (0x00).

Figure 13. Detailed State Diagram

Power Management

Power consumption can be managed with the Wait state, because the Wait state typically consumes only 90 μA of I_{DD} current. An example of the power management feature is given below. With the assumptions provided in the example, average I_{DD} is estimated to be 167 μA.

Table 1. Power Management

SYSTEM STATE MACHINE STATE	PROGRAMMABLE PARAMETER	PROGRAMMED VALUE	DURATION	TYPICAL CURRENT
Prox Init			2.73 ms	0.200 mA
Prox Accum	PPULSE	0x04	0.064 ms	
Prox Accum – LED On			0.029 ms (Note 1)	119 mA
Prox Accum – LED OFF			0.035 ms (Note 2)	0.200 mA
Prox Wait			2.73 ms	0.200 mA
Prox ADC	PTIME	0xFF	2.73 ms	0.200 mA
Wait	WTIME	0xEE	49.2 ms	0.090 mA
	WLONG	0		

NOTES: 1. Prox Accum – LED On time = 7.3 μs per pulse × 4 pulses = 29.3μs = 0.029 ms
2. Prox Accum – LED Off time = 8.7 μs per pulse × 4 pulses = 34.7μs = 0.035 ms

Average I_{DD} Current = ((0.029 × 119) + (0.035 x 0.200) + (2.73 × 0.200) + (49.2 × 0.090) + (2.73 × 0.200 × 2)) / 57 ≈ 167 μA

Keeping with the same programmed values as the example, Table 2 shows how the average I_{DD} current is affected by the Wait state time, which is determined by WEN, WTIME, and WLONG. Note that the worst-case current occurs when the Wait state is not enabled.

Table 2. Average I_{DD} Current

WEN	WTIME	WLONG	WAIT STATE	AVERAGE I_{DD} CURRENT
0	n/a	n/a	0 ms	622 μA
1	0xFF	0	2.73 ms	490 μA
1	0xEE	0	49.2 ms	167 μA
1	0x00	0	699 ms	97 μA6
1	0x00	1	8389 ms	91 μA

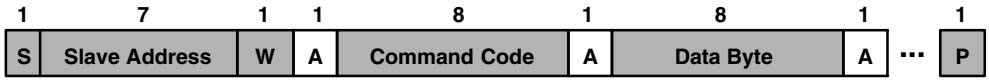
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

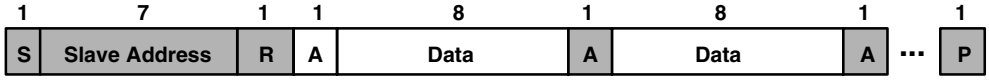
The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 14). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c–bus.org/references/.

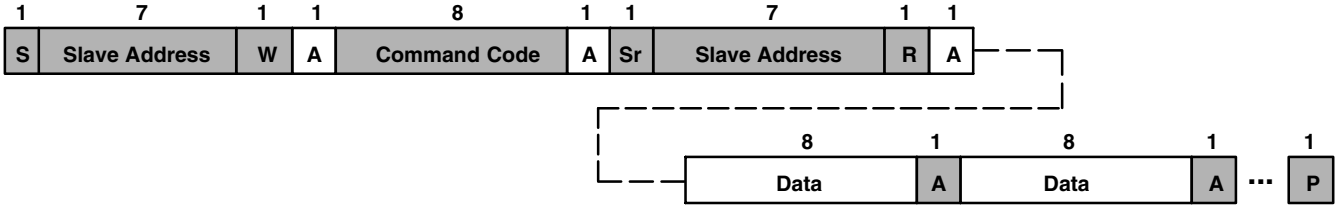
A Acknowledge (0)
N Not Acknowledged (1)
P Stop Condition
R Read (1)
S Start Condition
Sr Repeated Start Condition
W Write (0)
... Continuation of protocol
Master-to-Slave
Slave-to-Master



I²C Write Protocol



I²C Read Protocol



I²C Read Protocol — Combined Format

Figure 14. I²C Protocols

Register Set

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 1.

Table 3. Register Address

ADDRESS	RESISTER NAME	R/W	REGISTER FUNCTION	RESET VALUE
––	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filter	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x18	PDATAL	R	Proximity data low byte	0x00
0x19	PDATAH	R	Proximity data high byte	0x00
0x1E	POFFSET	R/W	Proximity Offset register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control-status-data register for subsequent read/write operations.

Command Register

The command register specifies the address of the target register for future read and write operations, as well as issues special function commands.

Table 4. Command Register

	7	6	5	4	3	2	1	0	
COMMAND	**CMD**	**TYPE**		**ADDR/SF**					**Reset 0x00**

FIELD	BITS	DESCRIPTION	
CMD	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**DESCRIPTION**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
		Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.	
ADDR/SF	4:0	Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-data register for subsequent read and write transactions. The field values listed below apply only to special function commands:	
		FIELD VALUE	**DESCRIPTION**
		00100	Interrupt set — forces an interrupt
		00101	Proximity interrupt clear
		other	Reserved — Do not write
		The interrupt set special function command sets the interrupt bits in the status register (0x13). For the interrupt to be visible on the INT pin, the proximity interrupt enable bit (PIEN) in the enable register (0x00) must be asserted. The interrupt set special function must be cleared with an interrupt clear special function. The proximity interrupt clear special function clears any pending interrupt and is self clearing.	

Enable Register (0x00)

The enable register is used to power the device on/off, enable functions, and interrupts.

Table 5. Enable Register

	7	6	5	4	3	2	1	0	
ENABLE	Reserved	SAI	PIEN	Reserved	WEN	PEN	Reserved	PON	Reset 0x00

FIELD	BITS	DESCRIPTION
Reserved	7	Reserved. Write as 0.
SAI	6	Sleep after interrupt. When asserted, the device will power down at the end of a proximity cycle if an interrupt has been generated.
PIEN	5	Proximity interrupt enable. When enabled, the proximity interrupt drives the INT pin. When disabled, the interrupt is masked from the INT pin, but remains visible in the Status register (0x13).
Reserved	4	Reserved. Write as 0.
WEN	3	Wait enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
Reserved	1	Reserved. Write as 0.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channel to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

Proximity Time Register (0x02)

The proximity time register controls the integration time of the proximity ADC in 2.73 ms increments. Upon power up, the proximity time register is set to 0xFF. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

Table 6. Proximity Integration Time Control Register

FIELD	BITS	DESCRIPTION			
PTIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.73 ms	1023

Wait Time Register (0x03)

Wait time is set 2.73 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

Table 7. Wait Time Register

FIELD	BITS	DESCRIPTION			
WTIME	7:0	REGISTER VALUE	WAIT TIME	TIME (WLONG = 0)	TIME (WLONG = 1)
		0xFF	1	2.73 ms	0.033 sec
		0xB6	74	202 ms	2.4 sec
		0x00	256	699 ms	8.4 sec

NOTE: The Proximity Wait Time Register should be configured before PEN is asserted.

Proximity Interrupt Threshold Registers (0x08 – 0x0B)

The proximity interrupt threshold registers provide the upper and lower threshold values to the proximity interrupt comparators. See Interrupts in the Principles of Operation section for detailed information. Upon power up, the interrupt threshold registers reset to 0x00.

Table 8. Proximity Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity interrupt low threshold low byte
PILTH	0x09	7:0	Proximity interrupt low threshold high byte
PIHTL	0x0A	7:0	Proximity interrupt high threshold low byte
PIHTH	0x0B	7:0	Proximity interrupt high threshold high byte

Interrupt Persistence Filter Register (0x0C)

The interrupt persistence filter sets the number of consecutive proximity cycles that are out-of-range before an interrupt is generated. Out-of-range is determined by the proximity interrupt threshold registers (0x08 through 0x0B). See Interrupts in the Principles of Operation section for further information. Upon power up, the interrupt persistence filter register resets to 0x00, which will generate an interrupt at the end of each proximity cycle.

Table 9. Interrupt Persistence Filter Register

	7	6	5	4	3	2	1	0	
PERS	PPERS				Reserved				Reset 0x00

FIELD	BITS	DESCRIPTION	
PPERS	7:4	Proximity persistence. Controls rate of proximity interrupt to the host processor.	
		FIELD VALUE	INTERRUPT PERSISTENCE FUNCTION
		0000	Every proximity cycle generates an interrupt
		0001	1 proximity value out of range
		0010	2 consecutive proximity values out of range
		...	...
		1111	15 consecutive proximity values out of range
Reserved	3:0	Reserved. Write as 0.	

Configuration Register (0x0D)

The configuration register sets the proximity LED drive level and wait long time.

Table 10. Configuration Register

	7	6	5	4	3	2	1	0	
CONFIG	Reserved						WLONG	PDL	Reset 0x00

FIELD	BITS	DESCRIPTION
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
PDL	0	Proximity drive level. When asserted, the proximity LDR drive current is reduced by 9.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that the LDR pin will generate during the Prox Accum state.

Table 11. Proximity Pulse Count Register

	7	6	5	4	3	2	1	0	
PPULSE	PPULSE								Reset 0x00

FIELD	BITS	DESCRIPTION
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Table 12. Control Register

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		PDIODE		PGAIN		Reserved		Reset 0x00

FIELD	BITS	DESCRIPTION		
PDRIVE (Note 1)	7:6	Proximity LED Drive Strength.		
		FIELD VALUE	LED STRENGTH — PDL = 0	LED STRENGTH — PDL = 1
		00	120 mA	15 mA
		01	60 mA	7.5 mA
		10	30 mA	3.8 mA
		11	15 mA	1.9 mA
PDIODE	5:4	Proximity Diode Selector.		
		FIELD VALUE	DIODE SELECTION	
		00	Proximity uses neither diode	
		01	Proximity uses the CH0 diode	
		10	Proximity uses the CH1 diode	
		11	Reserved — Do not write	
PGAIN	3:2	Proximity Gain.		
		FIELD VALUE	PROXIMITY GAIN VALUE	
		00	1× gain	
		01	2× gain	
		10	4× gain	
		11	8× gain	
Reserved	1:0	Reserved. Write as 0.		

NOTE 1: LED STRENGTH currents are nominal values. Specifications can be found in the Proximity Characteristics table.

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Table 13. ID Register

	7	6	5	4	3	2	1	0	
ID	ID								Reset ID

FIELD	BITS	DESCRIPTION	
ID	7:0	Part number identification	0x32 = TSL26721 & TSL26725
			0x3B = TSL26723 & TSL2777

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Table 14. Status Register

	7	6	5	4	3	2	1	0	
STATUS	Reserved	PSAT	PINT	Reserved			PVALID	Reserved	Reset 0x00

FIELD	BIT	DESCRIPTION
Reserved	7	Reserved. Read as 0.
PSAT	6	Proximity Saturation. Indicates that the proximity measurement saturated.
PINT	5	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
Reserved	4:2	Reserved. Read as 0.
PVALID	1	Proximity Valid. Indicates that the proximity channel has completed an integration cycle after PEN has been asserted.
Reserved	0	Reserved. Read as 0.

Proximity Data Registers (0x18 – 0x19)

Proximity data is stored as a 16-bit value. When the lower byte is read, the upper byte is latched into a shadow register. The shadow register ensures that both bytes are the result of the same proximity cycle, even if additional proximity cycles occur between the lower byte and upper byte register readings. The simplest way to read both bytes is to perform a two-byte I^2C read operation using the auto-increment protocol, which is set in the Command register TYPE field.

Table 15. Proximity Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

Proximity Offset Register (0x1E)

The 8-bit proximity offset register provides compensation for proximity offsets caused by device variations, optical crosstalk, and other environmental factors. Proximity offset is a sign-magnitude value where the sign bit, bit 7, determines if the offset is negative (bit 7 = 0) or positive (bit 7 = 1). At power up, the register is set to 0x00. The magnitude of the offset compensation depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE). Because a number of environmental factors contribute to proximity offset, this register is best suited for use in an adaptive closed-loop control system. See available TAOS application notes for proximity offset register application information.

Table 16. Proximity Offset Register

	7	6	5	4	3	2	1	0	
POFFSET	**SIGN**	**MAGNITUDE**							**Reset 0x00**

FIELD	BIT	DESCRIPTION
SIGN	7	Proximity Offset Sign. The offset sign shifts the proximity data negative when equal to 0 and positive when equal to 1.
MAGNITUDE	6:0	Proximity Offset Magnitude. The offset magnitude shifts the proximity data positive or negative, depending on the proximity offset sign. The actual amount of the shift depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE).

APPLICATION INFORMATION: HARDWARE

LED Driver Pin with Proximity Detection

In a proximity sensing system, the IR LED can be pulsed by the TSL2672 with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LED, the key goal can be meet. Place a 1-μF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LED anode, and a 22-μF capacitor at the output of the LED voltage regulator to supply the 100-mA current surge.

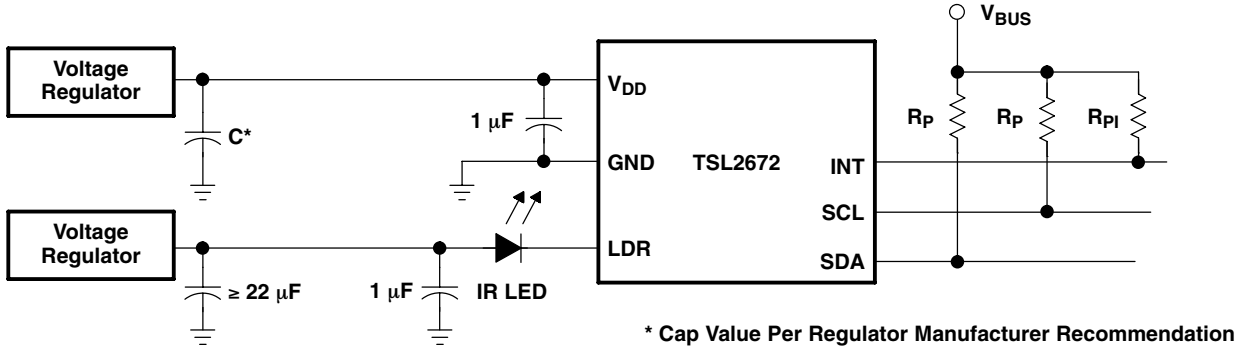


Figure 15. Proximity Sensing Using Separate Power Supplies

If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22-Ω resistor in series with the V_{DD} supply line and a 1-μF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

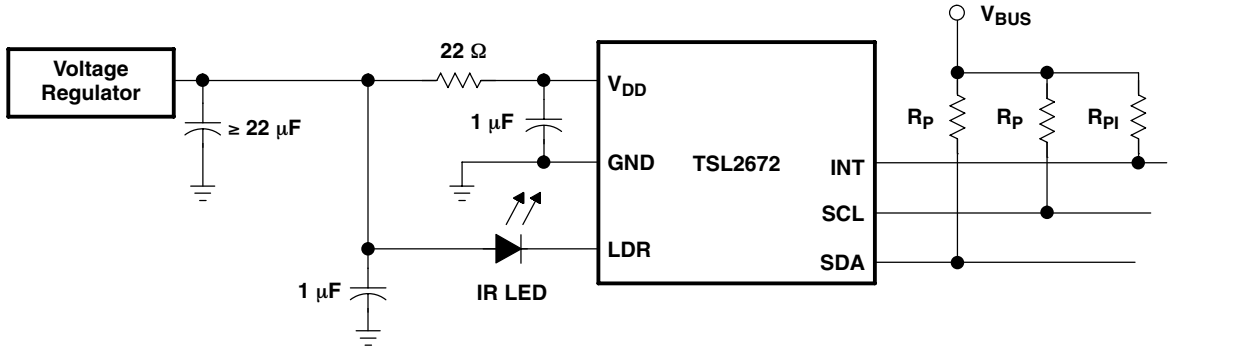


Figure 16. Proximity Sensing Using Single Power Supply

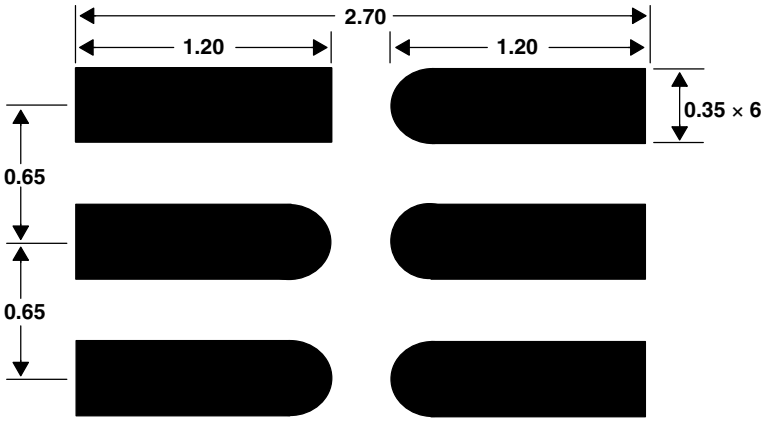
V_{BUS} in the above figures refers to the I^2C bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

The I^2C signals and the Interrupt are open-drain outputs and require pull–up resistors. The pull-up resistor (R_P) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The TAOS EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

APPLICATION INFORMATION: HARDWARE

PCB Pad Layouts

Suggested land pattern based on the IPC–7351B Generic Requirements for Surface Mount Design and Land Pattern Standard (2010) for the small outline no-lead (SON) package is shown in Figure 17.



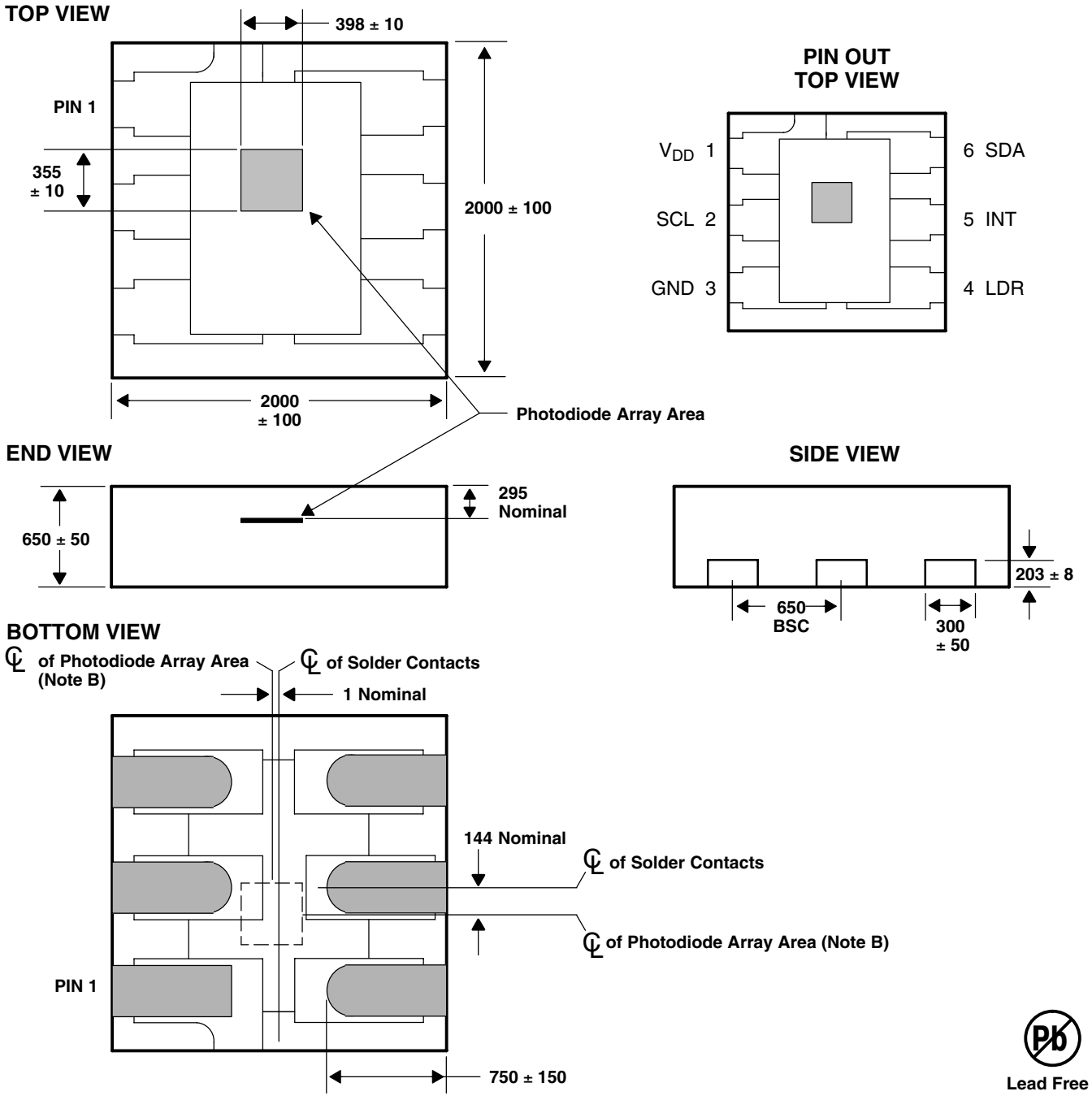
TOP VIEW

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Figure 17. Suggested FN Package PCB Layout

PACKAGE INFORMATION

PACKAGE FN **Dual Flat No-Lead**



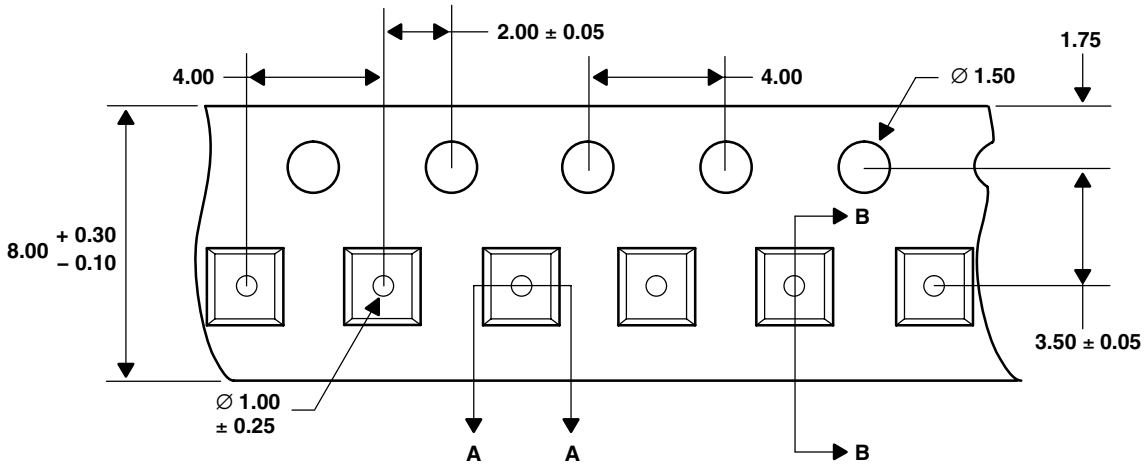
Lead Free

NOTES: A. All linear dimensions are in micrometers.
B. The die is centered within the package within a tolerance of ± 75 µm.
C. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
D. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
E. This package contains no lead (Pb).
F. This drawing is subject to change without notice.

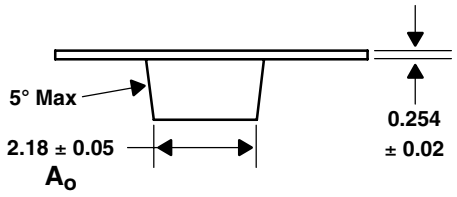
Figure 18. Package FN — Dual Flat No-Lead Packaging Configuration

CARRIER TAPE AND REEL INFORMATION

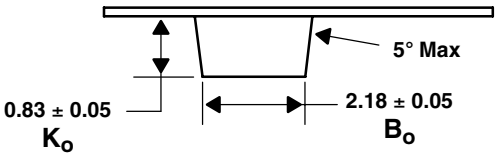
TOP VIEW

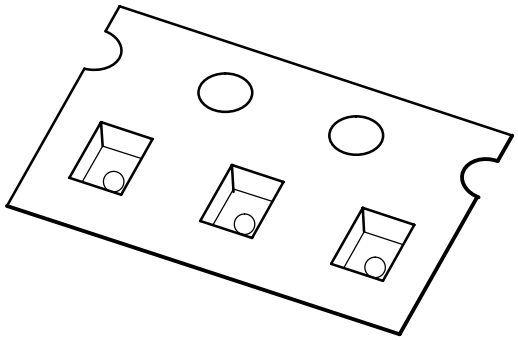


DETAIL A



DETAIL B





NOTES:
A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 178 millimeters in diameter and contains 3500 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
G. This drawing is subject to change without notice.

Figure 19. Package FN Carrier Tape

SOLDERING INFORMATION

The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 17. Solder Reflow Profile

PARAMETER	REFERENCE	DEVICE
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T1)	t_1	Max 60 sec
Time above 230°C (T2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/sec

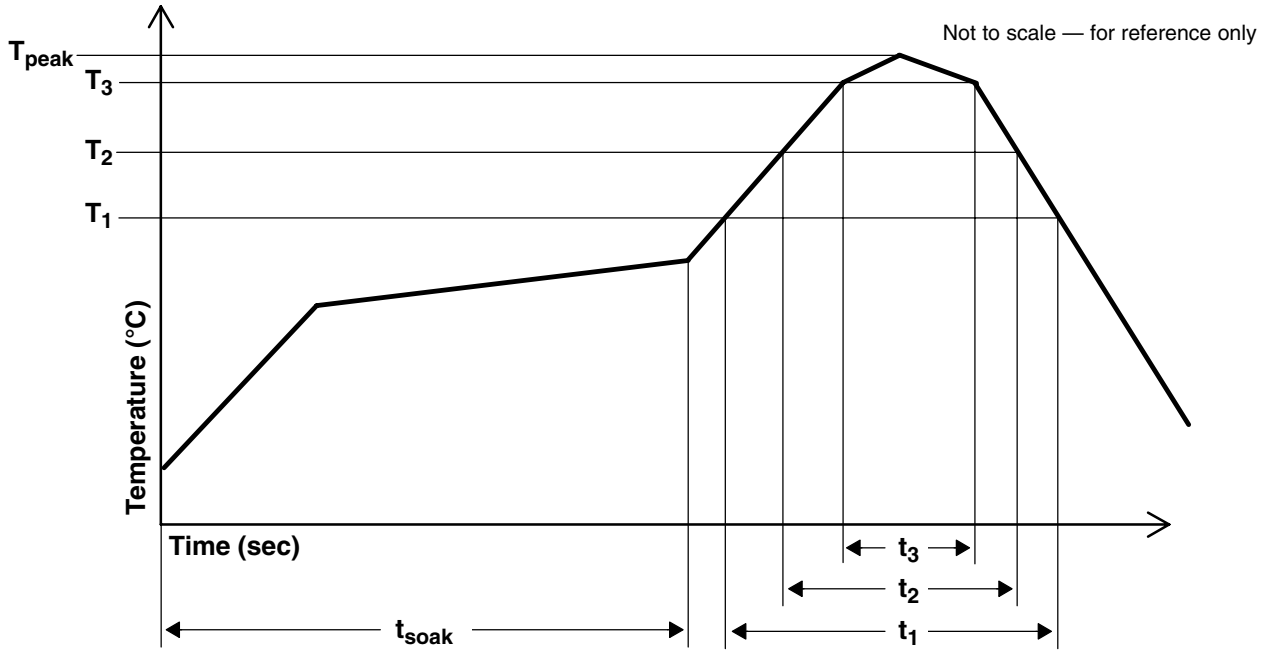


Figure 20. Solder Reflow Profile Graph

STORAGE INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

Shelf Life:	12 months
Ambient Temperature:	< 40°C
Relative Humidity:	< 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The FN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

Floor Life:	168 hours
Ambient Temperature:	< 30°C
Relative Humidity:	< 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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