Filtronic

FPD1500DFN

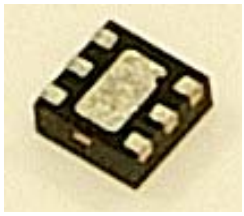
Datasheet v3.0

LOW NOISE HIGH LINEARITY PACKAGED PHEMT

FEATURES (1850MHZ):

- 27 dBm Output Power (P1dB)
- 18 dB Small-Signal Gain (SSG)
- 1.2 dB Noise Figure
- 42 dBm Output IP3
- 45% Power-Added Efficiency
- FPD1500DFN - RoHS compliant

PACKAGE:



RoHS



GENERAL DESCRIPTION:

The FPD1500DFN is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 750 µm Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and input power levels.

TYPICAL APPLICATIONS:

- Drivers or output stages in PCS/Cellular base station transmitter amplifiers
- High intercept-point LNAs
- WLL and WLAN systems, and other types of wireless infrastructure systems.

ELECTRICAL SPECIFICATIONS:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power at 1dB Gain Compression	P1dB	VDS = 5 V; IDS = 50% IDSS	26	27		dBm
Small-Signal Gain	SSG	VDS = 5 V; IDS = 50% IDSS	16.0	18		dB
Power-Added Efficiency	PAE	VDS = 5 V; IDS = 50% IDSS; POUT = P1dB		45		%
Noise Figure	NF	VDS = 5 V; IDS = 50% IDSS		1.2		dB
Output Third-Order Intercept Point (from 15 to 5 dB below P1dB)	IP3	VDS = 5V; IDS = 50% IDSS Matched for optimal power Matched for best IP3		 40 42		dBm
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	375	465	550	mA
Maximum Drain-Source Current	IMAX	VDS = 1.3 V; VGS ≅ +1 V		750		mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		400		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		1	15	µA
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 1.5 mA	0.7	0.9	1.3	V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 1.5 mA	12	16		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 1.5 mA	12	16		V

Note: $T_{AMBIENT}$ = 22°; RF specification measured at f = 1850 MHz using CW signal (except as noted)

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ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < +0V	8V
Gate-Source Voltage	VGS	0V < VDS < +8V	-3V
Drain-Source Current	IDS	For VDS > 2V	IDss
Gate Current	IG	Forward or reverse current	15mA
RF Input Power[2]	PIN	Under any acceptable bias state	350mW
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-55°C to 150°C
Total Power Dissipation	PTOT	See De-Rating Note below	2.2W
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits	

Notes:

[1] $T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device

[2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1

[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously

[4] Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,

where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power

Total Power Dissipation to be de-rated as follows above 22°C:

P_{TOT}= 2.2 - (0.0167W/°C) x T_{PACK}

where T_{PACK}= source tab lead temperature above 22°C

(coefficient of de-rating formula is the Thermal Conductivity)

Example: For a 65°C carrier temperature: P_{TOT} = 2.2W – (0.0167 x (65 – 22)) = 1.48W

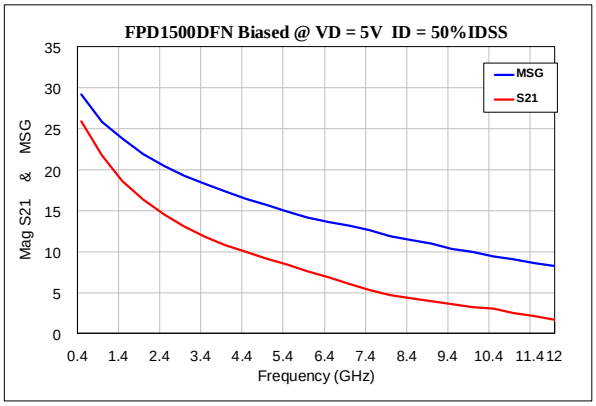
[5] The use of a filled via-hole directly beneath the exposed heatsink tab on the bottom of the package is strongly recommended to provide for adequate thermal management. Ideally the bottom of the circuit board is affixed to a heatsink or thermal radiator

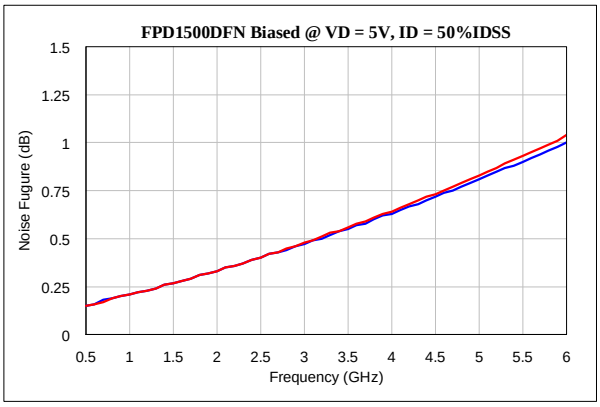
BIASING GUIDELINES:

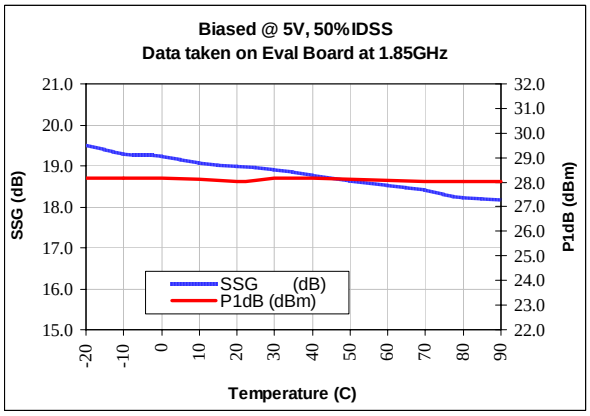
- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.
- For standard Class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are “quasi- E/D mode” devices, exhibit Class AB traits when operated at 50% of IDSS. To achieve a larger separation between P1dB and IP3, an operating point in the 25% to 33% of IDSS range is suggested. Such Class AB operation will not degrade the IP3 performance.

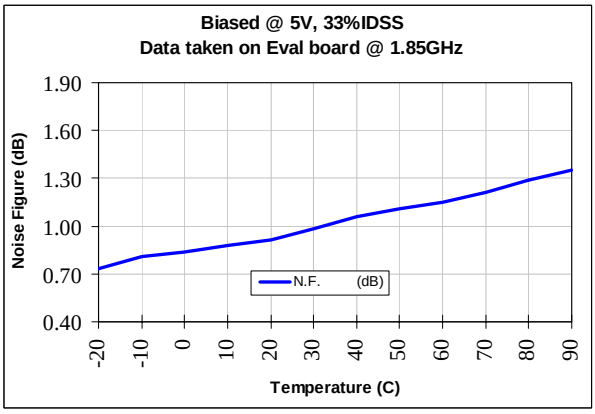
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TYPICAL TUNED RF PERFORMANCE:

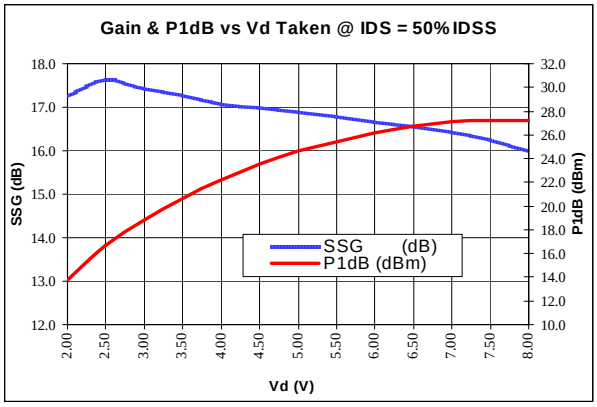


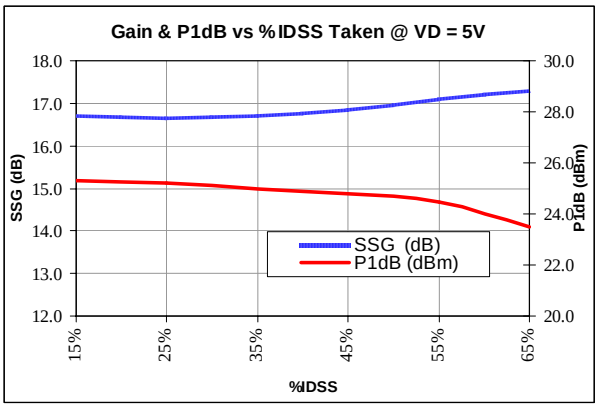






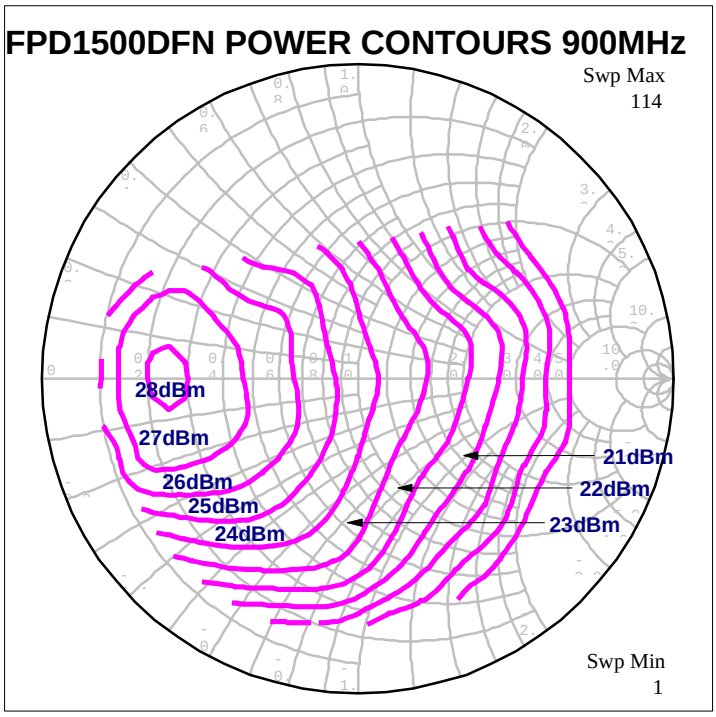
BIAS RESPONSE:

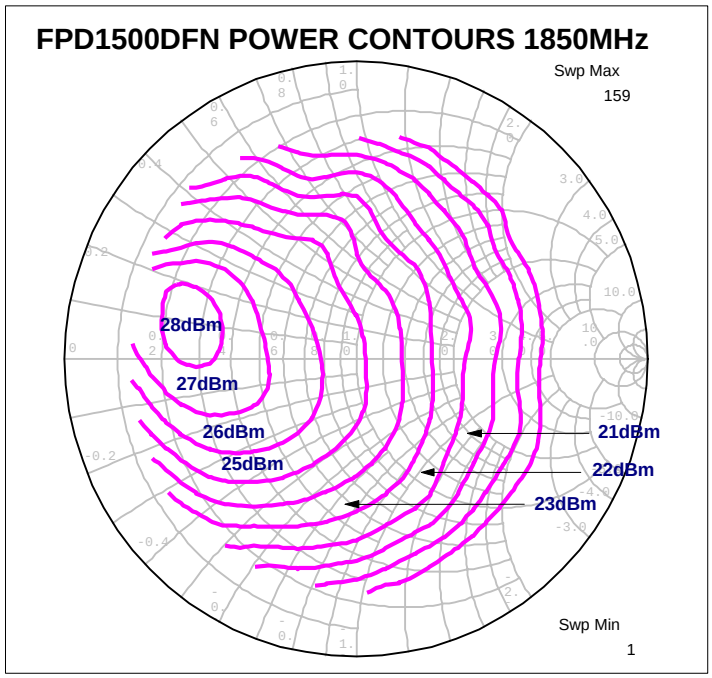




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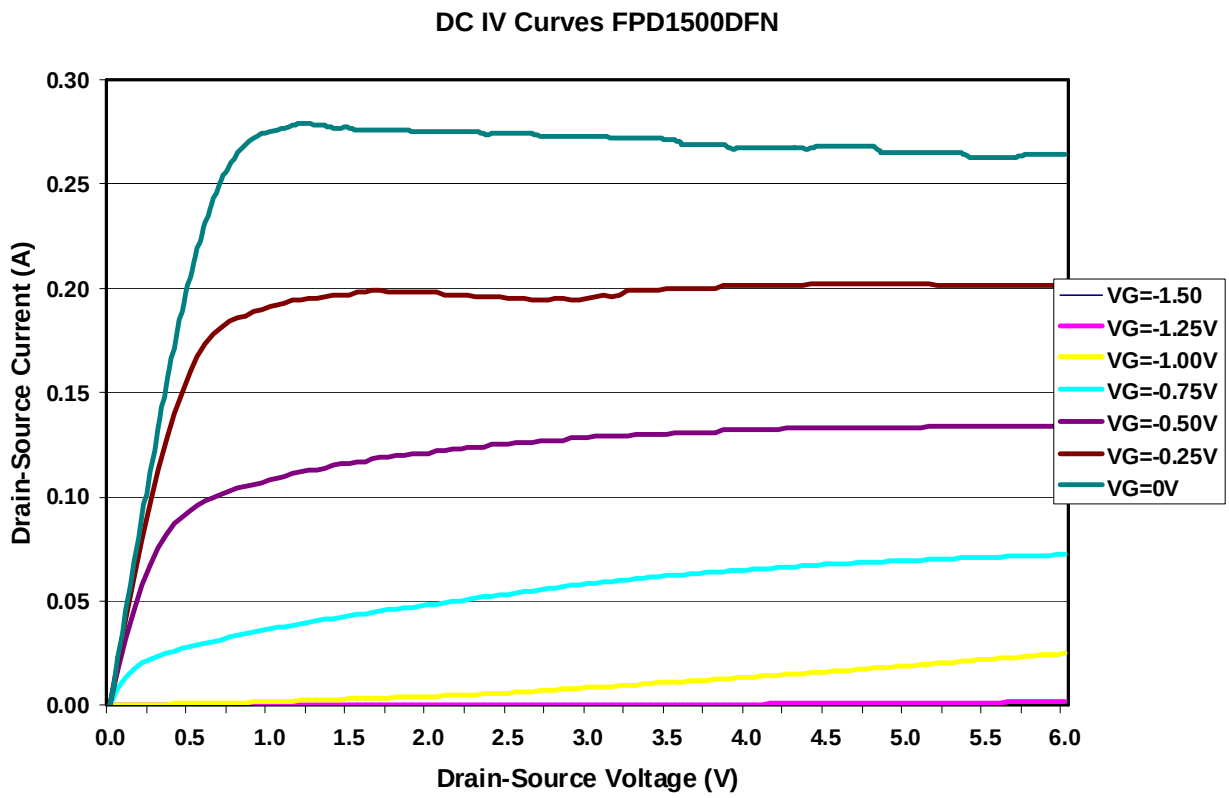
TYPICAL OUTPUT PLANE CONTOURS (VDS = 5V, IDS = 50%IDSS):





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TYPICAL I-V CHARACTERISTICS:



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the V_{DS} > 1.3V will generally cause errors in the current measurements, even in stabilized circuits.

Recommendation: Traditionally a device's I_{DSS} rating (I_{DS} at V_{GS} = 0V) was used as a predictor of RF power, and for MESFETs there is a correlation between I_{DSS} and P_{1dB} (power at 1dB gain compression). For pHEMTs it can be shown that there is *no* meaningful statistical correlation between I_{DSS} and P_{1dB}; specifically a linear regression analysis shows $r^2 < 0.7$, and the regression fails the F-statistic test. I_{DSS} is sometimes useful as a guide to circuit tuning, since the S_{22} does vary with the quiescent operating point I_{DS}.

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NOISE PARAMETERS:

Bias 3V, 50%IDSS

Freq (GHz)	Γopt		Rn/50
	Mag	Angle	
0.900	0.345	18.350	0.029
1.800	0.384	86.350	0.043
2.000	0.401	97.050	0.039
2.200	0.448	116.200	0.032
2.400	0.463	129.200	0.031
2.600	0.483	137.900	0.034
2.800	0.482	146.800	0.022
3.000	0.503	149.850	0.022
3.500	0.487	160.750	0.023
4.000	0.513	172.500	0.020
4.500	0.506	177.500	0.035
5.000	0.521	-172.250	0.027
5.500	0.563	-160.450	0.031
6.000	0.570	-153.650	0.041

Bias 5V, 25%IDSS

Freq (GHz)	Γopt		Rn/50
	Mag	Angle	
0.900	0.367	27.250	0.030
1.800	0.416	75.400	0.046
2.000	0.445	80.800	0.042
2.200	0.454	103.150	0.035
2.400	0.450	125.500	0.034
2.600	0.502	129.550	0.028
2.800	0.467	135.950	0.023
3.000	0.475	142.050	0.023
3.500	0.478	151.550	0.024
4.000	0.495	163.200	0.020
4.500	0.490	168.500	0.034
5.000	0.497	179.700	0.024
5.500	0.544	-168.300	0.023
6.000	0.558	-161.200	0.028

Bias 5V, 50%IDSS

Freq (GHz)	Γopt		Rn/50
	Mag	Angle	
0.900	0.181	73.550	0.038
1.800	0.283	91.250	0.051
2.000	0.346	100.550	0.047
2.200	0.400	119.700	0.038
2.400	0.426	131.450	0.036
2.600	0.450	136.800	0.039
2.800	0.445	148.400	0.028
3.000	0.485	156.550	0.026
3.500	0.470	163.800	0.029
4.000	0.492	175.300	0.026
4.500	0.500	-178.800	0.042
5.000	0.509	-169.350	0.036
5.500	0.554	-158.100	0.042
6.000	0.568	-150.900	0.054

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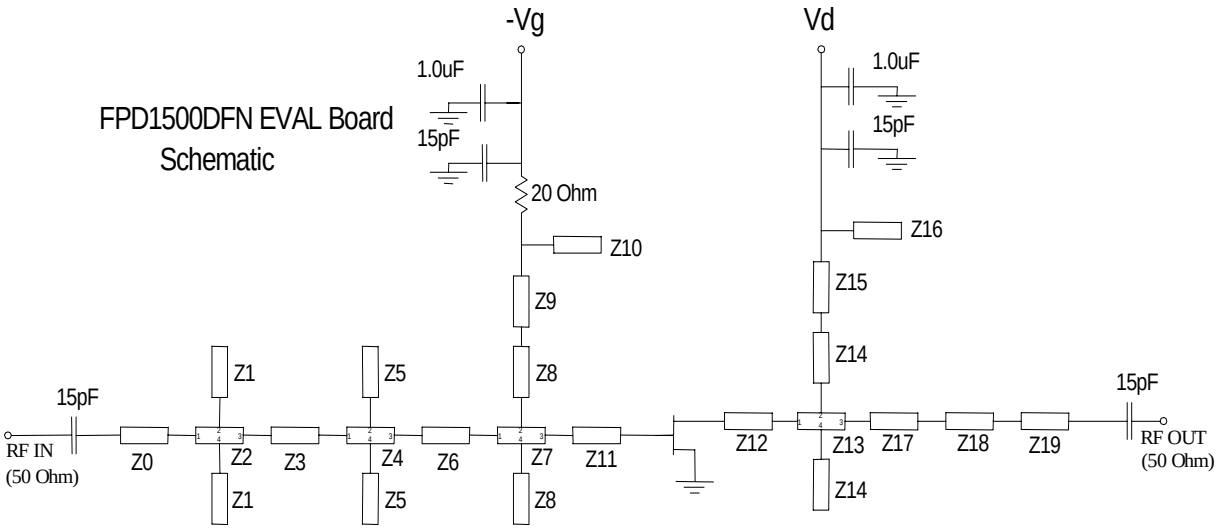
S-PARAMETERS:

Biased @ 5V, 50%IDSS

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.500	0.841	-91.2	19.661	126.2	0.023	51.0	0.294	-137.3
1.000	0.770	-134.6	12.134	102.2	0.031	41.1	0.308	-159.7
1.500	0.770	-157.8	8.561	87.3	0.037	38.0	0.317	-168.0
2.000	0.760	-173.0	6.590	77.3	0.040	35.6	0.324	-175.2
2.500	0.775	176.0	5.303	68.3	0.045	38.0	0.339	179.6
3.000	0.773	168.8	4.514	61.0	0.051	35.7	0.345	173.0
3.500	0.768	163.2	3.898	53.4	0.056	35.0	0.349	166.4
4.000	0.765	158.2	3.471	46.6	0.064	32.2	0.355	159.1
4.500	0.759	152.8	3.160	39.0	0.069	32.4	0.365	154.0
5.000	0.753	145.2	2.878	32.1	0.076	29.2	0.372	148.1
5.500	0.751	138.5	2.625	24.9	0.084	24.8	0.377	145.1
6.000	0.761	131.1	2.407	17.7	0.089	20.4	0.380	140.3
6.500	0.766	124.7	2.204	10.3	0.092	14.8	0.385	135.0
7.000	0.769	118.9	2.018	3.7	0.097	10.3	0.388	129.1
7.500	0.760	113.7	1.845	-2.6	0.100	6.7	0.392	123.8
8.000	0.756	108.6	1.717	-7.8	0.105	6.2	0.396	120.8
8.500	0.759	103.5	1.643	-13.6	0.113	3.1	0.408	117.8
9.000	0.771	97.8	1.573	-19.1	0.121	-1.7	0.418	114.3
9.500	0.768	93.1	1.510	-25.8	0.136	-5.3	0.428	110.0
10.000	0.775	87.6	1.453	-32.5	0.145	-12.3	0.451	104.3
10.500	0.803	82.4	1.419	-39.8	0.155	-17.9	0.465	97.9
11.000	0.800	76.0	1.328	-47.2	0.164	-22.5	0.475	91.1
11.500	0.808	69.5	1.275	-53.2	0.170	-27.9	0.489	86.5
12.000	0.817	63.9	1.208	-59.7	0.177	-32.2	0.502	79.2

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REFERENCE DESIGN (5.3 – 5.9GHZ)

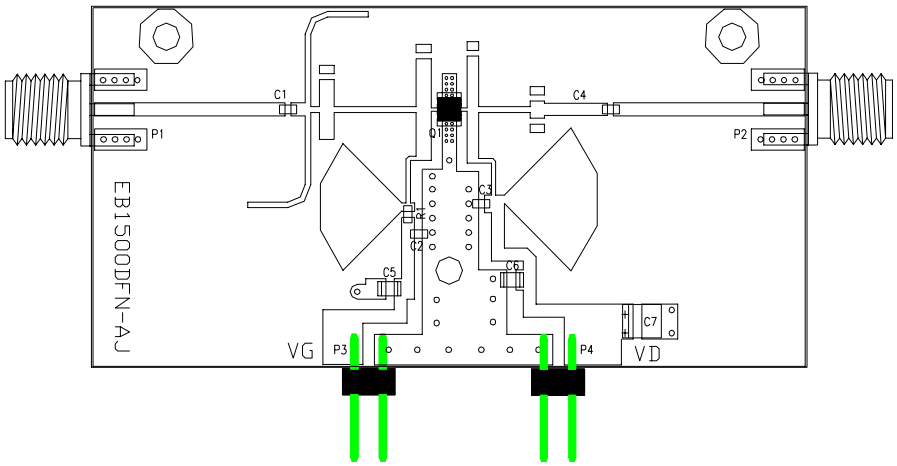


Desc.	Value
Z0	0.045" x 0.050" Microstrip
Z1	0.020" x 0.500" Microstrip
Z2	W1=0.020" W2=0.020" W3=0.020" W4=0.020" Microstrip Cross
Z3	0.020" x 0.030" Microstrip
Z4	W1=0.020" W2=0.052" W3=0.020" W4=0.052" Microstrip Cross
Z5	0.052" x 0.94" Microstrip
Z6	0.020" x 0.285" Microstrip
Z7	W1=0.020" W2=0.054" W3=0.020" W4=0.054" Microstrip Cross
Z8	0.054" x 0.166" Microstrip
Z9	0.015" x 0.166" Microstrip
Z10	0.310" x 90° Microstrip Radial Stub
Z16	0.350" x 90° Microstrip Radial Stub
Z11, Z12	0.012" x 0.037" Microstrip
Z13	W1=0.020" W2=0.040" W3=0.020" W4=0.040" Microstrip Cross
Z14	0.040" x 0.175" Microstrip
Z15	0.015" x 0.157" Microstrip
Z17	0.020" x 0.180" Microstrip
Z18	0.060" x 0.050" Microstrip
Z19	0.042" x 0.220" Microstrip

PARAMETER	UNIT	PERFORMANCE
Frequency	**GHz**	**5.3 to 5.9**
Gain	**dB**	**10.5**
P1dB	**dBm**	**27**
N.F.	**dB**	**1.5**
OIP3	**dBm**	**40**
S11	**dB**	**-10**
S22	**dB**	**-9**
Vd	**V**	**5**
Vg	**V**	**-0.4 to -0.7**
Id	**mA**	**200**

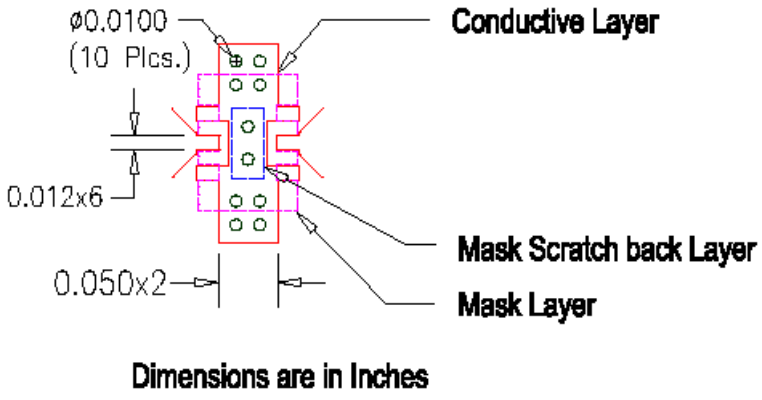
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EVALUATION BOARD (5.3 – 5.9 GHz)



Component	Description
R1	Resistor 0.06 x 0.03 20Ω 1/4W
C1, C2, C3, C4	Cap. 0.06 x 0.03 15pF
C5, C6	Cap. 0.08 x 0.05 0.01uF
C7	Cap. SMD-B 1.0uF
P1, P2	Edge Mount RF Connecter
P3, P4	2 Pin Header
Q1	FPD1500DFN
PCB	EV-SP-000051-002 (R4003, 20mil Thick)
Base Plate	TF-SP-000055-001

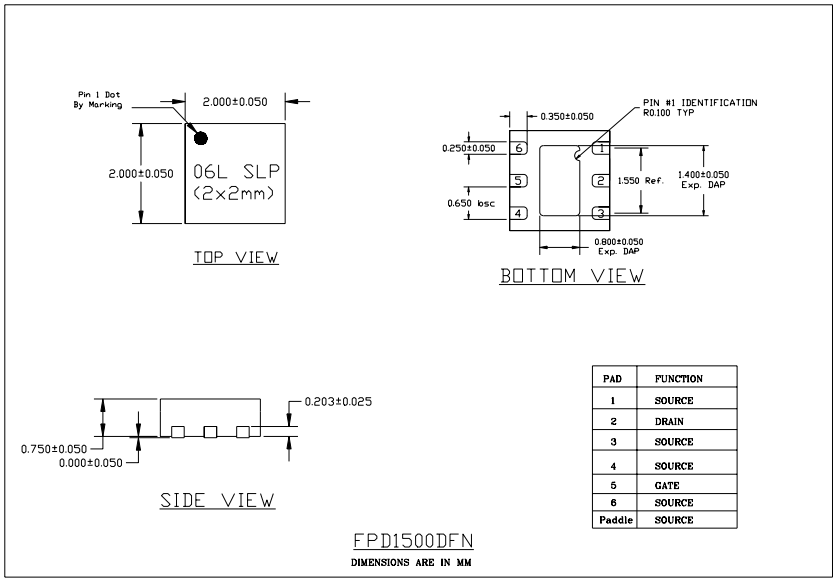
PCB FOOTPRINT:



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PACKAGE OUTLINE:

(dimensions in millimetres – mm)



PAD	FUNCTION
1	SOURCE
2	DRAIN
3	SOURCE
4	SOURCE
5	GATE
6	SOURCE
Paddle	SOURCE

PREFERRED ASSEMBLY INSTRUCTIONS:

Available on request

HANDLING PRECAUTIONS:



To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATION NOTES & DESIGN DATA:

Application Notes and design data including S-parameters are available on request.

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.

ORDERING INFORMATION:

PART NUMBER	DESCRIPTION
FPD1500DFN	Packaged pHEMT
EB1500DFN-BB	Packaged pHEMT eval board – 900MHz
EB1500DFN-BA	Packaged pHEMT eval board – 1.85GHz
EB1500DFN-BC	Packaged pHEMT eval board – 2.0GHz
EB1500DFN-BE	Packaged pHEMT eval board – 2.4GHz
EB1500DFN-AJ	Packaged pHEMT eval board – 5.3 to 5.9GHz

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

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