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March 2015



FDD3682

N-Channel PowerTrench® MOSFET 100V, 32A, 36m Ω

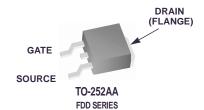
Features

- $r_{DS(ON)} = 32m\Omega$ (Typ.), $V_{GS} = 10V$, $I_D = 32A$
- $Q_q(tot) = 18.5nC (Typ.), V_{GS} = 10V$
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101

Formerly developmental type 82755

Applications

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- · Direct Injection / Diesel Injection System
- 42V Automotive Load Control
- · Electronic Valve Train System





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain to Source Voltage	100	V
V _{GS}	Gate to Source Voltage	±20	V
	Drain Current		
	Continuous ($T_C = 25^{\circ}C$, $V_{GS} = 10V$)	32	А
I_D	Continuous (T _C = 100°C, V _{GS} = 10V)	23	А
	Continuous ($T_{amb} = 25^{\circ}C$, $V_{GS} = 10V$, $R_{\theta JA} = 52^{\circ}C/W$)	5.5	А
	Pulsed	Figure 4	А
E _{AS}	Single Pulse Avalanche Energy (Note 1)	55	mJ
D	Power dissipation	95	W
P_{D}	Derate above 25°C	0.63	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252	1.58	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	52	°C/W

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3682	FDD3682	TO-252AA	330mm	16mm	2500 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units	
Off Characteristics							
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100	-	-	V	
I _{DSS}	Lzero Gate Voltage Drain Gurrent	V _{DS} = 80V	-	-	1		
		$V_{GS} = 0V$ $T_C = 150^{\circ}$	C -	-	250	μΑ	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$	-	-	±100	nA	

On Characteristics

V _{GS(TH)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2	-	4	V
r _{DS(ON)}	Drain to Source On Resistance	$I_D = 32A, V_{GS} = 10V$	-	0.032	0.036	Ω
		I _D = 16A, V _{GS} = 6V	-	0.040	0.060	
		$I_D = 32A, V_{GS} = 10V,$ $T_C = 175^{\circ}C$	-	0.080	0.090	

Dynamic Characteristics

C _{ISS}	Input Capacitance	V 05V V	0)./	-	1250	-	pF
C _{OSS}	Output Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$, $f = 1MHz$		-	190	-	pF
C _{RSS}	Reverse Transfer Capacitance			-	45	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V$		-	18.5	28	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 2V$ $V_{DD} = 50V$	-	2.4	3.6	nC	
	Gate to Source Gate Charge		$I_{D} = 32A$	-	6.5	-	nC
Q _{gs} Q _{gs2}	Gate Charge Threshold to Plateau		$I_g = 1.0 \text{mA}$	-	4.1	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	4.6	-	nC

Resistive Switching Characteristics $(V_{GS} = 10V)$

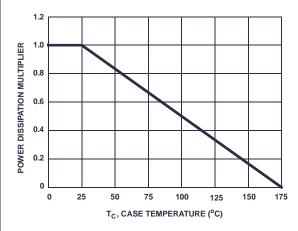
t _{ON}	Turn-On Time		-	-	83	ns
t _{d(ON)}	Turn-On Delay Time	$V_{DD} = 50V, I_{D} = 32A$ $V_{GS} = 10V, R_{GS} = 16\Omega$	-	9	-	ns
t _r	Rise Time		-	46	-	ns
t _{d(OFF)}	Turn-Off Delay Time		-	24	-	ns
t _f	Fall Time		-	26	-	ns
t _{OFF}	Turn-Off Time		-	-	75	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 32A$	ı	-	1.25	V
		I _{SD} = 16A	-	-	1.0	V
t _{rr}	Reverse Recovery Time	$I_{SD} = 32A$, $dI_{SD}/dt = 100A/\mu s$	-	-	55	ns
Q_{RR}	Reverse Recovery Charge	$I_{SD} = 32A$, $dI_{SD}/dt = 100A/\mu s$	-	-	92	nC

Notes: 1: Starting $T_J = 25^{\circ}C$, L = 0.27mH, $I_{AS} = 20A$.





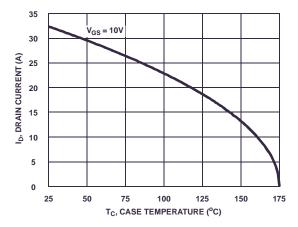


Figure 1. Normalized Power Dissipation vs Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

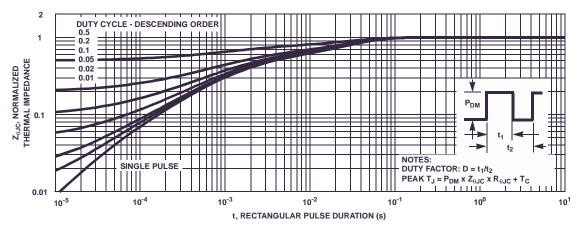


Figure 3. Normalized Maximum Transient Thermal Impedance

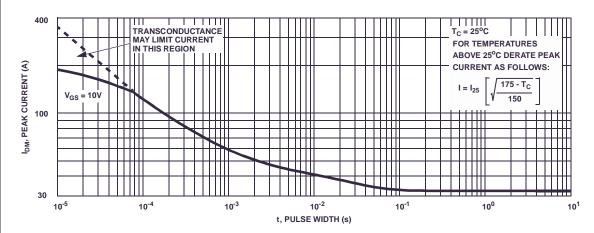
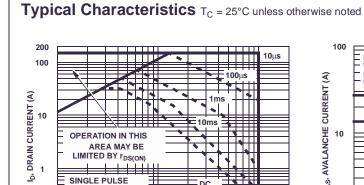


Figure 4. Peak Current Capability

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 $T_J = MAX RATED$ $T_C = 25$ °C

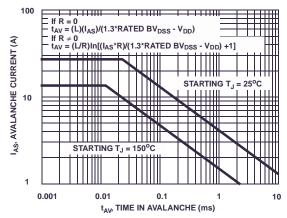


Figure 5. Forward Bias Safe Operating Area

V_{DS}, DRAIN TO SOURCE VOLTAGE (V)

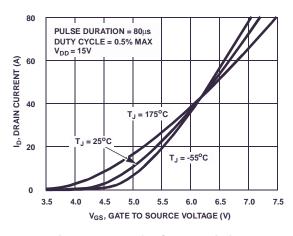
200

100

NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability



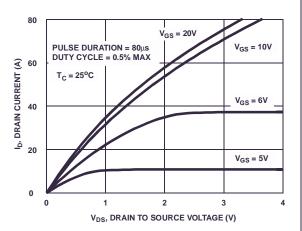
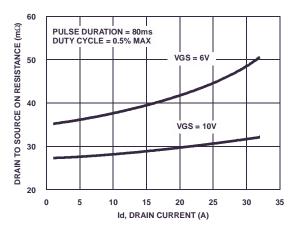


Figure 7. Transfer Characteristics

Figure 8. Saturation Characteristics



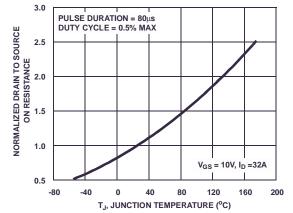


Figure 9. Drain to Source On Resistance vs Drain Current

Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

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Typical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

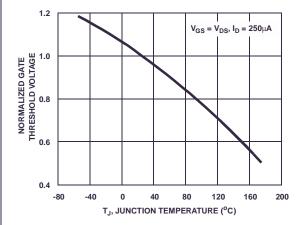


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

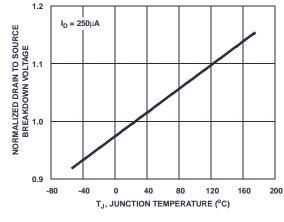


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

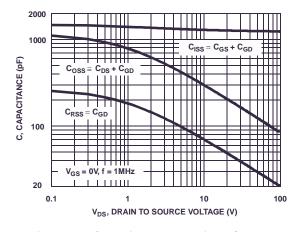


Figure 13. Capacitance vs Drain to Source Voltage

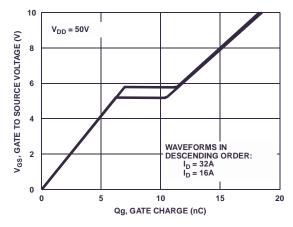
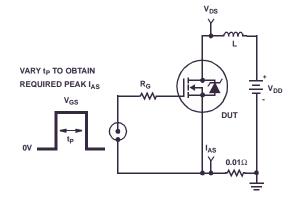


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms



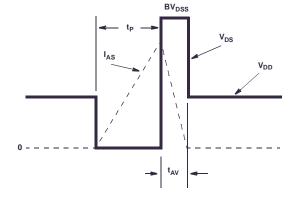


Figure 15. Unclamped Energy Test Circuit

Figure 16. Unclamped Energy Waveforms

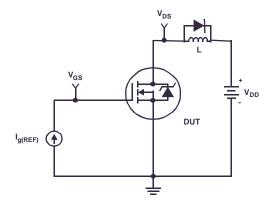


Figure 17. Gate Charge Test Circuit

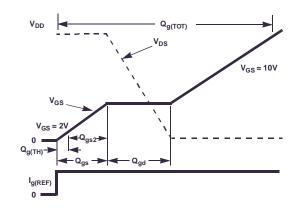


Figure 18. Gate Charge Waveforms

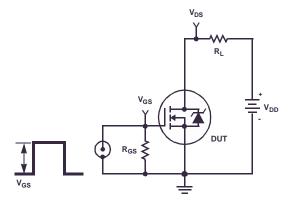


Figure 19. Switching Time Test Circuit

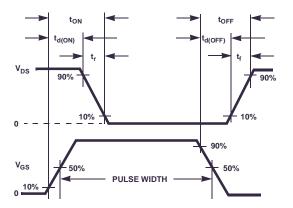


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \tag{EQ. 1}$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeter square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\Theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)}$$
 (EQ. 2)

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)}$$
 (EQ. 3)

Area in Centimeters Squared

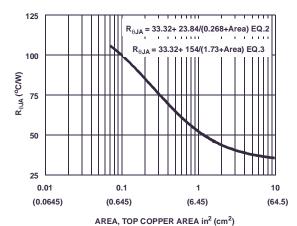


Figure 21. Thermal Resistance vs Mounting
Pad Area

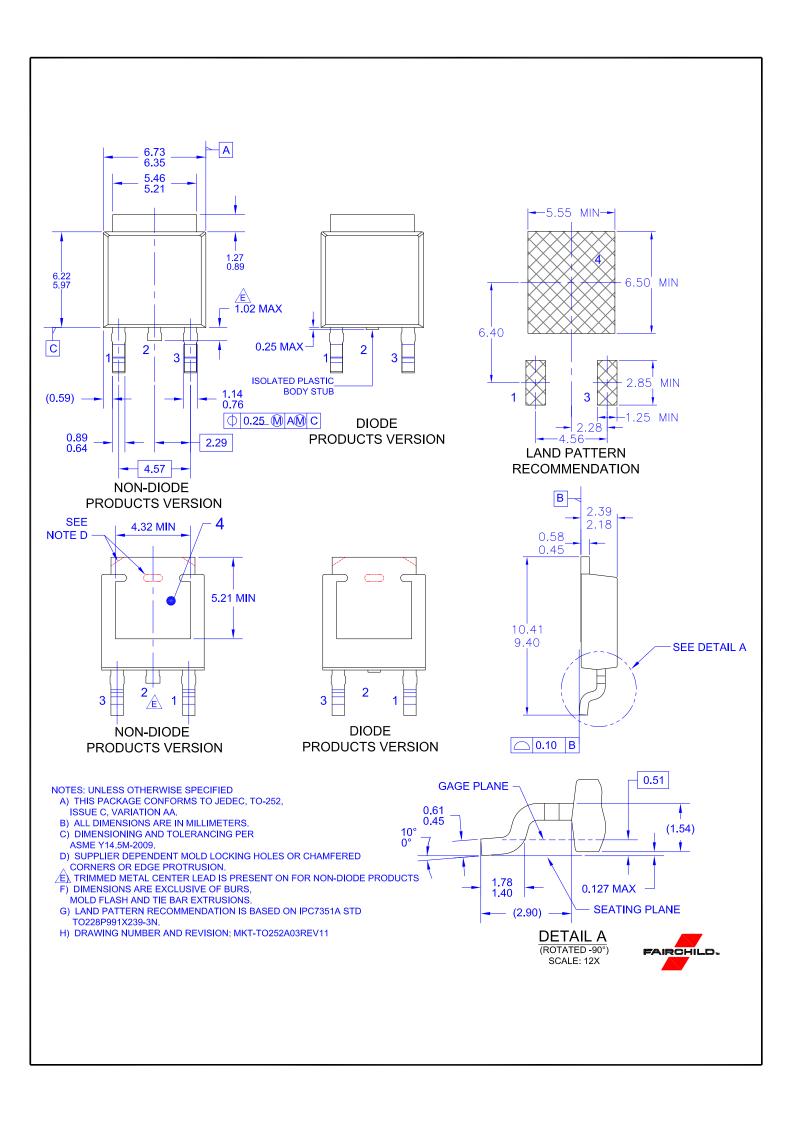
```
PSPICE Electrical Model
.SUBCKT FDD3682 2 1 3 ;
                           rev Jun 2002
Ca 12 8 4e-10
Cb 15 14 6e-10
                                                                                                   LDRAIN
Cin 6 8 1.22e-9
                                                             DPLCAP
                                                                                                           DRAIN
Dbody 7 5 DbodyMOD
                                                                                                  RLDRAIN
Dbreak 5 11 DbreakMOD
                                                                      €RSLC1
                                                                                   DBREAK 
Dplcap 10 5 DplcapMOD
                                                            RSLC2<sup>₹</sup>
                                                                          ESLC
Ebreak 11 7 17 18 112
                                                                                          11
Eds 14 8 5 8 1
                                                                        50
Egs 13 8 6 8 1
                                                                      ≨RDRAIN
                                                                                          17
                                                                                               DBODY
Esg 6 10 6 8 1
                                                    ESG
                                                                                  FRRFAK
Evthres 6 21 19 8 1
                                                              EVTHRES
Evtemp 20 6 18 22 1
                                                                (19)
8
                                                                                    MWEAK
                                    LGATE
                                                  EVTEMP
                                            RGATE
                                                    18
22
It 8 17 1
                                                                           ←MMED
                                          I<sub>9</sub>
                                                 20
                                                                  MSTRC
                                    RLGATE
Lgate 1 9 4.88e-9
                                                                                                  LSOURCE
Ldrain 2 5 1.0e-9
                                                                   CIN
                                                                                                           SOURCE
Lsource 3 7 2.24e-9
                                                                                    RSOURCE
                                                                                                 RLSOURCE
RLgate 1 9 48.8
RLdrain 2 5 10
                                                                                       RBREAK
                                                           14
13
                                                      <u>13</u>
8
RLsource 3 7 22.4
                                                                                    17
                                                                                                RVTEMP
                                                   S1B
                                                            o S2B
Mmed 16 6 8 8 MmedMOD
                                                         13
                                                                  СВ
                                                                                                19
Mstro 16 6 8 8 MstroMOD
                                              CA
                                                                                   IT
Mweak 16 21 8 8 MweakMOD
                                                                                                  VBAT
                                                                     <u>5</u>
                                                      EGS
Rbreak 17 18 RbreakMOD 1
                                                                                 8
Rdrain 50 16 Rdrain MOD 10.5e-3
Rgate 9 20 1.8
                                                                                       RVTHRES
RSLC1 5 51 RSLCMOD 1.0e-6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 11.9e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD
Vbat 22 19 DC 1
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*70),2.5))}
.MODEL DbodyMOD D (IS=2.4E-12 RS=4.4e-3 TRS1=2.0e-3 TRS2=4.5e-7
+ CJO=9e-10 M=0.58 TT=2.9e-8 XTI=4.0)
.MODEL DbreakMOD D (RS=0.6 TRS1=1.4e-3 TRS2=-5.0e-5)
.MODEL DplcapMOD D (CJO=2.75e-10 IS=1.0e-30 N=10 M=0.56)
.MODEL MstroMOD NMOS (VTO=4.16 KP=32 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MmedMOD NMOS (VTO=3.48 KP=2.7 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.8)
.MODEL MweakMOD NMOS (VTO=2.96 KP=0.068 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=18 RS=0.1)
.MODEL RbreakMOD RES (TC1=1.1e-3 TC2=-1.1e-8)
.MODEL RdrainMOD RES (TC1=1.5e-2 TC2=4e-5)
.MODEL RSLCMOD RES (TC1=3.0e-3 TC2=2.9e-6)
.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-3.9e-3 TC2=-1.4e-5)
.MODEL RytempMOD RES (TC1=-3.5e-3 TC2=1.3e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-2.0)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=-5.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.4 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.4)
FNDS
Note: For further discussion of the PSPICE model, consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global
Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank
Wheatley.
```

SABER Electrical Model REV Jun 2002 template FDD3682 n2,n1,n3 electrical n2,n1,n3 var i iscl dp..model dbodymod = (isl=2.4e-12,rs=4.4e-3,trs1=2.0e-3,trs2=4.5e-7,cjo=9e-10,m=0.58,tt=2.9e-8,xti=4.0) dp..model dbreakmod = (rs=0.6.trs1=1.4e-3.trs2=-5e-5)dp..model dplcapmod = (cjo=2.7e-10,isl=10e-30,nl=10,m=0.56) m..model mstrongmod = (type=_n,vto=4.16,kp=32,is=1e-30, tox=1) m..model mmedmod = $(type=_n, vto=3.48, kp=2.7, is=1e-30, tox=1)$ m..model mweakmod = (type=_n,vto=2.96,kp=0.068,is=1e-30, tox=1,rs=0.1) sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-5,voff=-2) I DRAIN sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2,voff=-5) DRAIN sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.4,voff=0.3) 10 sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.3,voff=-0.4) RLDRAIN c.ca n12 n8 = 4e-10ERSLC1 c.cb n15 n14 = 6e-10RSLC2 ₹ c.cin n6 n8 = 1.22e-9ISCI dp.dbody n7 n5 = model=dbodymod DBREAK 3 dp.dbreak n5 n11 = model=dbreakmod RDRAIN <u>6</u> dp.dplcap n10 n5 = model=dplcapmod FSG (11 DBODY **EVTHRES** spe.ebreak n11 n7 n17 n18 = 112 19 **MWEAK** I GATE **EVTEMP** spe.eds n14 n8 n5 n8 = 1 RGATE spe.egs n13 n8 n6 n8 = 1 EBREAK **←**MMED 20 spe.esg n6 n10 n6 n8 = 1 MSTRO RLGATE spe.evthres n6 n21 n19 n8 = 1 LSOURCE CIN spe.evtemp n20 n6 n18 n22 = 1 SOURCE RSOURCE i.it n8 n17 = 1RLSOURCE I.lgate n1 n9 = 4.88e-9RBREAK I.ldrain n2 n5 = 1.0e-917 I.lsource n3 n7 = 2.24e-9**₹**RVTEMP o S2B 13 19 res.rlgate n1 n9 = 48.8 CA IT res.rldrain n2 n5 = 10 **VBAT** res.rlsource n3 n7 = 22.4 EGS **EDS** m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u **RVTHRES** m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u res.rbreak n17 n18 = 1, tc1=1.1e-3,tc2=-1.1e-8 res.rdrain n50 n16 = 10.5e-3, tc1=1.5e-2,tc2=4e-5 res.rgate n9 n20 = 1.8 res.rslc1 n5 n51 = 1.0e-6, tc1=3.0e-3,tc2=2.9e-6 res.rslc2 n5 n50 = 1.0e3res.rsource n8 n7 = 11.9e-3, tc1=1e-3,tc2=1e-6 res.rvthres n22 n8 = 1, tc1=-3.9e-3, tc2=-1.4e-5res.rvtemp n18 n19 = 1, tc1=-3.5e-3,tc2=1.3e-6 sw vcsp.s1a n6 n12 n13 n8 = model=s1amod sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod v.vbat n22 n19 = dc=1 equations { i (n51->n50) +=iscl

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|sc| = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/70))** 2.5))

SPICE Thermal Model JUNCTION REV 20 Jun 2002 FDD3682_JC TH TL CTHERM1 TH 6 1.6e-3 CTHERM2 6 5 4.5e-3 CTHERM3 5 4 5.0e-3 RTHERM1 CTHERM1 CTHERM4 4 3 8.0e-3 CTHERM5 3 2 8.2e-3 CTHERM6 2 TL 4.7e-2 6 RTHERM1 TH 6 3.3e-2 RTHERM2 6 5 7.9e-2 RTHERM3 5 4 9.5e-2 RTHERM2 CTHERM2 RTHERM4 4 3 1.4e-1 RTHERM5 3 2 2.9e-1 RTHERM6 2 TL 6.7e-1 5 SABER Thermal Model SABER thermal model FDD3682 RTHERM3 CTHERM3 template thermal_model th tl thermal_c th, tl ctherm.ctherm1 th 6 = 1.6e-3 4 ctherm.ctherm2 6 5 =4.5e-3 ctherm.ctherm3 5 4 =5.0e-3 ctherm.ctherm4 4 3 =8.0e-3 ctherm.ctherm5 3 2 =8.2e-3 RTHERM4 CTHERM4 ctherm.ctherm6 2 tl =4.7e-2 rtherm.rtherm1 th 6 =3.3e-2 rtherm.rtherm2 6 5 = 7.9e-2 3 rtherm.rtherm3 5 4 = 9.5e-2 rtherm.rtherm4 4 3 =1.4e-1 rtherm.rtherm5 3 2 =2.9e-1 CTHERM5 RTHERM5 rtherm.rtherm6 2 tl =6.7e-1 2 RTHERM6 CTHERM6 CASE tl



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105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

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Skype отдела продаж:

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