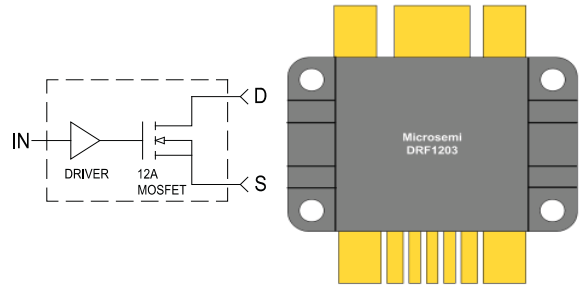



## MOSFET Driver Hybrid

The DRF1203 hybrid includes a high power gate driver and the power MOSFET. The driver output can be configured as Inverting and Non-Inverting. It was designed to provide the system designer increased flexibility and lowered cost over a non-integrated solution.



### FEATURES

- Switching Frequency: DC TO 30MHz
- Low Pulse Width Distortion
- Single Power Supply
- 1V CMOS Schmitt Trigger Input 1V Hysteresis
- Inverting Non-Inverting Select
- RoHS Compliant 
- Switching Speed 3-4ns
- $B_{V_{ds}} = 1Kv$
- $I_{ds} = 12A$  avg.
- $R_{ds(on)} \leq .90$  Ohm
- $P_D = 560W$

### TYPICAL APPLICATIONS

- Class C, D and E RF Generators
- Switch Mode Power Amplifiers
- Pulse Generators
- Ultrasound Transducer Drivers
- Acoustic Optical Modulators

### Driver Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
$V_{DD}$	Supply Voltage	15	V
IN, FN	Input Single Voltages	-.7 to +5.5	
$I_{O\text{PK}}$	Output Current Peak	8	A
$T_{JMAX}$	Operating and Storage Temperature	175	°C

### Driver Specifications

Symbol	Parameter	Min	Typ	Max	Unit
$V_{DD}$	Supply Voltage	10		15	V
IN	Input Voltage	3		5.5	
$IN_{(R)}$	Input Voltage Rising Edge		3		ns
$IN_{(F)}$	Input Voltage Falling Edge		3		
$I_{DDQ}$	Quiescent Current		2		mA
$I_O$	Output Current		8		A
$C_{ISS}$	Input Capacitance		3		
$R_{IN}$	Input Parallel Resistance		1		MΩ
$V_{T(ON)}$	Input, Low to High Out (See Truth Table)	0.8		1.1	V
$V_{T(OFF)}$	Input, High to Low Out (See Truth Table)	1.9		2.2	
$T_{DLY}$	Time Delay (throughput)		38		ns
$t_r$	Rise Time		5		ns
$t_f$	Fall Time		5		
$T_D$	Prop. Delay		35		

## Driver Output Characteristics

DRF1203

Symbol	Parameter	Min	Typ	Max	Unit
$C_{out}$	Output Capacitance		2500		pF
$R_{out}$	Output Resistance		.8		$\Omega$
$L_{out}$	Output Inductance		3		nH
$F_{MAX}$	Operating Frequency CL = 3000nF + 50 $\Omega$	30			MHz
$F_{MAX}$	Operating Frequency RL = 50 $\Omega$	50			

## Driver Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.5		$^{\circ}\text{C}/\text{W}$
$R_{\theta JHS}$	Thermal Resistance Junction to Heat Sink		2.5		
$T_{JSTG}$	Storage Temperature		-55 to 150		$^{\circ}\text{C}$
$P_{DJHS}$	Maximum Power Dissipation @ $T_{SINK} = 25^{\circ}\text{C}$		60		W
$P_{DJC}$	Total Power Dissipation @ $T_C = 25^{\circ}\text{C}$		100		

## MOSFET Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
$BV_{DSS}$	Drain Source Voltage	1000			V
$I_D$	Continuous Drain Current $T_{HS} = 25^{\circ}\text{C}$			12	A
$R_{DS(on)}$	Drain-Source On State Resistance		0.90		$\Omega$
$T_{jmax}$	Operating Temperature			175	$^{\circ}\text{C}$

## MOSFET Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$C_{iss}$	Input Capacitance		2000		pF
$C_{oss}$	Output Capacitance		165		
$C_{rss}$	Reverse Transfer Capacitance		75		

## MOSFET Thermal Characteristics

Symbol	Parameter	Min	Type	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case		0.53		$^{\circ}\text{C}/\text{W}$
$R_{\theta JHS}$	Thermal Resistance Junction to Heat Sink		0.141		
$T_{JSTG}$	Storage Temperature		-55 to 150		$^{\circ}\text{C}$
$P_{DHS}$	Maximum Power Dissipation @ $T_{SINK} = 25^{\circ}\text{C}$		1060		W
$P_{DC}$	Total Power Dissipation @ $T_C = 25^{\circ}\text{C}$		2830		

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

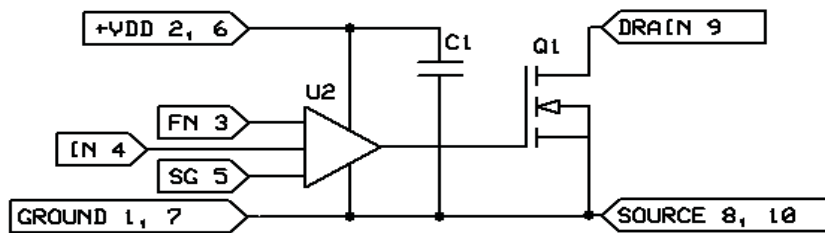


Figure 1, DRF1203 Simplified Circuit Diagram

The Simplified DRF1203 Circuit Diagram is illustrated above. By including the driver high speed by-pass capacitor (C1), their contribution to the internal parasitic loop inductance of the driver output is greatly reduced. This, coupled with the tight geometry of the hybrid, allows optimal gate drive to the MOSFET. This low parasitic approach, coupled with the Schmitt trigger input (IN), Kelvin signal ground (SG) and the Anti-Ring Function, provide improved stability and control in Kilowatt to Multi-Kilowatt, high Frequency applications. The IN pin is the input for the control signal and is applied to a Schmitt Trigger. Both the FN and IN pins are referenced to the Kelvin ground (SG.) The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for the ring abatement. The power drivers provide high current to the gate of the MOSFETS.

The Function (FN, pin 3) is the invert or non-invert select Pin, it is Internally held high.

Truth Table *Referenced to SG		
FN (pin 3)*	IN (pin 4)*	MOSFET
HIGH	HIGH	ON
HIGH	LOW	OFF
LOW	HIGH	OFF
LOW	LOW	ON

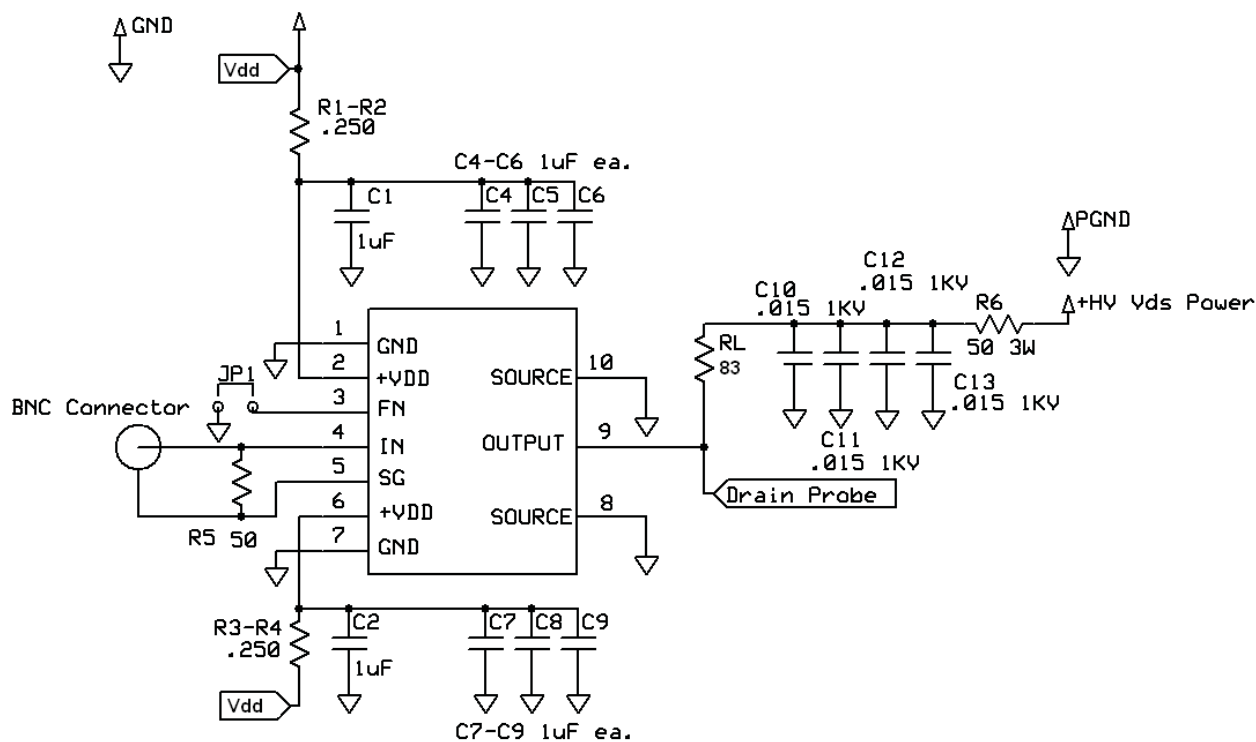
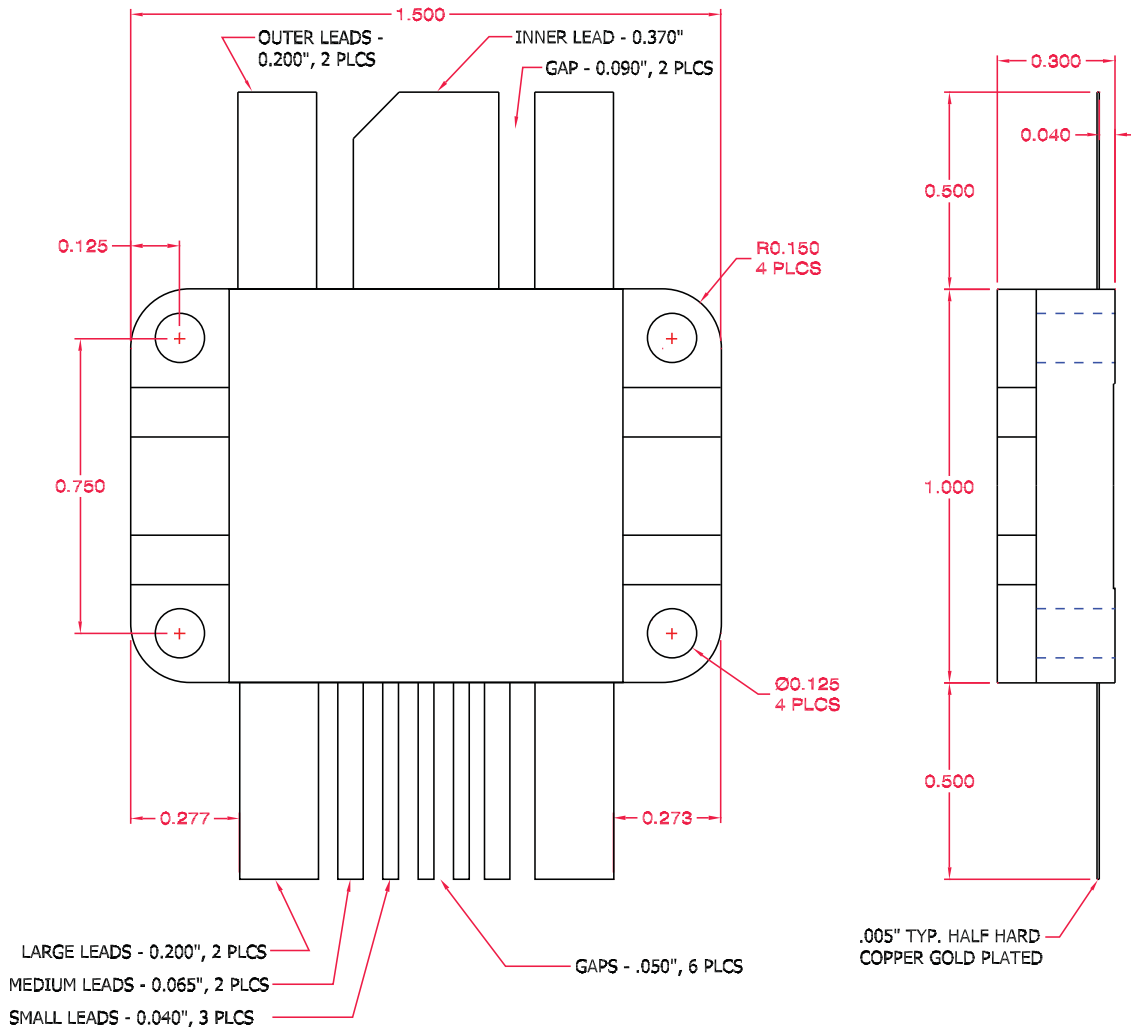


Figure 2, DRF1203 Test Circuit

The Test Circuit illustrated above was used to evaluate the DRF1203 (available as an evaluation Board DRF12XX / EVALSW.) The input control signal is applied to the DRF1203 via IN(4) and SG(5) pins using RG188. This provides excellent noise immunity and control of the signal ground currents.

The  $+V_{DD}$  inputs (2,6) are by-passed (C1,C2, C4-C9), this is in addition to the internal by-passing mentioned previously. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load.  $R_L$  set for  $I_{DM}$  at  $V_{DS}$  max this load is used to evaluate the output performance of the DRF1203.

Pin Assignments	
Pin 1	Ground
Pin 2	+Vdd
Pin 3	FN
Pin 4	IN
Pin 5	SG
Pin 6	+Vdd
Pin 7	Ground
Pin 8	Source
Pin 9	Drain
Pin 10	Source



All dimensions are ± .005

Figure 3, DRF1203 Mechanical Outline

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9