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# FDH44N50

## N-Channel SMPS Power MOSFET

### 500 V, 44 A, 120 mΩ

#### Features

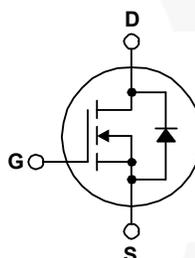
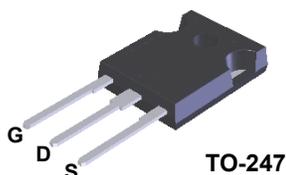
- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement (Typ. 90 nC)
- Improved Gate, Avalanche and High Reapplied dv/dt Ruggedness
- Reduced  $R_{DS(on)}$  (110 mΩ (Typ.) @  $V_{GS} = 10$  V,  $I_D = 22$  A)
- Reduced Miller Capacitance and Low Input Capacitance (Typ.  $C_{rss} = 40$  pF)
- Improved Switching Speed with Low EMI
- 175°C Rated Junction Temperature

#### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

#### Applications

- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDH44N50	Unit
$V_{DSS}$	Drain to Source Voltage	500	V
$V_{GS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current		
	Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10$ V)	44	A
	Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10$ V)	32	A
	Pulsed <sup>1</sup>	176	A
$P_D$	Power Dissipation	750	W
	Derate Above $25^\circ\text{C}$	5	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
	Soldering Temperature for 10 Seconds	300 (1.6mm from case)	$^\circ\text{C}$
	Mounting Torque, 8-32 or M3 Screw	10lbf*in (1.1N*m)	

#### Thermal Characteristics

Symbol	Parameter	FDH44N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDH44N50	FDH44N50	TO-247	Tube	N/A	N/A	30 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Statics</b>						
$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	500	-	-	V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temp. Coefficient	Reference to $25^\circ\text{C}$ , $I_D = 1\ \text{mA}$	-	0.61	-	$\text{V}/^\circ\text{C}$
$r_{DS(ON)}$	Drain to Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 22\ \text{A}$	-	0.11	0.12	$\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	3.15	4	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\ \text{V}$	-	-	25	$\mu\text{A}$
		$V_{GS} = 0\ \text{V}$	-	-	250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$	-	-	$\pm 100$	nA

## Dynamics

$g_{fs}$	Forward Transconductance	$V_{DS} = 50\ \text{V}, I_D = 22\ \text{A}$	11	-	-	S
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 10\ \text{V}$	-	90	108	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DS} = 400\ \text{V}$	-	24	29	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$I_D = 44\ \text{A}$	-	31	37	nC
$t_{d(ON)}$	Turn-On Delay Time	$V_{DD} = 250\ \text{V}$ , $I_D = 44\ \text{A}$ , $R_G = 2.15\ \Omega$ , $R_D = 5.68\ \Omega$	-	16	-	ns
$t_r$	Rise Time		-	84	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	45	-	ns
$t_f$	Fall Time		-	79	-	ns
$C_{ISS}$	Input Capacitance		$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	-	5335	-
$C_{OSS}$	Output Capacitance		-	645	-	pF
$C_{RSS}$	Reverse Transfer Capacitance		-	40	-	pF

## Avalanche Characteristics

$E_{AS}$	Single Pulse Avalanche Energy <sup>2</sup>		1500	-	-	mJ
$I_{AR}$	Avalanche Current		-	-	44	A

## Drain-Source Diode Characteristics

$I_S$	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode.	-	-	44	A
$I_{SM}$	Pulsed Source Current <sup>1</sup> (Body Diode)		-	-	176	A
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 44\ \text{A}$	-	0.900	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 44\ \text{A}, dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$	-	920	1100	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 44\ \text{A}, dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$	-	14	18	$\mu\text{C}$

### Notes:

- 1: Repetitive rating; pulse-width limited by maximum junction temperature.
- 2: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.61\ \text{mH}$ ,  $I_{AS} = 44\ \text{A}$

## Typical Characteristics

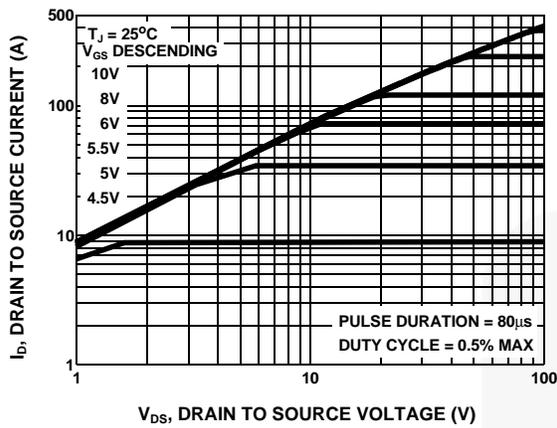


Figure 1. Output Characteristics

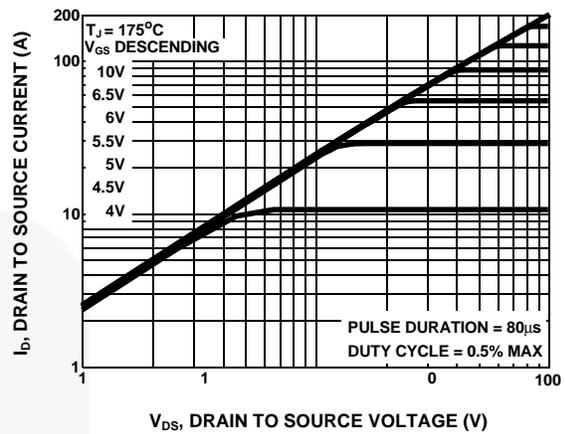


Figure 2. Output Characteristics

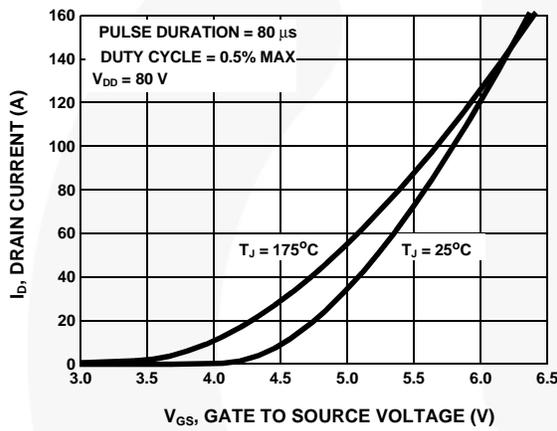


Figure 3. Transfer Characteristics

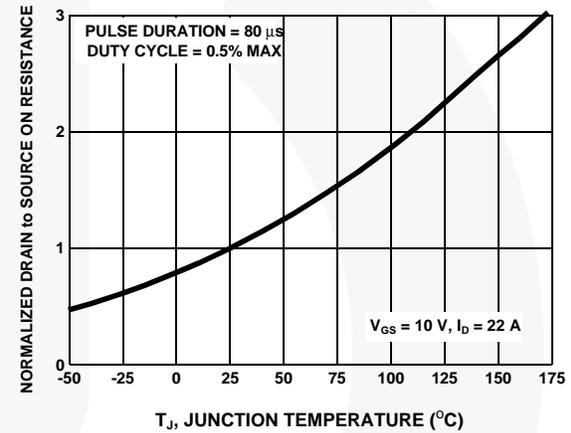


Figure 4. Normalized Drain To Source On Resistance vs Junction Temperature

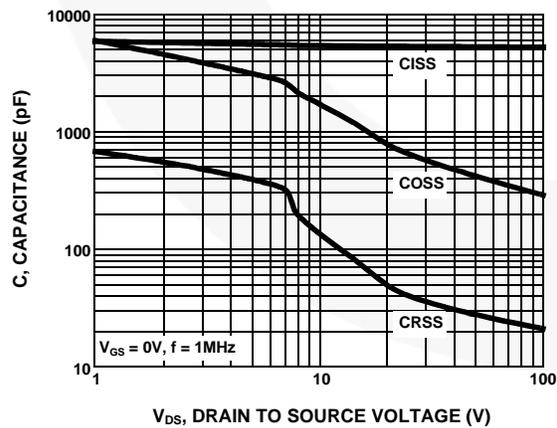


Figure 5. Capacitance vs Drain To Source Voltage

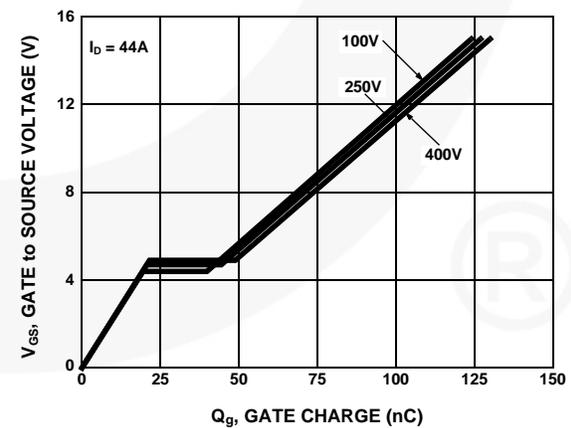


Figure 6. Gate Charge Waveforms For Constant Gate Current

Typical Characteristics (Continued)

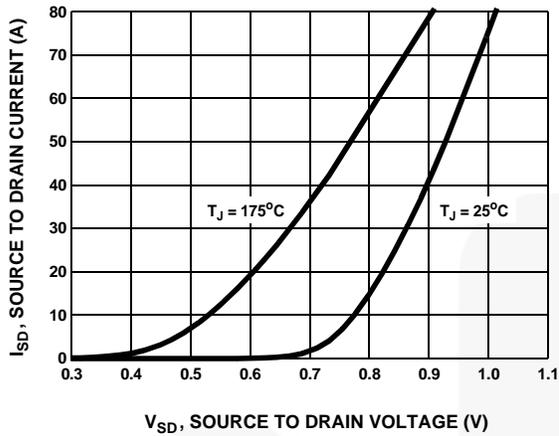


Figure 7. Body Diode Forward Voltage vs Body Diode Current

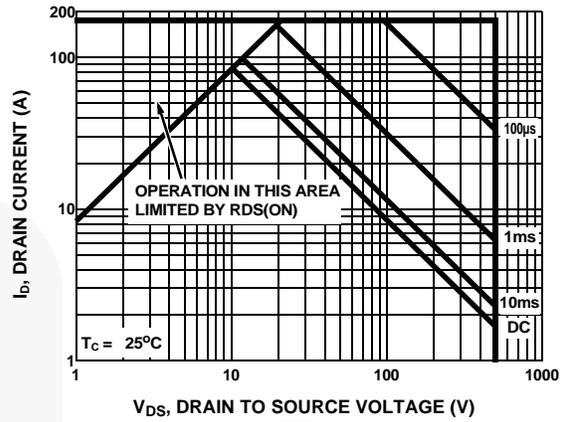


Figure 8. Maximum Safe Operating Area

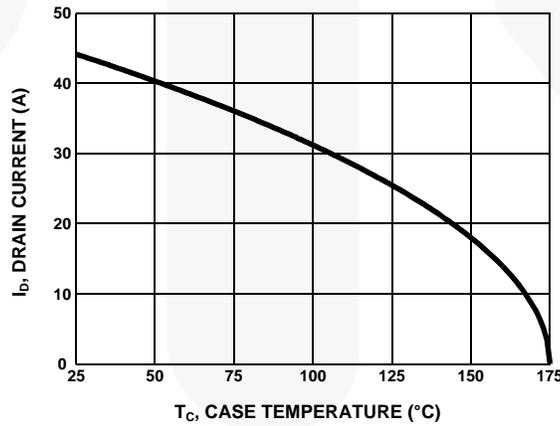


Figure 9. Maximum Drain Current vs Case Temperature

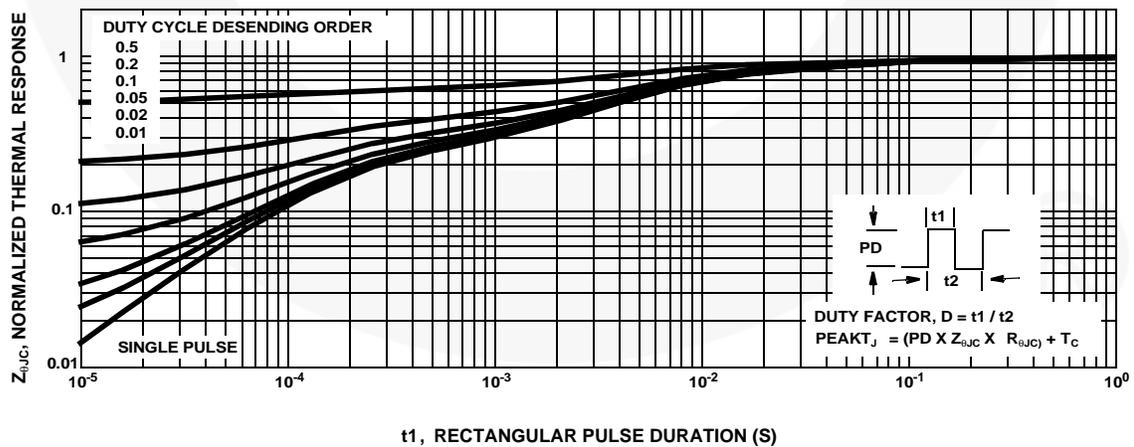


Figure 10. Normalized Transient Thermal Impedance, Junction to Case

## Test Circuits and Waveforms

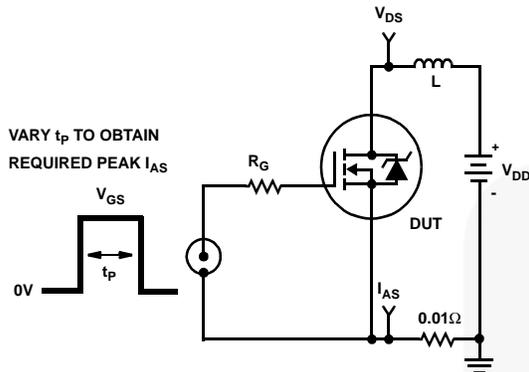


Figure 11. Unclamped Energy Test Circuit

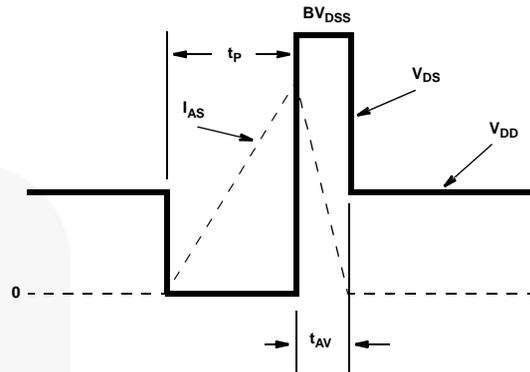


Figure 12. Unclamped Energy Waveforms

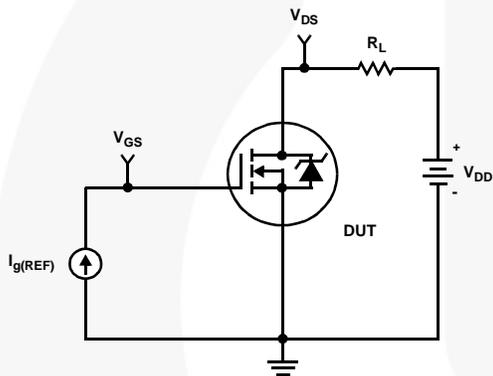


Figure 13. Gate Charge Test Circuit

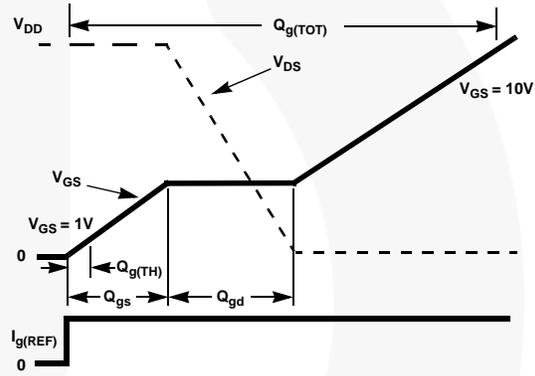


Figure 14. Gate Charge Waveforms

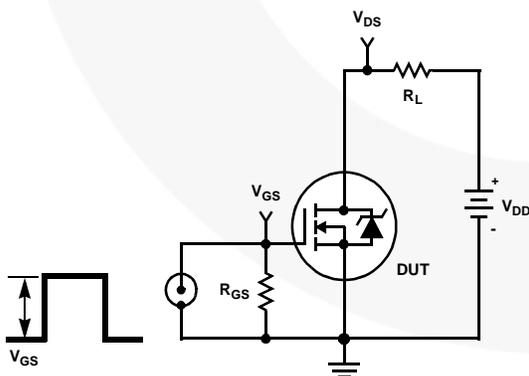


Figure 15. Switching Time Test Circuit

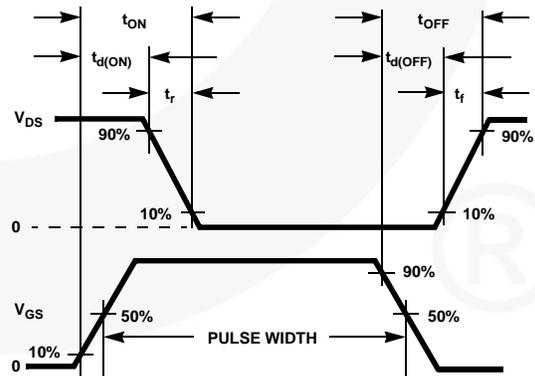
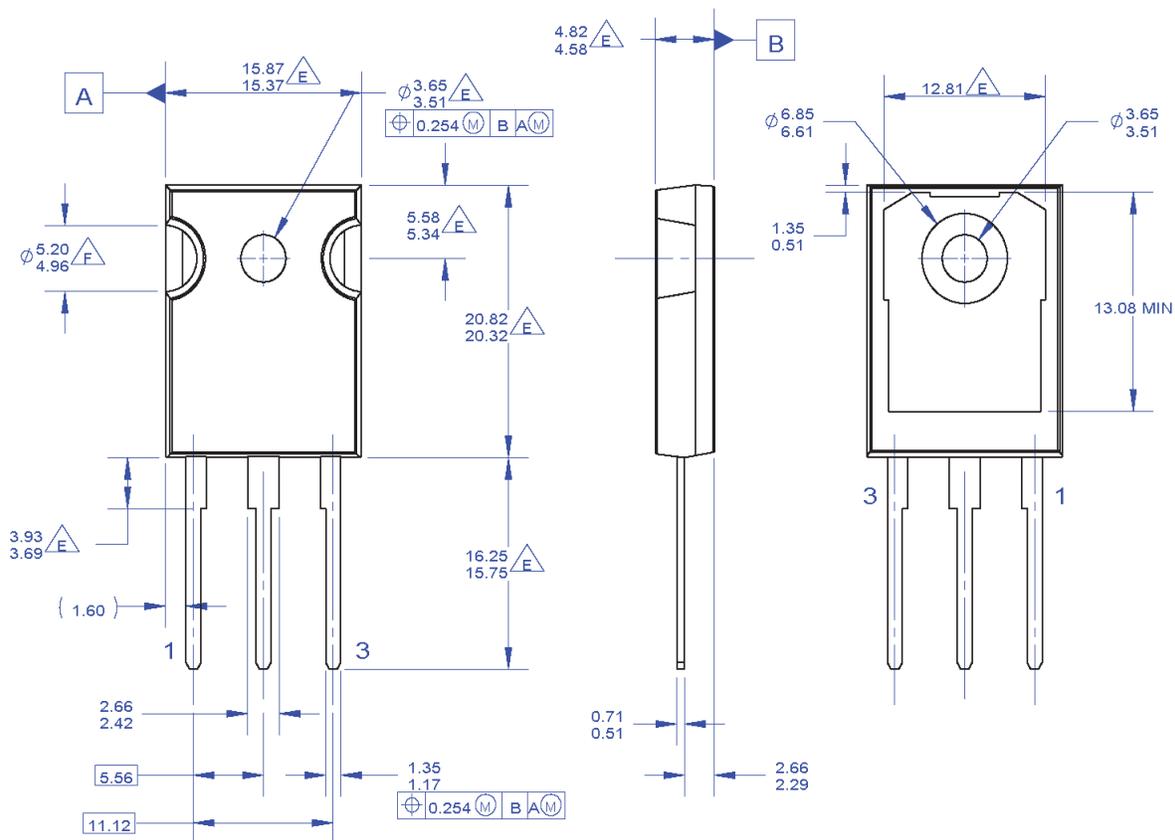


Figure 16. Switching Time Waveform

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

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- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

DOES NOT COMPLY JEDEC STANDARD VALUE

NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03\_REV03

**Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB**

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