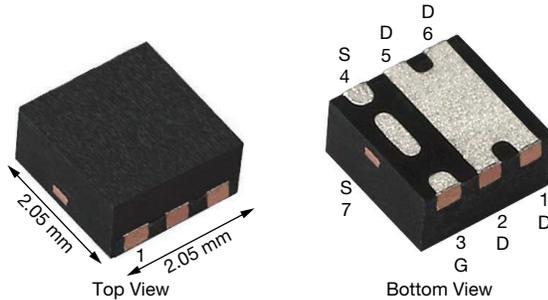


P-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (Typ.)
-150	2.6 at V _{GS} = -10 V	-1.6 ^a	4.2 nC
	2.7 at V _{GS} = -6 V	-1.6 ^a	

PowerPAK® SC-70-6L Single

Marking Code: B4

Ordering Information:

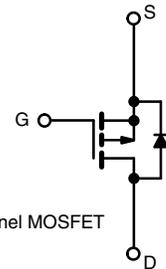
SiA485DJ-T1-GE3 (Lead (Pb)-free and halogen-free)

FEATURES

- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
 - Small footprint area
 - Low on-resistance
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE
APPLICATIONS

- Active clamp switch
- Load switch



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	-150	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	-1.6	A
	T _C = 70 °C		-1.3	
	T _A = 25 °C		-0.7 ^{b, c}	
	T _A = 70 °C		-0.57 ^{b, c}	
Pulsed Drain Current (t = 100 μs)		I _{DM}	-2	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	-1.6	
	T _A = 25 °C		-1.6 ^{b, c}	
Avalanche Current		I _{AS}	-1.5	
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	0.1	mJ
Maximum Power Dissipation	T _C = 25 °C	P _D	15.6	W
	T _C = 70 °C		10	
	T _A = 25 °C		2.9 ^{b, c}	
	T _A = 70 °C		1.8 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	32	43	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	6	8	

Notes

- T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA	-150	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-2.5	-	-4.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -150 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -150 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-0.8	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -0.5 A	-	2.1	2.6	Ω
		V _{GS} = -6 V, I _D = -0.5 A	-	2.2	2.7	
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -0.5 A	-	1.5	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = -75 V, V _{GS} = 0 V, f = 1 MHz	-	155	-	pF
Output Capacitance	C _{oss}		-	8	-	
Reverse Transfer Capacitance	C _{rss}		-	5.5	-	
Total Gate Charge	Q _g	V _{DS} = -75 V, V _{GS} = -10 V, I _D = -0.5 A	-	4.2	6.3	nC
Gate-Source Charge	Q _{gs}		-	0.9	-	
Gate-Drain Charge	Q _{gd}		-	1.3	-	
Gate Resistance	R _g	f = 1 MHz	2	10	20	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -75 V, R _L = 75 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 1 Ω	-	5	10	ns
Rise Time	t _r		-	20	40	
Turn-Off Delay Time	t _{d(off)}		-	10	20	
Fall Time	t _f		-	20	40	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-		-1.6	A
Pulse Diode Forward Current	I _{SM}		-		-2	
Body Diode Voltage	V _{SD}	I _S = -0.5 A, V _{GS} = 0 V	-	-0.8	-1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = -1 A, dI/dt = 100 A/μs, T _J = 25 °C	-	40	80	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	65	130	nC
Reverse Recovery Fall Time	t _a		-	28	-	ns
Reverse Recovery Rise Time	t _b		-	12	-	

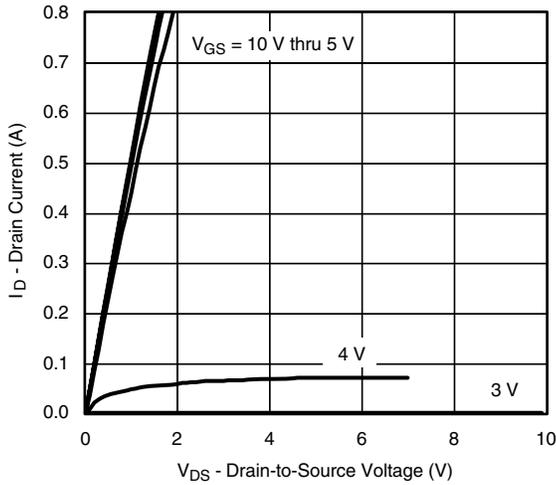
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

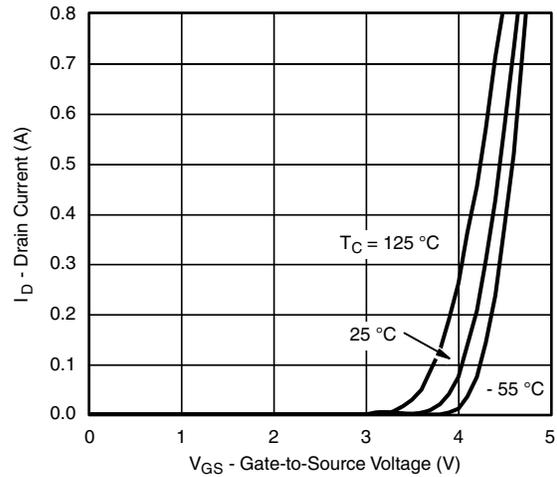
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



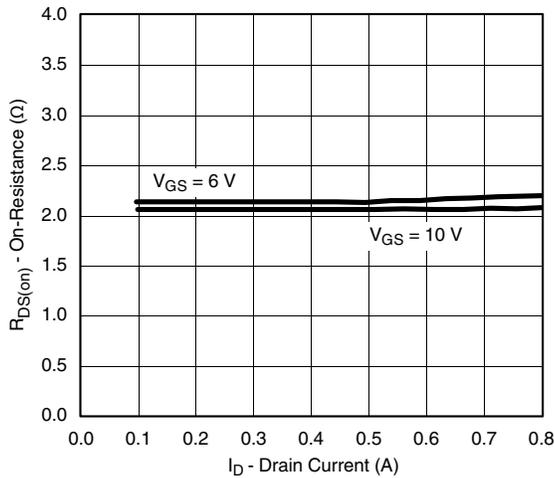
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



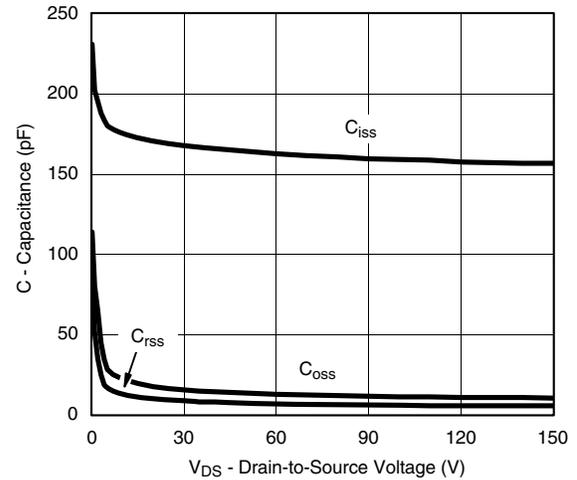
Output Characteristics



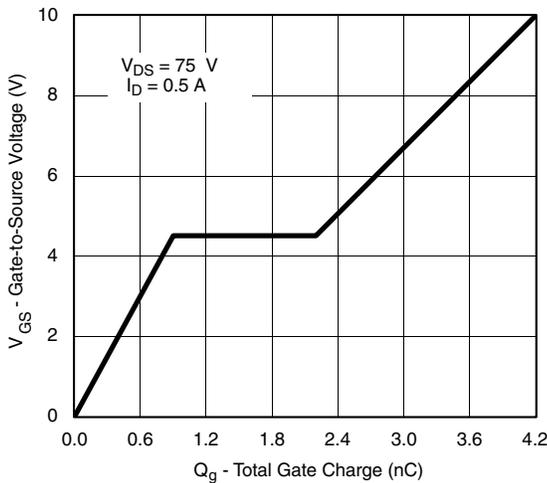
Transfer Characteristics



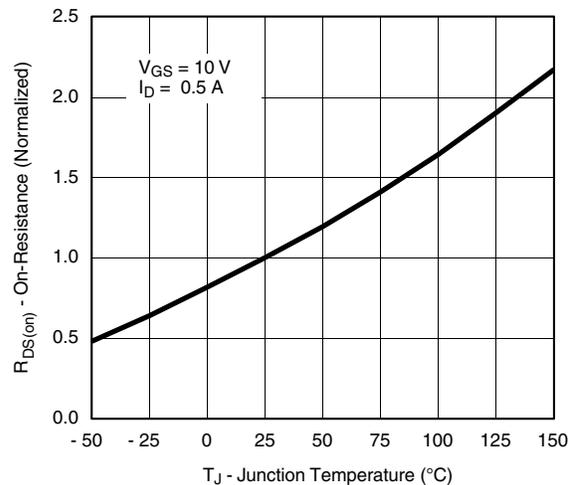
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



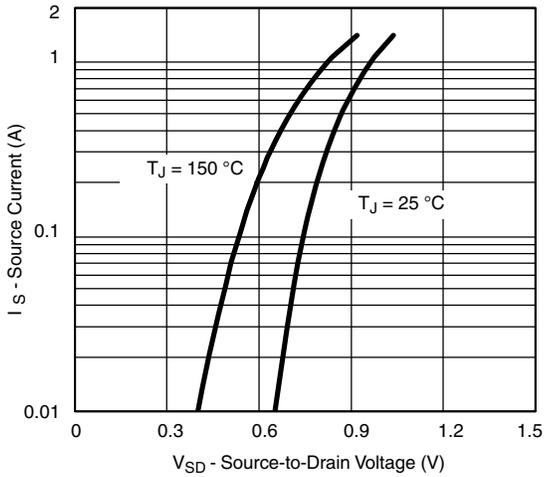
Gate Charge



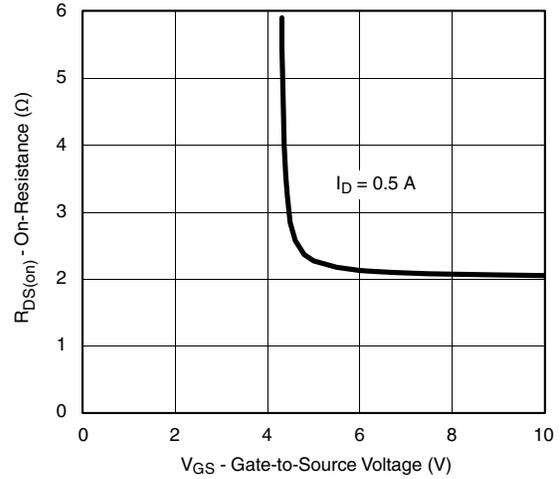
On-Resistance vs. Junction Temperature



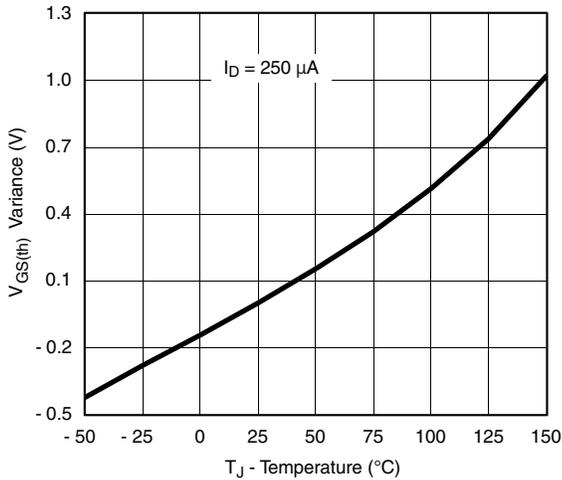
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



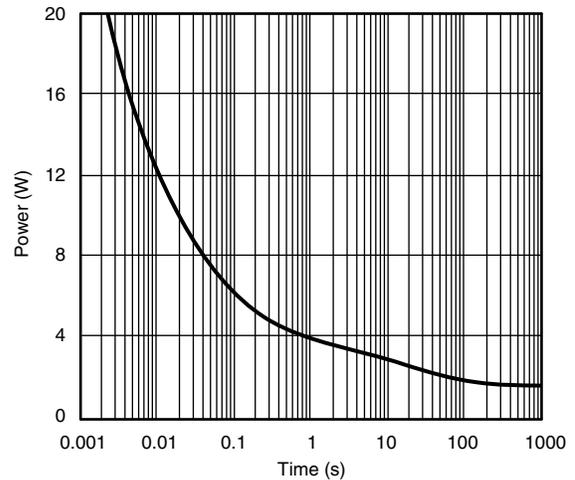
Source-Drain Diode Forward Voltage



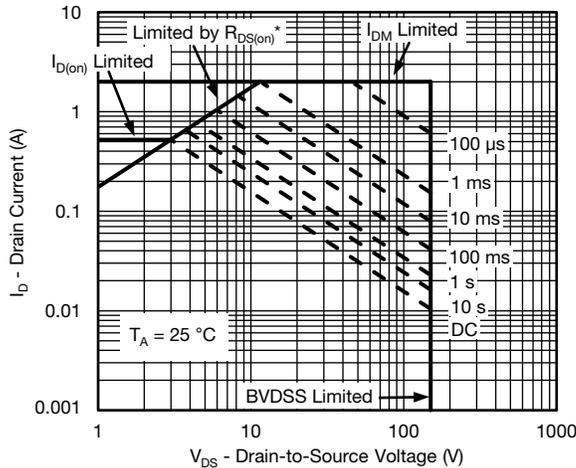
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



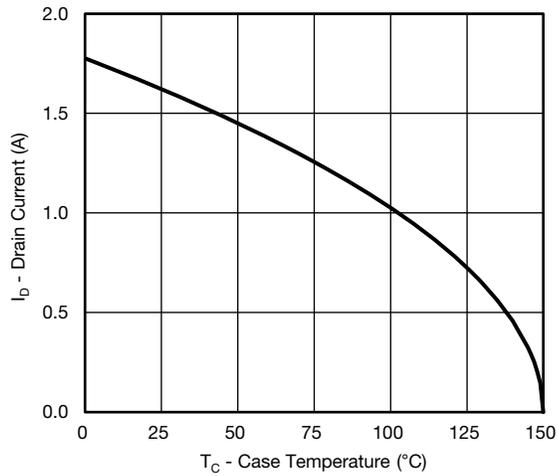
Single Pulse Power, Junction-to-Ambient



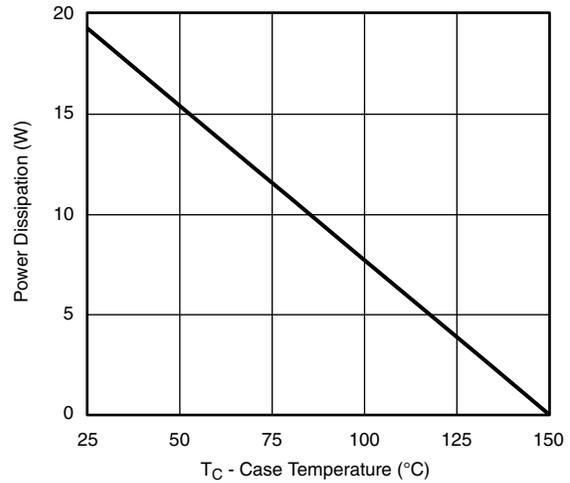
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*

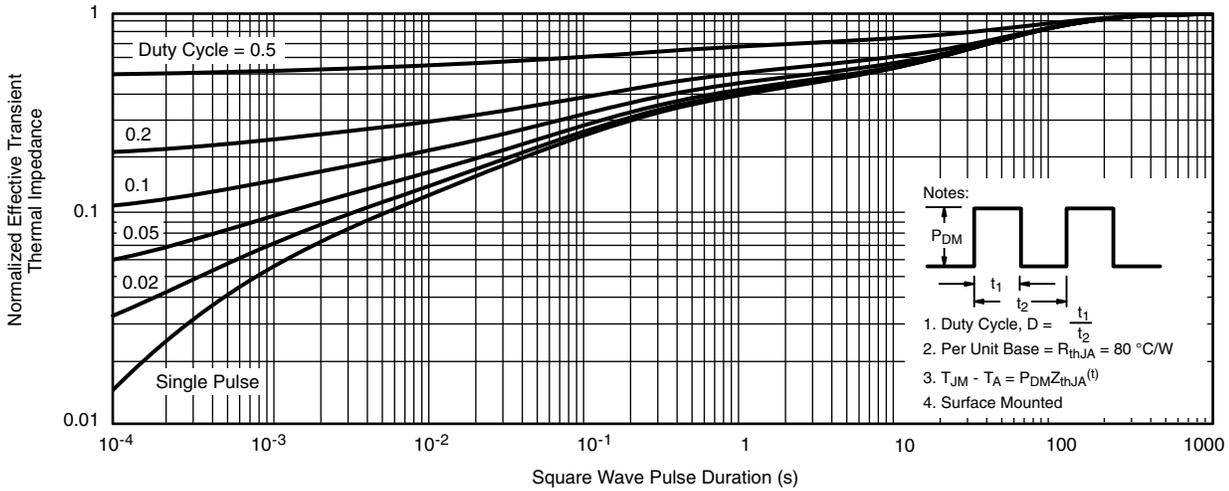


Power Derating

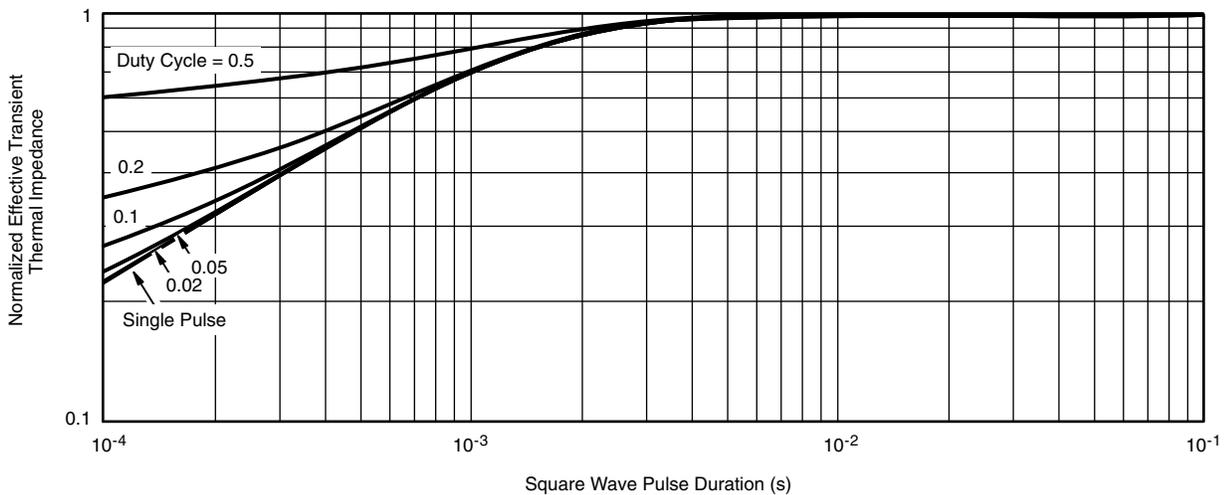
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



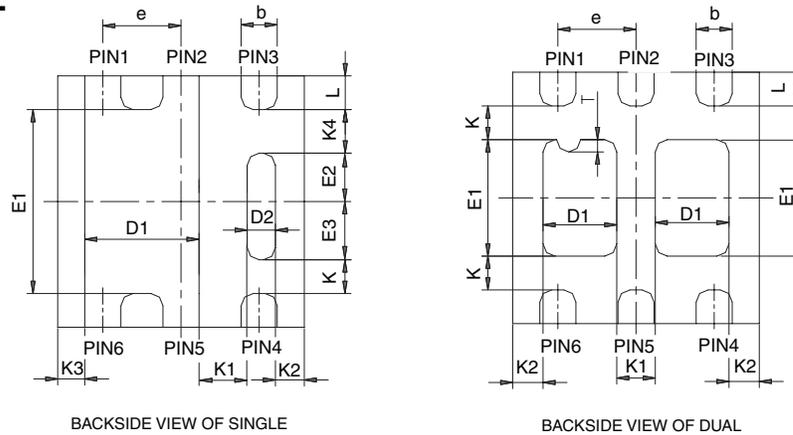
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

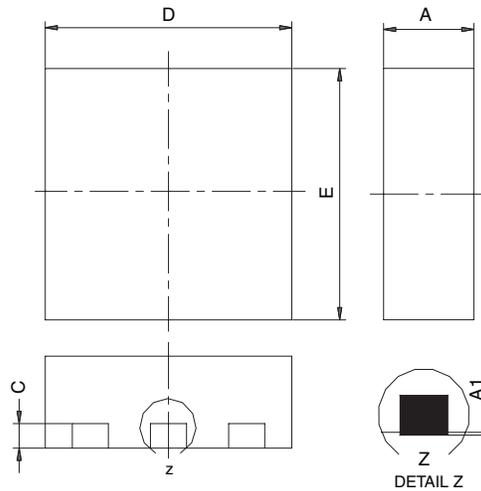
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62988.

PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL

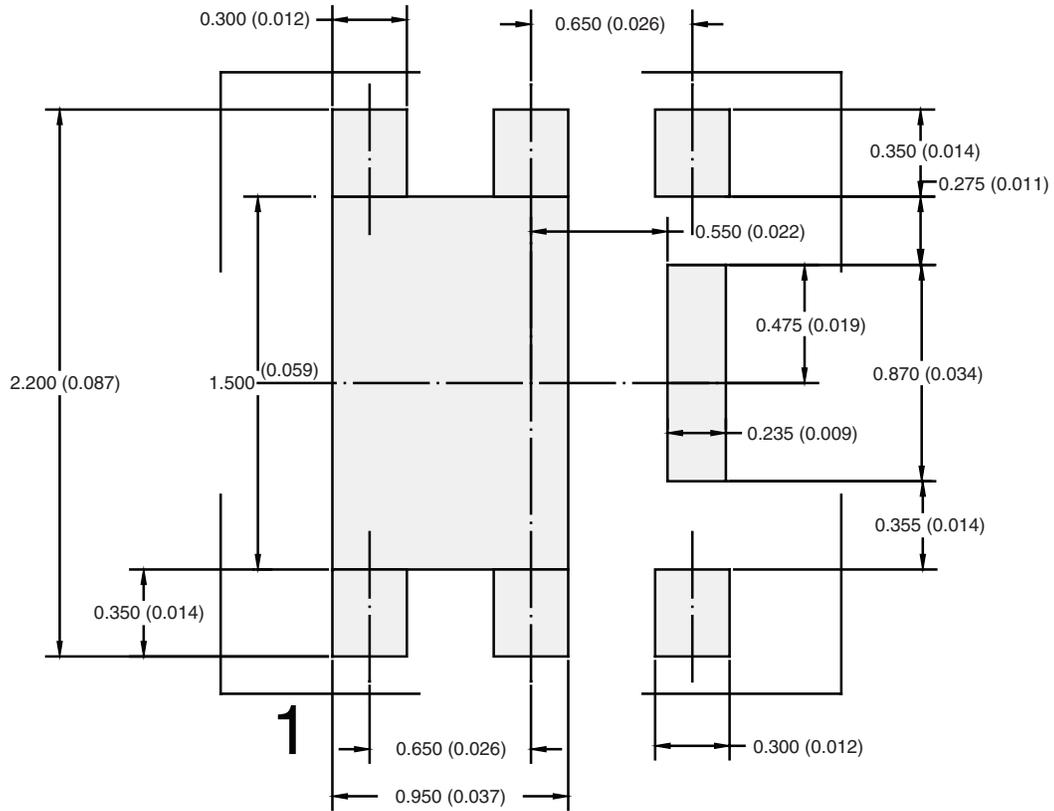


- Notes:
1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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<http://moschip.ru/get-element>

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