Rev 0; 4/06

DALLAS SEMICONDUCTOR MAXIM

Triple, 8-Bit NV Variable Resistor with Dual Settings and User EEPROM

DS3901

General Description

The DS3901 is a triple, 8-bit nonvolatile (NV) variable resistor. Each of the resistors has two setting registers, which are selectable by software or by pin configuration. The selected register determines the value of the variable resistor. Additionally, all three resistors have a high-impedance setting. Resistor R0 has the additional flexibility of allowing an external shunt resistor to provide increased dynamic range. Internal address settings allow the DS3901 slave address to be programmed to one of 128 possible addresses. The DS3901 also features an optional password-protection scheme that allows the protection of sensitive data.

Features

- **Three 256-Position Linear Digital Resistors**
- **Full-Scale Resistances 50kΩ, 30kΩ, 20kΩ**
- **Dual NV Settings for Each Resistor**
- **Low Temperature-Coefficient Resistors**
- **I²C Serial Interface**
- **Wide Operating Voltage (2.4V to 5.5V)**
- **Two-Level Password Write Protection**
- **232 Bytes of User EEPROM**
- **Programmable Slave Address**
- **-40°C to +95°C Operating Temperature Range**

Applications

Optical Transceivers

Optical Transponders

Instrumentation and Industrial Controls

RF Power Amps

Audio Power-Amp Biasing

Replacement for Mechanical Variable Resistors and DIP Switches

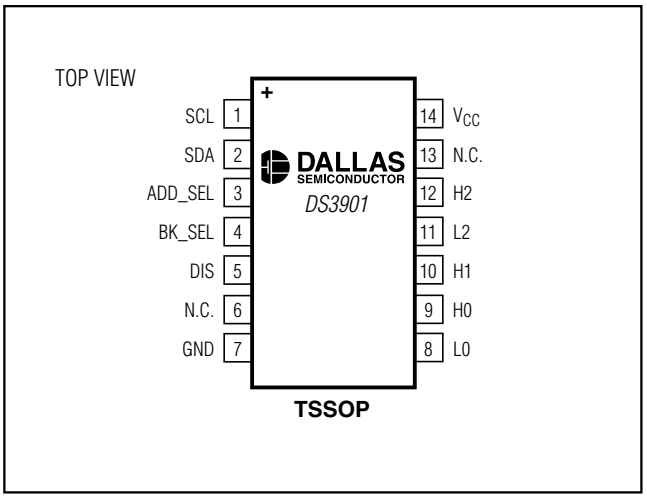
Typical Operating Circuit appears at end of data sheet.

Ordering Information

PART	TEMP RANGE	RESISTOR VALUES FOR R0, R1, AND R2	PIN-PACKAGE
DS3901E+	-40°C to +95°C	50kΩ, 30kΩ, 20kΩ	14 TSSOP

+Denotes lead-free package.

Pin Configuration



TSSOP

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Triple, 8-Bit NV Variable Resistor with Dual Settings and User EEPROM

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC}, SDA, SCL Relative to GND .....-0.5V to +6.0V
Voltage on ADD_SEL, BK_SEL, DIS Relative to GND .....-0.5V to (V_{CC} + 0.5V), not to exceed +6.0V
Voltage on H0, H1, H2, L2, L0 Relative to GND.....-0.5V to +6.0V
Maximum Resistor Current.....3mA

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....Refer to IPC/JEDEC J-STD-020 Specification
Maximum Switch Current 3mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.4		5.5	V
Input Logic 0 (SDA, SCL, ADD_SEL)	V_{IL}	(Note 1)	-0.3		0.3 x V_{CC}	V
Input Logic 1 (SDA, SCL, ADD_SEL)	V_{IH}	(Note 1)	0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (BK_SEL, DIS)	V_{IL}	(Note 1)	-0.3		+0.8	V
Input Logic 1 (BK_SEL, DIS)	V_{IH}	(Note 1)	2.0		V_{CC} + 0.3	V
Voltage on Resistor Inputs	H0, H1, L0, H2, L2		-0.3		+5.5	V
Switch Current (L0_SW, Hi-Z0, Hi-Z1, Hi-Z2)	I_{SW}	(Note 2)			3	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.4V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	I_{STBY}	(Note 3)			250	µA
Input Leakage	I_L		-1		+1	µA
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	
Pulldown Resistance (BK_SEL)	R_{BK}		20	30	45	kΩ
Pullup Resistance (DIS)	R_{DIS}		20	30	45	kΩ
BK_SEL Pulse Width			20			µs

ANALOG RESISTOR CHARACTERISTICS

(V_{CC} = +2.4V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resistor Tolerance		T_A = +25°C	-20		+20	%
Position 00h Resistance	R0, R2			242	500	Ω
	R1			149	250	
Position FFh Resistance	R0			50		kΩ
	R1			30		
	R2			20		
Switch Resistance	R_{L0_SW}	At 3mA			150	Ω
Absolute Linearity		(Note 4)	-0.75		+0.75	LSB
Relative Linearity		(Note 5)	-0.75		+0.75	LSB
Temperature Coefficient		Position FFh (Notes 2, 6)		50		ppm/°C
Hi-Z Resistor Leakage	I_{RHIZ}	H0, H1, H2, L0, or L2 = V_{CC}	-1		+1	µA

I²C CHARACTERISTICS

(V_{CC} = +2.4V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted. Timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 7)	0		400	kHz
Bus Free Time between STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup time	$t_{SU:STA}$		0.6			µs
Rise Time of Both SDA and SCL Signals	t_R	(Note 8)	$20 + 0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 8)	$20 + 0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B	(Note 8)			400	pF
EEPROM Write Time	t_W	(Note 9)			10	ms
Input Capacitance	C_I			5		pF
Startup Time	t_{ST}			0.3	2	ms

Triple, 8-Bit NV Variable Resistor with Dual Settings and User EEPROM

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.4V to +5.5V.)

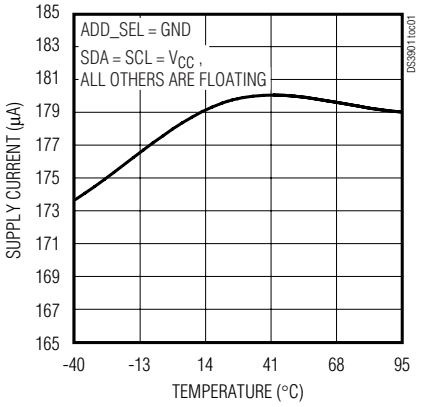
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		T_A =+ 70 °C (Note 2)	50,000			

Note 1: All voltages referenced to ground.
Note 2: Guaranteed by design.
Note 3: I_{STBY} specified for the inactive state measured with SDA = SCL = V_{CC}, ADD_SEL = GND, BK_SEL, DIS, H0, H1, H2, L2, L0 floating.
Note 4: Absolute linearity is the deviation of a measured resistor-setting value from the expected value at each particular resistor setting. Expected value is calculated by connecting a straight line from the measured minimum setting to the measured maximum setting.
Note 5: Relative linearity is the deviation of the step size change between two LSB settings from the expected step size. The expected LSB step size is the slope of the straight line from measured minimum position to measured maximum position.
Note 6: See the *Typical Operating Characteristics*.
Note 7: Timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I^2C standard mode.
Note 8: CB—total capacitance of one bus line in picofarads.
Note 9: EEPROM write begins after a STOP condition occurs.

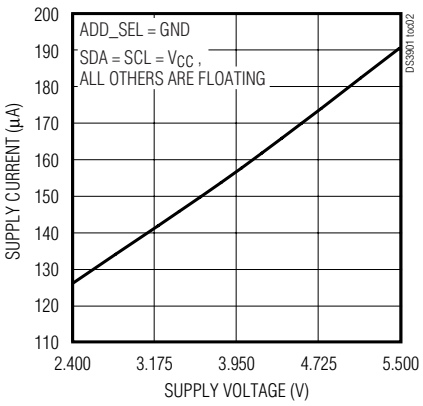
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

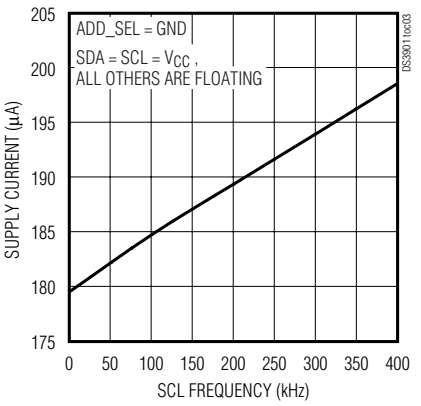
SUPPLY CURRENT vs. TEMPERATURE



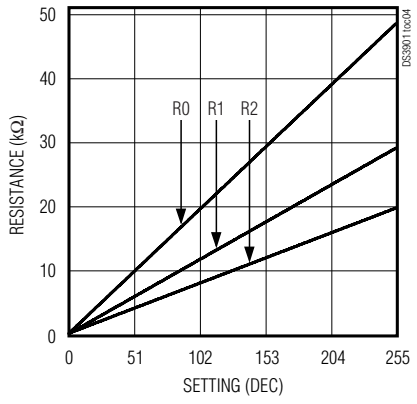
SUPPLY CURRENT vs. SUPPLY VOLTAGE



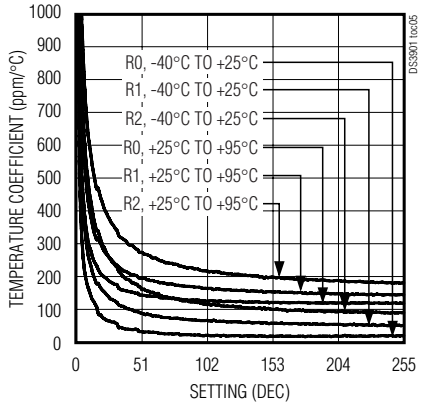
SUPPLY CURRENT vs. SCL FREQUENCY



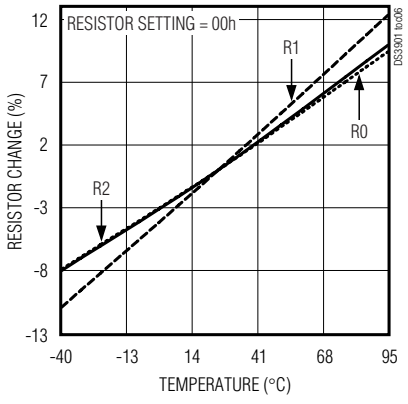
RESISTANCE vs. RESISTOR SETTING



TEMPERATURE COEFFICIENT vs. RESISTOR SETTING



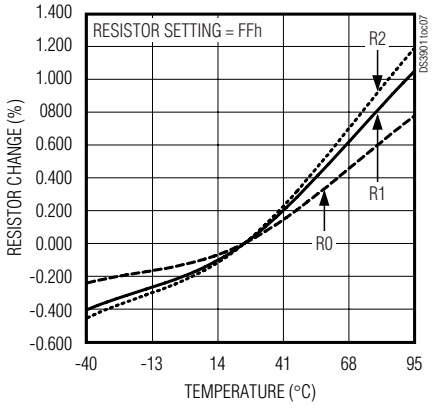
CHANGE IN RESISTANCE vs. TEMPERATURE



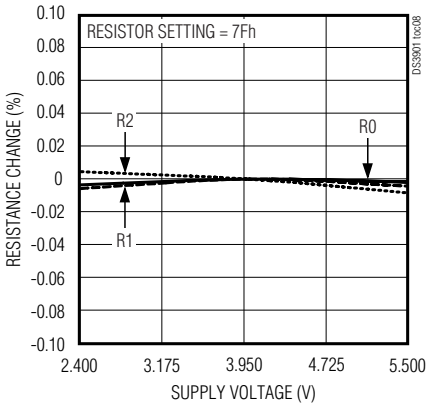
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

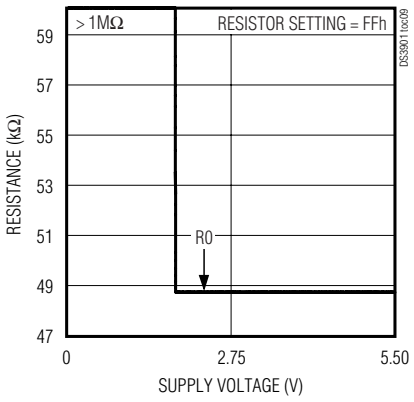
CHANGE IN RESISTANCE vs. TEMPERATURE



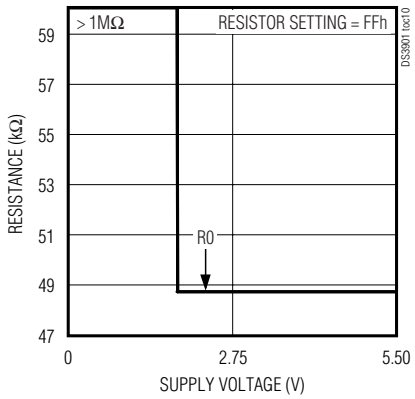
RESISTANCE vs. SUPPLY VOLTAGE



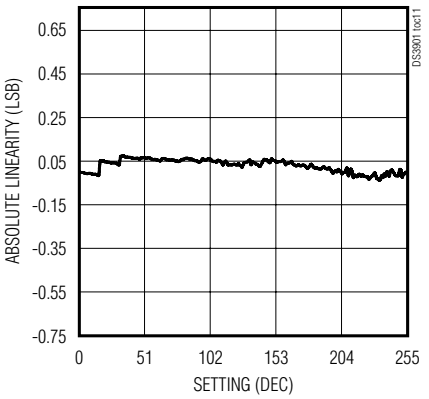
RESISTANCE vs. POWER-UP SUPPLY VOLTAGE



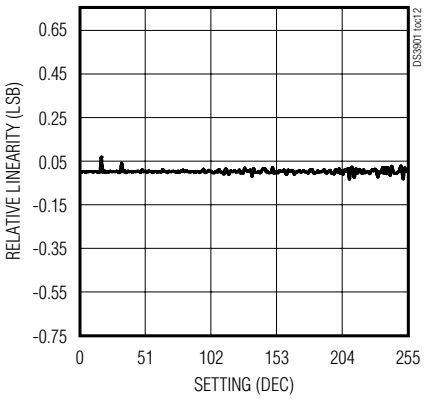
RESISTANCE vs. POWER-DOWN SUPPLY VOLTAGE



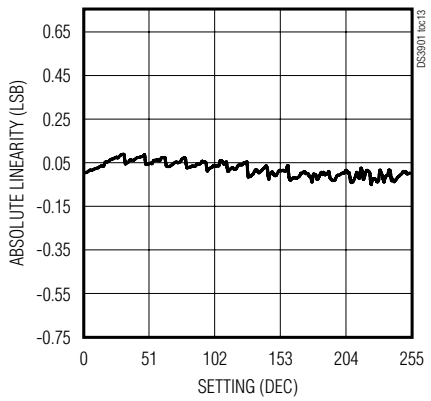
R0 ABSOLUTE LINEARITY vs. RESISTOR SETTING



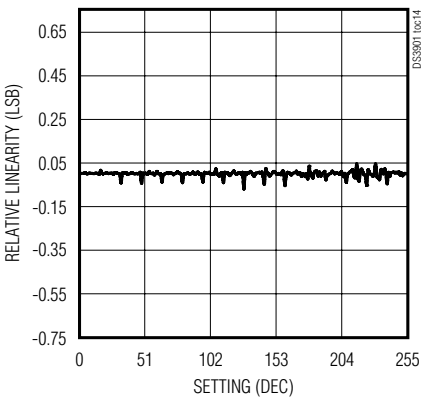
R0 RELATIVE LINEARITY vs. RESISTOR SETTING



R1 ABSOLUTE LINEARITY vs. RESISTOR SETTING



R1 RELATIVE LINEARITY vs. RESISTOR SETTING

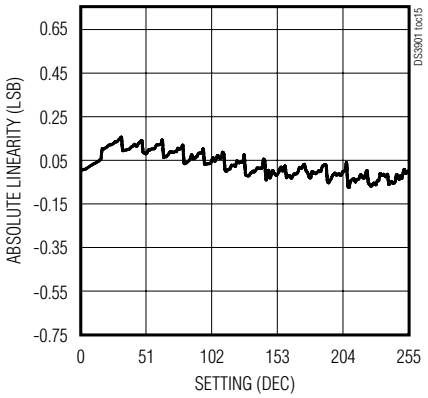


Triple, 8-Bit NV Variable Resistor with Dual Settings and User EEPROM

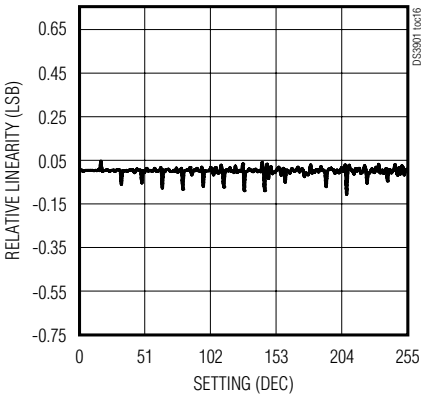
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

R2 ABSOLUTE LINEARITY vs. RESISTOR SETTING



R2 RELATIVE LINEARITY vs. RESISTOR SETTING

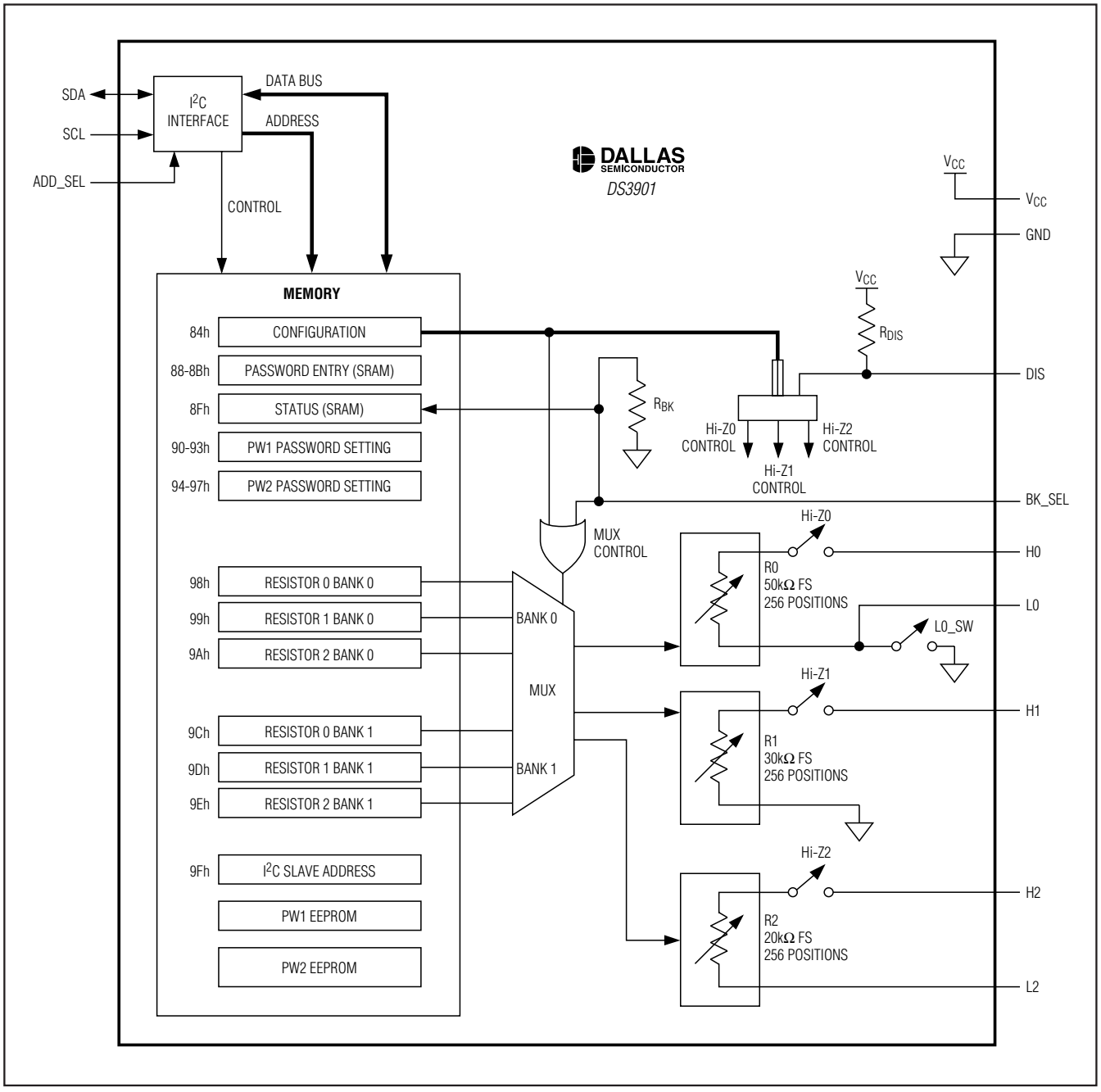


Pin Description

PIN	NAME	FUNCTION
1	SCL	I^2C Clock Input
2	SDA	I^2C Data I/O Pin
3	ADD_SEL	I^2C Slave Address Select Pin
4	BK_SEL	Bank Select Pin. This pin has an internal pulldown resistor, R_{BK}.
5	DIS	High-Impedance Disable Input. This pin has an internal pullup resistor, R_{DIS}.
6, 13	N.C.	No Connection
7	GND	Ground
8	L0	Resistor 0 Low Terminal
9	H0	Resistor 0 High Terminal
10	H1	Resistor 1 High Terminal
11	L2	Resistor 2 Low Terminal
12	H2	Resistor 2 High Terminal
14	V_{CC}	Voltage Supply

Triple, 8-Bit NV Variable Resistor with Dual Settings and User EEPROM

Block Diagram



Triple, 8-Bit NV Variable Resistor with Dual Settings and User EEPROM

Detailed Description

The DS3901 contains three configurable variable resistors. The *Block Diagram* illustrates the features of the DS3901. The following sections discuss these features in detail.

Dual Bank Resistor Settings

The setting for each resistor can be loaded from one of two possible registers. These registers are referred to as "banks" with each resistor having a "Bank 0" and "Bank 1" value. The bank to be loaded as the resistor value is selected by the OR'ing of the BK_SEL pin logic state and the BSC control bit (bit 3, register 84h). See the *Memory Map* section for details. If the result of the OR'ing is a 0, then all three resistors will use the values stored in their Bank 0 locations. If the result is a 1, then all three resistors will use the values stored in their Bank 1 locations.

Shunt Resistor Switch

Resistor 0 has the option to have an external fixed resistor connected to the L0 pin. This provides a means to select between a standard full-scale resistor value and an extended full-scale value. By default, the L0_SW bit (bit 4 of the Configuration Register, 84h) is set to a value of 0. When the L0_SW bit is 0, the internal connection from the low side of Resistor 0 to ground is opened, and the low terminal of Resistor 0 is only connected to the L0 pin. This allows for an external resistor to be attached to the L0 pin for an extended full-scale value. By writing the switch control bit L0_SW to a 1, the low terminal of Resistor 0 is internally connected to ground.

High-Impedance Function

There are two ways to place the resistors in a high-impedance (Hi-Z) state. One way is to set the DIS pin to a 1. This is done by either floating the pin (there is an internal pullup resistor, R_{DIS}) or by connecting DIS directly to V_{CC}. When the DIS pin is held high or left floating, all three resistors are held in a high-impedance state. The second method is to use bits 0 to 2 of the Configuration Register (84h), to set each resistor to a high-impedance state (see the *Memory Map* section for details). The state of the DIS pin overrides the state of the high-impedance control bits (see the *Memory Map* section for details).

Slave Address Byte

The ADD_SEL pin is used to select the I^2C address of the DS3901. When the ADD_SEL pin is connected low, the I^2C address of the DS3901 is A2h. When the ADD_SEL pin is connected high, the value stored in the Slave Address register (9Fh) is used. The default value for the Slave Address register is shown in the *Memory Map* section. The Slave Address register can be programmed to one of 128 possible addresses since the LSB of the Slave Address register is reserved as the read/write bit for the I^2C command structure.

Password Protection

The memory of the DS3901 is write-protected with a two-level password scheme. All memory locations can be read without a password, with the exception of the Password Entry registers and Password Setting registers. Once the appropriate password is entered in the Password Entry bytes (88 to 8Bh), the DS3901 will allow write access to the memory areas designated for that password. The setting for the PW1 password is written in the PW1 Password Setting register (bytes 90 to 93h). The setting for the PW2 password is written in the PW2 Password Setting register (bytes 94 to 97h). See the *Memory Map* section for more details. Entering the PW2 password allows access to areas protected by the PW1 password.

When shipped from the factory, both password settings are all zeroes. Likewise, every time the device is powered up the Password Entry register (SRAM) defaults to all zeroes. If write protection is not desired, leave the password setting at the factory default and ignore the Password Entry register. Write protection goes into effect once either or both default password settings have been changed to unique values.

Memory Map

The memory consists of 256 bytes and is write-protected with a two-level password scheme. Table 1 below shows how the memory map is organized. Register details are discussed in the *Register Descriptions* section.

Table 1. Memory Map

DESCRIPTION	ADDR	BINARY MSB							LSB	FACTORY DEFAULT	ACCESS			TYPE
											NO PW	PW1	PW2	
Lower Memory	00–7Fh	PW2 EEPROM								00h	R	R	R/W	EEPROM
Memory	80–83h	PW1 EEPROM								00h	R	R/W	R/W	EEPROM
Configuration	84h				L0_SW	BSC	HiZ2	HiZ1	HiZ0	00h	R	R/W	R/W	EEPROM
Memory	85–87h	PW1 EEPROM								00h	R	R/W	R/W	EEPROM
Password Entry	88–8Bh	MSB–LSB								00h	W	W	W	SRAM
Memory	8C–8Eh	SRAM								00h	R/W	R/W	R/W	SRAM
Status	8Fh	0	0	0	BSS	0	0	0	DISS	000x000xb	R	R	R	SRAM
Password Setting PW1	90–93h	MSB–LSB								00h	—	—	W	EEPROM
Password Setting PW2	94–97h	MSB–LSB								00h	—	—	W	EEPROM
Resistor 0 Bank 0	98h	—								7Fh	R	R	R/W	EEPROM
Resistor 1 Bank 0	99h	—								7Fh	R	R	R/W	EEPROM
Resistor 2 Bank 0	9Ah	—								7Fh	R	R	R/W	EEPROM
Memory	9Bh	PW2 EEPROM								00h	R	R	R/W	EEPROM
Resistor 0 Bank 1	9Ch	—								7Fh	R	R	R/W	EEPROM
Resistor 1 Bank 1	9Dh	—								7Fh	R	R	R/W	EEPROM
Resistor 2 Bank 1	9Eh	—								7Fh	R	R	R/W	EEPROM
Slave Address	9Fh	I^2C SLAVE ADDRESS								A0h	R	R	R/W	EEPROM
Memory	A0h–FFh	PW2 EEPROM								00h	R	R	R/W	EEPROM

Register Descriptions

MEMORY REGISTERS 00h–7Fh: PW2 EEPROM

Factory Default:	00h
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

00h–7Fh	EEPROM

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MEMORY REGISTERS 80h–83h: PW1 EEPROM

Factory Default:	00h
Access Without Password:	Read only
Access With PW1 Password:	Read and Write
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

80h–83h	EEPROM

MEMORY REGISTER 84h: CONFIGURATION REGISTER

Factory Default:	00h
Access Without Password:	Read only
Access With PW1 Password:	Read and Write
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

84h				L0_SW	BSC	HiZ2	HiZ1	HiZ0
	b7							b0

bits 7–5	These bits are set to 0.
bit 4	**L0_SW:** Selectable switch (see the *Block Diagram*) that allows for an external shunt resistor to be connected to the L0 pin. 0 = Switch L0_SW is open (default). 1 = Switch L0_SW is closed.
bit 3	**BSC:** A control bit that, when OR'd with the state of the BK_SEL pin, selects which bank of registers will be used to determine the setting of Resistors 0, 1, and 2. 0 = BK_SEL pin determines which bank settings are used. 1 = Bank 1 settings are used.
bit 2	**HiZ2:** A control bit used to select a high-impedance state for Resistor 2. If the DIS pin is high, all resistors are high impedance regardless of Hi-Z control pin state. If the DIS pin is low, then the following is true: 0 = Resistor 2 is not in a high-impedance state (default). 1 = Resistor 2 is placed in a high-impedance state.
bit 1	**HiZ1:** A control bit used to select a high-impedance state for Resistor 1. If the DIS pin is high, all resistors are high impedance regardless of Hi-Z control pin state. If the DIS pin is low, then the following is true: 0 = Resistor 1 is not in a high-impedance state (default). 1 = Resistor 1 is placed in a high-impedance state.
bit 0	**HiZ0:** A control bit used to select a high-impedance state for Resistor 0. If the DIS pin is high, all resistors are high impedance regardless of Hi-Z control pin state. If the DIS pin is low, then the following is true: 0 = Resistor 0 is not in a high-impedance state. (Default) 1 = Resistor 0 is placed in a high-impedance state.

MEMORY REGISTERS 85h–87h: PW1 EEPROM

Factory Default:	00h
Access Without Password:	Read only
Access With PW1 Password:	Read and Write
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

85h–87h	EEPROM

MEMORY REGISTERS 88h-8Bh: PASSWORD ENTRY

Factory Default:	00000000h
Access Without Password:	Write only
Access With PW1 Password:	Write only
Access With PW2 Password:	Write only
Memory Type:	Volatile (SRAM)

88h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
89h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
8Ah	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
8Bh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	b7							b0

There are two passwords for the DS3901, the PW1 password and the PW2 password. The memory map register descriptions indicate the type of access granted for each level of password used. See the *Password Protection* section for details on password access.

MEMORY REGISTERS 8Ch–8Eh: SRAM

Factory Default:	00h
Access Without Password:	Read and Write
Access With PW1 Password:	Read and Write
Access With PW2 Password:	Read and Write
Memory Type:	Volatile (SRAM)

8Ch-8Eh	SRAM

MEMORY REGISTER 8Fh: STATUS

Factory Default:	000x000xb
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read only
Memory Type:	Volatile (SRAM)

8Fh	0	0	0	BSS	0	0	0	DISS
	b7							b0

bits 7–5	These bits are 0.
bit 4	**BSS:** A status bit that indicates the state of the BK_SEL pin. 0 = BK_SEL pin is low. 1 = BK_SEL pin is high.
bits 3–1	These bits are 0.
bit 0	**DISS:** A status bit that indicates the state of the DIS pin. 0 = DIS pin is low. Hi-Z control bits can be used to select high-impedance state for each resistor. 1 = DIS pin is high. All resistors are in a high-impedance state.

MEMORY REGISTERS 90h–93h: PW1 PASSWORD SETTING

Factory Default:	00000000h
Access Without Password:	None
Access With PW1 Password:	None
Access With PW2 Password:	Write only
Memory Type:	Nonvolatile (EEPROM)

90h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
91h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
92h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
93h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	b7							b0

These four bytes contain the password used to access memory that is protected by the PW1 password.

MEMORY REGISTERS 94h–97h: PW2 PASSWORD SETTING

Factory Default:	00000000h
Access Without Password:	None
Access With PW1 Password:	None
Access With PW2 Password:	Write only
Memory Type:	Nonvolatile (EEPROM)

94h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
95h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
96h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
97h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	b^{7}							b0

These four bytes contain the password used to access memory that is protected by the PW2 password.

MEMORY REGISTER 98h: RESISTOR 0, BANK 0

Factory Default:	7Fh
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

98h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	b7							b0

This register contains the Bank 0 values for Resistor 0. The OR'd result of the state of the BSC bit (bit 3, 84h) and the BK_SEL pin determines if Resistor 0 Bank 0 or Resistor 0 Bank 1 is used for the Resistor 0 setting. See the Configuration Register in Register 84h for logic details.

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MEMORY REGISTER 99h: RESISTOR 1, BANK 0

Factory Default:	7Fh
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

99h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	b7							b0

This register contains the Bank 0 values for Resistor 1. The OR'd result of the state of the BSC bit (bit 3, 84h) and the BK_SEL pin determines if Resistor 1 Bank 0 or Resistor 1 Bank 1 is used for the Resistor 1 setting. See the Configuration Register in Register 84h for logic details.

MEMORY REGISTER 9Ah: RESISTOR 2, BANK 0

Factory Default:	7Fh
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

9Ah	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	b7							b0

This register contains the Bank 0 values for Resistor 2. The OR'd result of the state of the BSC bit (bit 3, 84h) and the BK_SEL pin determines if Resistor 2 Bank 0 or Resistor 2 Bank 1 is used for the Resistor 2 setting. See the Configuration Register in Register 84h for logic details.

MEMORY REGISTER 9Bh: PW2 EEPROM

Factory Default:	00h
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

9Bh	EEPROM

MEMORY REGISTER 9Ch: RESISTOR 0, BANK 1

Factory Default:	7Fh
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

9Ch	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	b7							b0

This register contains the Bank 1 values for Resistor 0. The OR'd result of the state of the BSC bit (bit 3, 84h) and the BK_SEL pin determines if Resistor 0 Bank 0 or Resistor 0 Bank 1 is used for the Resistor 0 setting. See the Configuration Register in Register 84h for logic details.

MEMORY REGISTER 9Dh: RESISTOR 1, BANK 1

Factory Default:	7Fh
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

9Dh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	b7							b0

This register contains the Bank 1 values for Resistor 1. The OR'd result of the state of the BSC bit (bit 3, 84h) and the BK_SEL pin determines if Resistor 1 Bank 0 or Resistor 1 Bank 1 is used for the Resistor 1 setting. See the Configuration Register in Register 84h for logic details.

MEMORY REGISTER 9Eh: RESISTOR 2, BANK 1

Factory Default:	7Fh
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

9Eh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	b7							b0

This register contains the Bank 1 values for Resistor 2. The OR'd result of the state of the BSC bit (bit 3, 84h) and the BK_SEL pin determines if Resistor 2 Bank 0 or Resistor 2 Bank 1 is used for the Resistor 2 setting. See the Configuration Register in Register 84h for logic details.

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MEMORY REGISTER 9Fh: SLAVE ADDRESS REGISTER

Factory Default:	A0h
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

9Fh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	b7							b0

The I^2C slave address of the DS3901 depends on the state of the ADD_SEL pin. If this pin is low, then the slave address is fixed at A2h. If the ADD_SEL pin is high, then the slave address is determined by the value stored in EEPROM at address 9Fh. Factory default value for the slave address is A0h. The seven most significant bits are used (the LSB is not used because it is in the bit position of the R/W bit) to allow the slave address to be programmed to one of 128 possible addresses.

MEMORY REGISTERS A0h–FFh: PW2 EEPROM

Factory Default:	00h
Access Without Password:	Read only
Access With PW1 Password:	Read only
Access With PW2 Password:	Read and Write
Memory Type:	Nonvolatile (EEPROM)

A0h–FFh	EEPROM

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See the timing diagram for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See the timing diagram for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it immediately initiates a new data transfer following the current one. Repeated STARTS are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold-time requirements (see Figure 1). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (see Figure 1) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 1) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

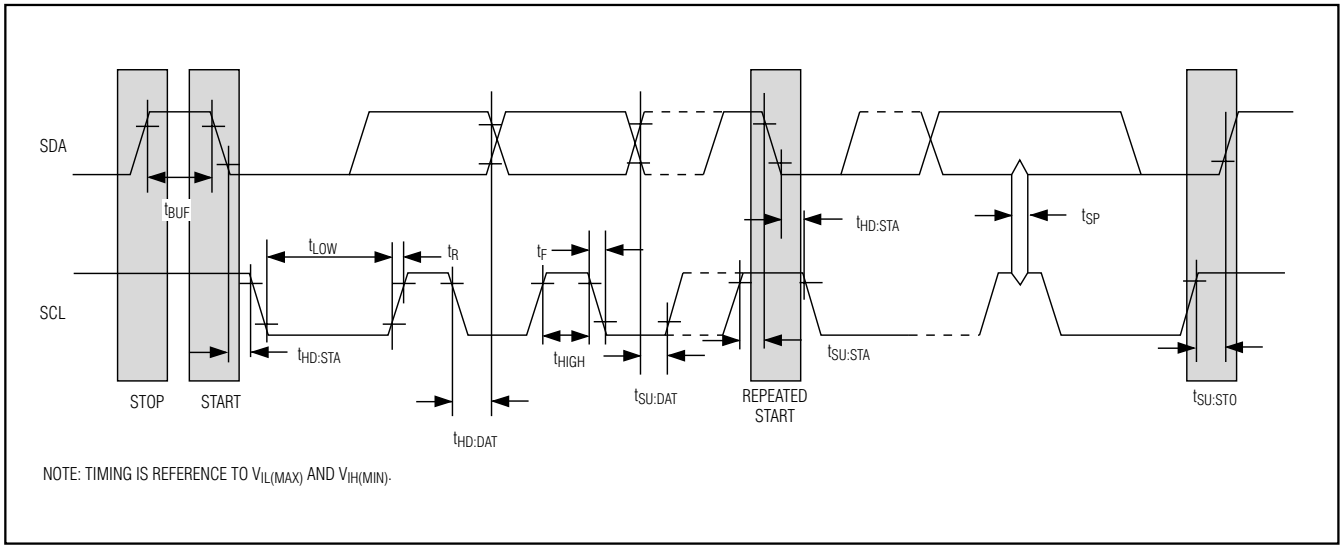


Figure 1. I²C Timing Diagram

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Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (MSB first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (MSB first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I^2C bus responds to a slave addressing byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The ADD_SEL pin and Slave Address register (9Fh) determine the I^2C slave address for the DS3901. If ADD_SEL is low, then the slave address is fixed at A2h. If ADD_SEL is high, then the slave address in the Slave Address Register (9Fh) is used.

The LSB of the Slave Address Byte is the R/$\overline{W}$ bit. If the R/$\overline{W}$ bit is 0, then the master indicates it will write data to the slave. If R/$\overline{W}$ = 1, then the master will read data from the slave. If an incorrect slave address is written, the DS3901 will assume the master is communicating with another I^2C device and ignore the communication until the next START condition is sent.

Memory Address: During an I^2C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I^2C Communication

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition.

The DS3901 is capable of writing up to 8 bytes (1 page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page.

Attempts to write to additional pages of memory without sending a STOP condition between pages result in the address counter wrapping around to the beginning of the present row. To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, and then wait for the bus free or EEPROM write time to elapse. Then the master may generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time an EEPROM page is written, the DS3901 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the page to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the DS3901, which allows the next page to be written as soon as the DS3901 is ready to receive the data. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to write again to the device.

EEPROM Write Cycles: When EEPROM writes occur, the DS3901 will write the whole EEPROM memory page even if only a single byte on the page was modified. Writes that do not modify all 8 bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes on the page that were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. The DS3901's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte, it NACKs to indicate the end of the transfer and generates a stop condition. This can be done with or without modifying the address counter's location before the read cycle.

Applications Information

Power-Supply Decoupling

To achieve best results, it is recommended that the power supply is decoupled with a 0.01µF or a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins to minimize lead inductance.

SDA and SCL Pullup Resistors

SDA is an open-collector output on the DS3901 that requires a pullup resistor to realize high logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be utilized for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *AC Electrical Characteristics* are within specification.

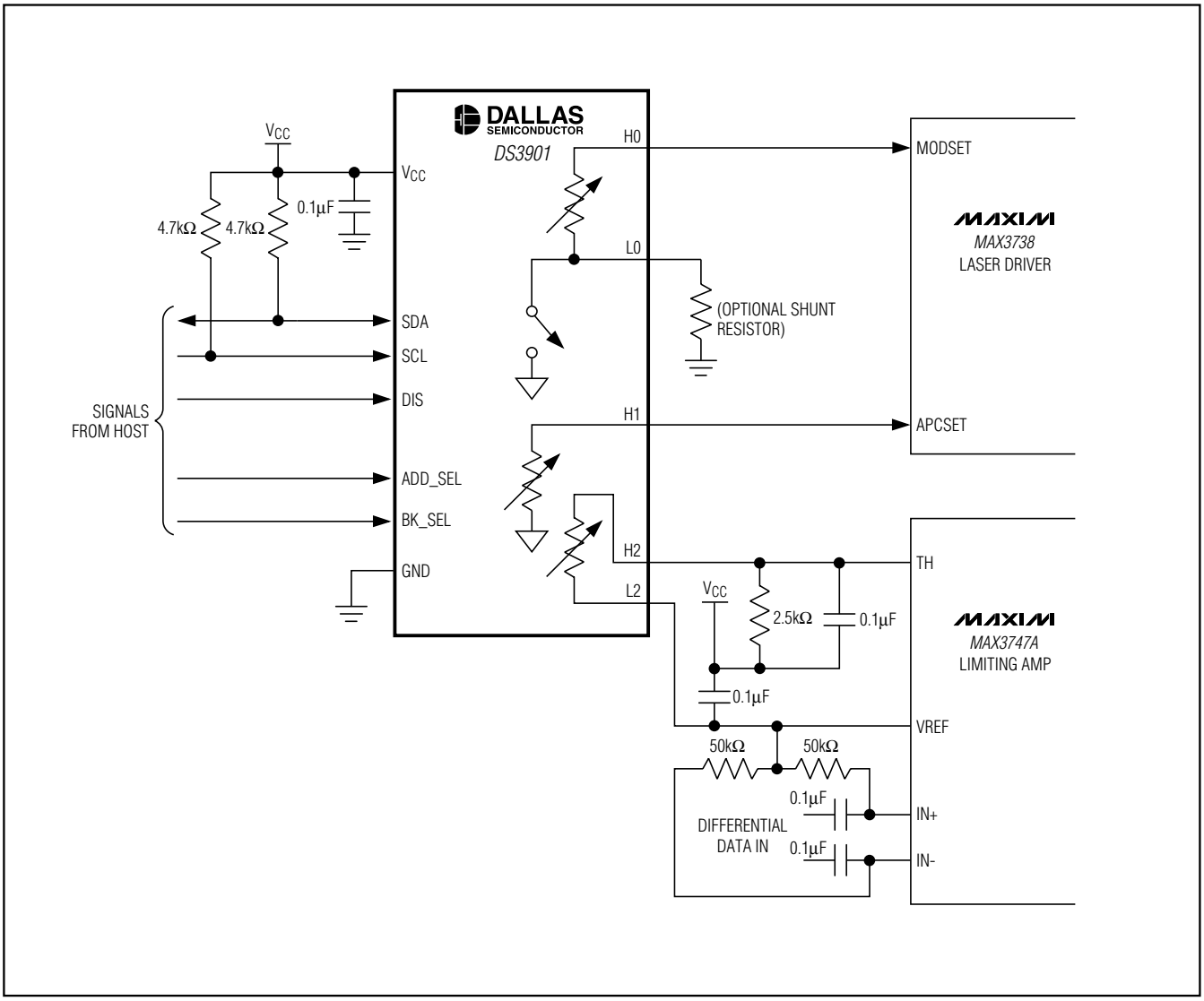
Chip Topology

TRANSISTOR COUNT: 52,353

SUBSTRATE CONNECTED TO GROUND

Triple, 8-Bit NV Variable Resistor with Dual Settings and User EEPROM

Typical Operating Circuit



Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

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