

LCD Segment Drivers

# Multi-function LCD Segment Drivers

**BU91510KV-M**

**MAX 216 Segment(54SEG x 4COM)**

**General Description**

The BU91510KV-M is 1/4 or 1/3 Duty General-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The BU91510KV-M can drive up to 216 LCD Segments directly. The BU91510KV-M can also control up to 6 General-purpose output pins / 6 PWM output pins.

**Key Specifications**

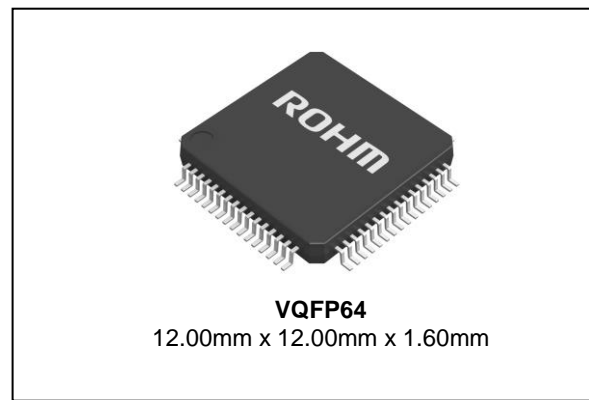
- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments: 216 Segments
- Display Duty: 1/3, 1/4 Selectable
- Bias: 1/2, 1/3 Selectable
- Interface: 3wire Serial Interface

**Features**

- AEC-Q100 Qualified (Note 1)
  - Either 1/4 or 1/3 Duty can be selected with the Serial Control Data.
    - 1/4 Duty Drive: up to 216 Segments
    - 1/3 Duty Drive: up to 162 Segments
  - Serial Data Control of Frame Frequency for Common and Segment Output Waveforms
  - Serial Data Control of Switching between the Segment Output Pin, PWM Output Pin and General-purpose Output Pin Functions(Max 6 Pin)
  - Built-in OSC Circuit
  - The INHb Pin can Force the Display to the off State.
  - Integrated Voltage Detected type Power on Reset (VDET) circuit
  - No External Component
  - Low Power Consumption Design
- (Note 1) Grade 2

**Package**

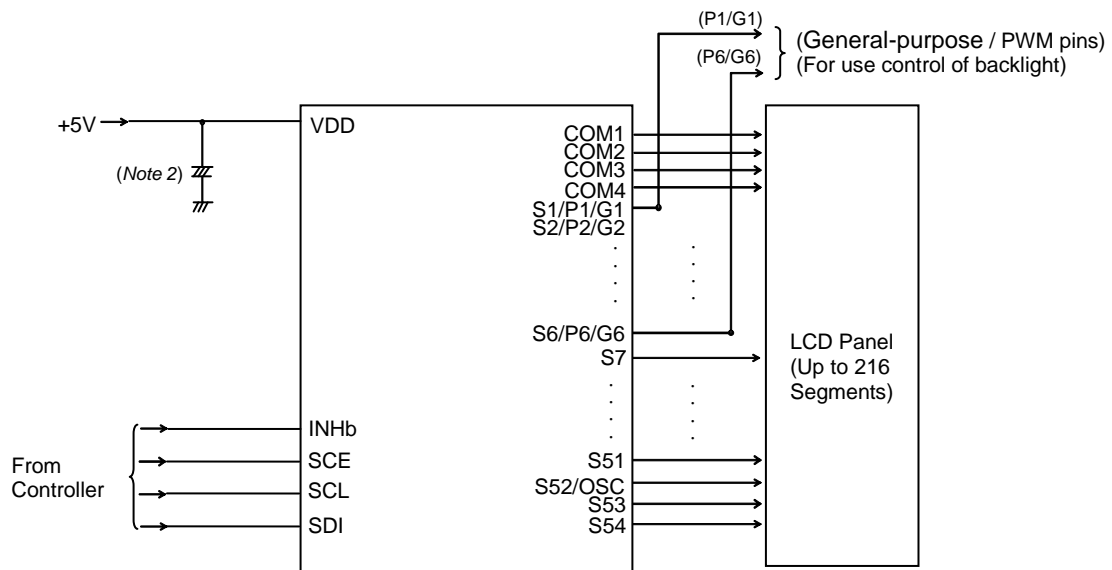
W(Typ) x D(Typ) x H(Max)



**Applications**

- Car Audio, Home Electrical Appliance, Meter Equipment etc.

**Typical Application Circuit**



(Note 2) Insert capacitors between VDD and VSS C ≥ 0.1μF

Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

Block Diagram

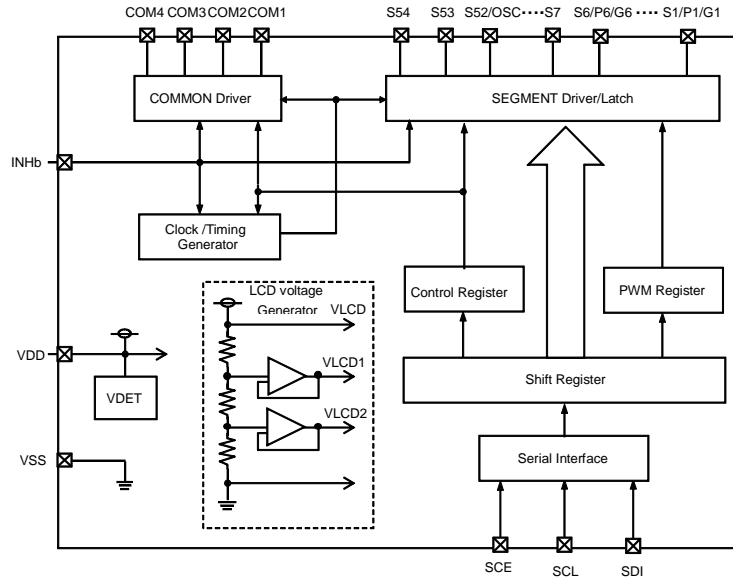


Figure 2. Block Diagram

Pin Arrangement

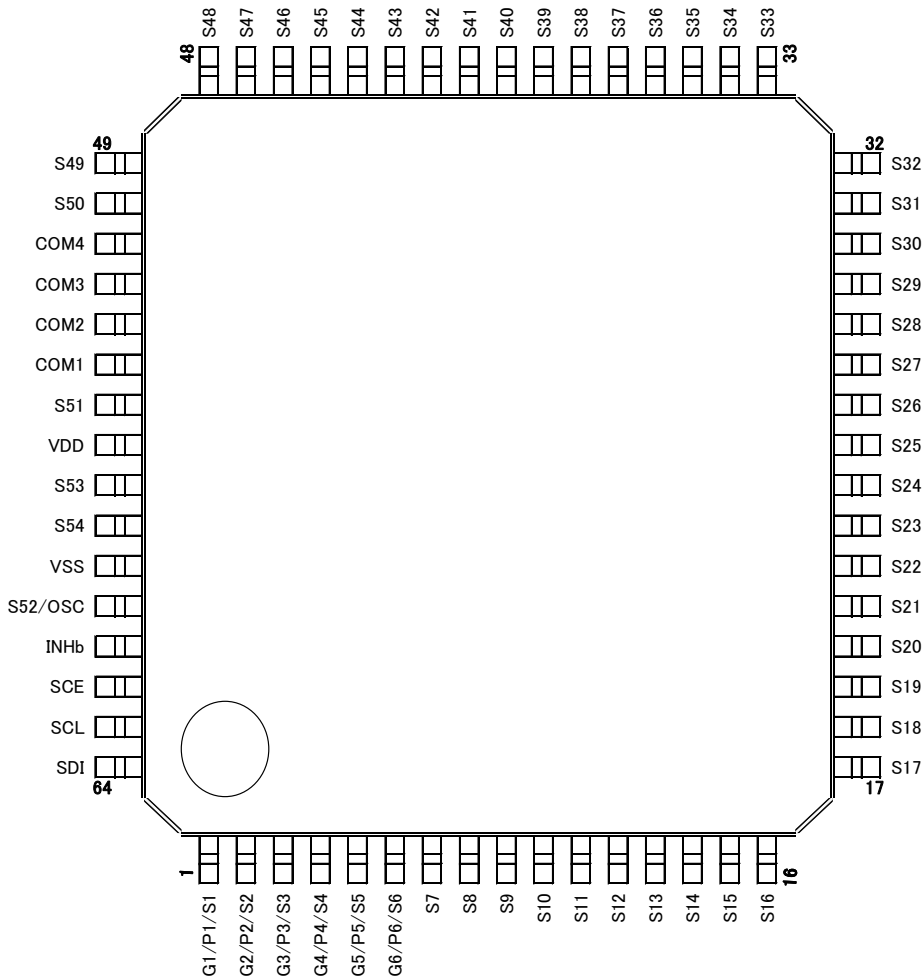


Figure 3. Pin Configuration (TOP VIEW)

**Absolute Maximum Ratings (VSS = 0.0V)**

| Parameter              | Symbol           | Conditions               | Ratings                | Unit |
|------------------------|------------------|--------------------------|------------------------|------|
| Maximum Supply Voltage | VDD              | VDD                      | -0.3 to +7.0           | V    |
| Input Voltage          | V <sub>IN1</sub> | SCE, SCL, SDI, INHb, OSC | -0.3 to +7.0           | V    |
| Allowable Loss         | Pd               | -                        | 1.00 <sup>(Note)</sup> | W    |
| Operating Temperature  | Topr             | -                        | -40 to +105            | °C   |
| Storage Temperature    | Tstg             | -                        | -55 to +125            | °C   |

(Note) When use more than Ta=25°C, subtract 10mW per degree. (Using ROHM standard board)

(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

**Caution1:** Operating the IC over absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

**Recommended Operating Conditions (Ta = -40°C to +105°C, VSS = 0.0V)**

| Parameter      | Symbol | Conditions | Ratings |     |     | Unit |
|----------------|--------|------------|---------|-----|-----|------|
|                |        |            | Min     | Typ | Max |      |
| Supply Voltage | VDD    | VDD        | 2.7     | -   | 6.0 | V    |

**Electrical Characteristics (Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)**

| Parameter                   | Symbol            | Pin                      | Conditions  | Limit          |         |                | Unit |
|-----------------------------|-------------------|--------------------------|---|----------------|---------|----------------|------|
|                             |                   |                          |   | Min            | Typ     | Max            |      |
| Hysteresis                  | V <sub>H</sub>    | SCE, SCL, SDI, INHb, OSC | -   | -              | 0.03VDD | -              | V    |
| Power On Detection Voltage  | V <sub>DET</sub>  | VDD                      | -   | 1.4            | 1.8     | 2.2            | V    |
| “H” Level Input Voltage     | V <sub>IH1</sub>  | SCE, SCL, SDI, INHb, OSC | VDD=4.0V to 6.0V  | 0.4VDD         | -       | VDD            | V    |
|                             | V <sub>IH2</sub>  | SCE, SCL, SDI, INHb, OSC | VDD=2.7V to 4.0V  | 0.8VDD         | -       | VDD            | V    |
| “L” Level Input Voltage     | V <sub>IL1</sub>  | SCE, SCL, SDI, INHb, OSC | -   | 0              | -       | 0.2VDD         | V    |
| “H” Level Input Current     | I <sub>IH1</sub>  | SCE, SCL, SDI, INHb, OSC | V <sub>I</sub> = 6.0V   | -              | -       | 5.0            | μA   |
| “L” Level Input Current     | I <sub>IL1</sub>  | SCE, SCL, SDI, INHb, OSC | V <sub>I</sub> = 0V   | -5.0           | -       | -              | μA   |
| “H” Level Output Voltage    | V <sub>OH1</sub>  | S1 to S54                | I <sub>O</sub> = -20μA  | VDD-0.9        | -       | -              | V    |
|                             | V <sub>OH2</sub>  | COM1 to COM4             | I <sub>O</sub> = -100μA   | VDD-0.9        | -       | -              |      |
|                             | V <sub>OH3</sub>  | P1/G1 to P6/G6           | I <sub>O</sub> = -1mA   | VDD-0.9        | -       | -              |      |
| “L” Level Output Voltage    | V <sub>OL1</sub>  | S1 to S54                | I <sub>O</sub> = 20μA   | -              | -       | 0.9            | V    |
|                             | V <sub>OL2</sub>  | COM1 to COM4             | I <sub>O</sub> = 100μA  | -              | -       | 0.9            |      |
|                             | V <sub>OL3</sub>  | P1/G1 to P6/G6           | I <sub>O</sub> = 1mA  | -              | -       | 0.9            |      |
| Middle Level Output Voltage | V <sub>MID1</sub> | S1 to S54                | 1/2 Bias I <sub>O</sub> = ±20μA                                 | 1/2VDD<br>-0.9 | -       | 1/2VDD<br>+0.9 | V    |
|                             | V <sub>MID2</sub> | COM1 to COM4             | 1/2 Bias I <sub>O</sub> = ±100μA                                | 1/2VDD<br>-0.9 | -       | 1/2VDD<br>+0.9 |      |
|                             | V <sub>MID3</sub> | S1 to S54                | 1/3 Bias I <sub>O</sub> = ±20μA                                 | 2/3VDD<br>-0.9 | -       | 2/3VDD<br>+0.9 |      |
|                             | V <sub>MID4</sub> | S1 to S54                | 1/3 Bias I <sub>O</sub> = ±20μA                                 | 1/3VDD<br>-0.9 | -       | 1/3VDD<br>+0.9 |      |
|                             | V <sub>MID5</sub> | COM1 to COM4             | 1/3 Bias I <sub>O</sub> = ±100μA                                | 2/3VDD<br>-0.9 | -       | 2/3VDD<br>+0.9 |      |
|                             | V <sub>MID6</sub> | COM1 to COM4             | 1/3 Bias I <sub>O</sub> = ±100μA                                | 1/3VDD<br>-0.9 | -       | 1/3VDD<br>+0.9 |      |
| Current Drain               | I <sub>DD1</sub>  | VDD                      | Power-saving mode   | -              | -       | 15             | μA   |
|                             | I <sub>DD2</sub>  | VDD                      | VDD = 5.0V<br>Output open<br>1/2 Bias<br>Frame Frequency = 80Hz | -              | 70      | 150            |      |
|                             | I <sub>DD3</sub>  | VDD                      | VDD = 5.0V<br>Output open<br>1/3 Bias<br>Frame Frequency = 80Hz | -              | 95      | 200            |      |

Oscillation Characteristics (Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

| Parameter                                    | Symbol            | Pin | Conditions                 | Limit |     |     | Unit |
|--|-------------------|-----|----------------------------|-------|-----|-----|------|
|  |                   |     |                            | Min   | Typ | Max |      |
| Oscillator Frequency1                        | f <sub>OSC1</sub> | -   | VDD = 2.7V to 6.0V         | 150   | -   | 360 | kHz  |
| Oscillator Frequency2                        | f <sub>OSC2</sub> |     | VDD = 5.0V                 | 255   | 300 | 345 | kHz  |
| External Clock Frequency <sup>(Note 3)</sup> | f <sub>OSC3</sub> | OSC | External clock mode (OC=1) | 30    | -   | 600 | kHz  |
| External Clock Rise Time                     | t <sub>r</sub>    |     |                            | -     | 160 | -   | ns   |
| External Clock Fall Time                     | t <sub>f</sub>    |     |                            | -     | 160 | -   | ns   |
| External Clock Duty                          | t <sub>DTY</sub>  |     |                            | 30    | 50  | 70  | %    |

(Note 3) Frame frequency is decided external clock and dividing ratio of FC0 to FC2 setting.

[Reference Data]

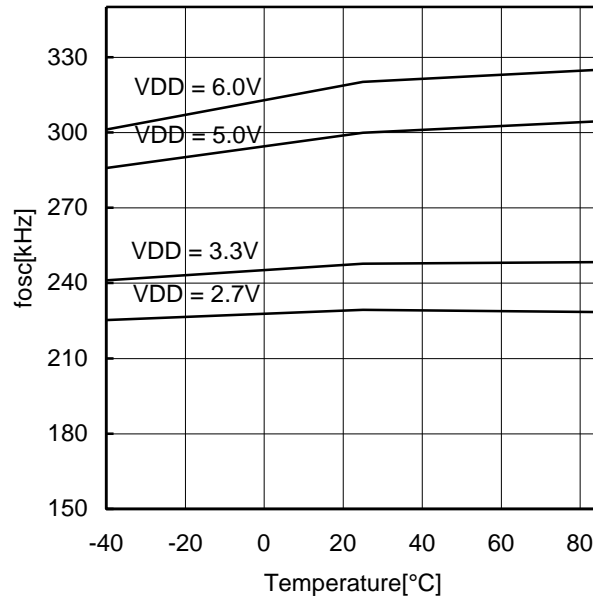
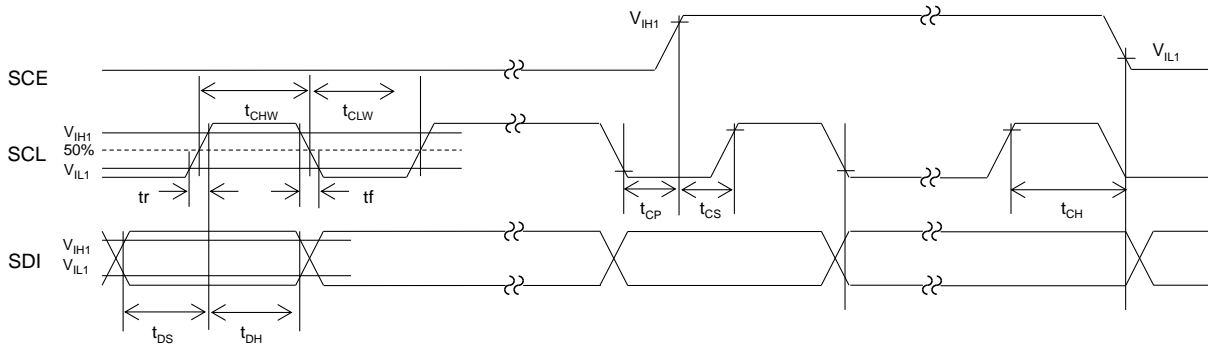


Figure 4. Oscillator Frequency Typical Temperature Characteristics

MPU Interface Characteristics (Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

| Parameter                    | Symbol           | Pin           | Conditions | Limit |     |     | Unit |
|------------------------------|------------------|---------------|------------|-------|-----|-----|------|
|                              |                  |               |            | Min   | Typ | Max |      |
| Data Setup Time              | t <sub>DS</sub>  | SCL, SDI      | -          | 160   | -   | -   | ns   |
| Data Hold Time               | t <sub>DH</sub>  | SCL, SDI      | -          | 160   | -   | -   | ns   |
| SCE Wait Time                | t <sub>CP</sub>  | SCE, SCL      | -          | 160   | -   | -   | ns   |
| SCE Setup Time               | t <sub>CS</sub>  | SCE, SCL      | -          | 160   | -   | -   | ns   |
| SCE Hold Time                | t <sub>CH</sub>  | SCE, SCL      | -          | 160   | -   | -   | ns   |
| High-Level Clock Pulse Width | t <sub>CHW</sub> | SCL           | -          | 160   | -   | -   | ns   |
| Low-Level Clock Pulse Width  | t <sub>CLW</sub> | SCL           | -          | 160   | -   | -   | ns   |
| Rise Time                    | t <sub>r</sub>   | SCE, SCL, SDI | -          | -     | 160 | -   | ns   |
| Fall Time                    | t <sub>f</sub>   | SCE, SCL, SDI | -          | -     | 160 | -   | ns   |
| INH Switching Time           | t <sub>c</sub>   | INHb, SCE     | -          | 10    | -   | -   | µs   |

1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

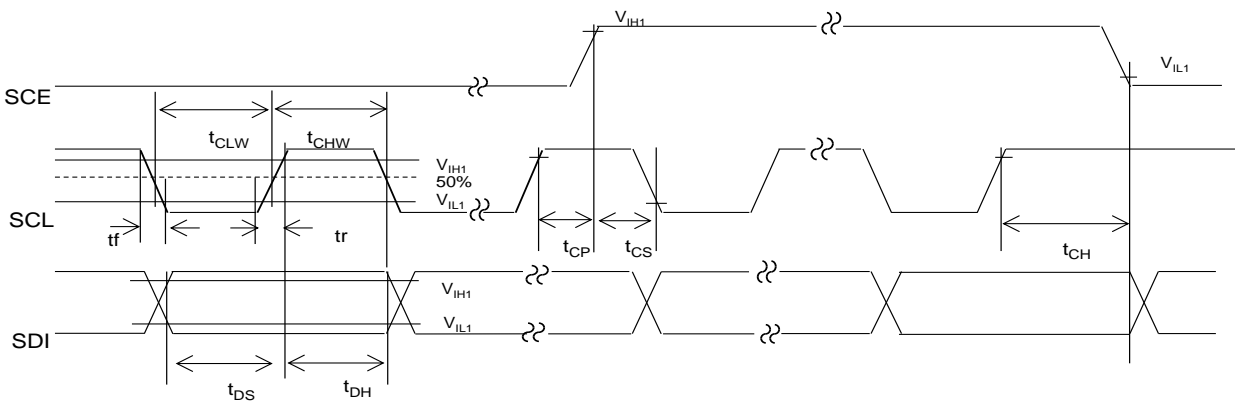


Figure 5. Serial Interface Timing

Pin Description

| Pin Name             | Pin No.             | Function   | Active      | I/O         | Handling when unused |
|----------------------|---------------------|--|-------------|-------------|----------------------|
| S1/P1/G1 to S6/P6/G6 | 1 to 6              | Segment output for displaying the Display Data transferred by serial data input. The S1/P1/G1 to S6/P6/G6 pins can also be used as General-purpose or PWM output when so set up by the control data.   | -           | O           | OPEN                 |
| S7 to S51, S53, S54  | 7 to 50, 55, 57, 58 | Segment output for displaying the Display Data transferred by serial data input.   | -           | O           | OPEN                 |
| COM1 to COM4         | 51 to 54            | Common driver output pins. The frame frequency is fo[Hz].  | -           | O           | OPEN                 |
| S52/OSC              | 60                  | Segment output for displaying the Display Data transferred by serial data input. The S52/OSC pin can be used external clock input pin when set up by the control data.   | -           | I<br>O      | VSS<br>OPEN          |
| SCE<br>SCL<br>SDI    | 62<br>63<br>64      | Serial data transfer inputs. Must be connected to the controller.<br>SCE: Chip enable<br>SCL: Synchronization clock<br>SDI: Transfer data  | H<br>-<br>- | I<br>I<br>I | VSS<br>VSS<br>VSS    |
| INHb                 | 61                  | Display Off control input<br>INHb = low (VSS) ...Display forced off<br>S1/P1/G1 to S6/P6/G6 = low (VSS)<br>S7 to S54 = low (VSS)<br>COM1 to COM4 = low (VSS)<br>Shuts off current to the LCD drive bias voltage generation divider resistors.<br>Stop the internal oscillation circuit.<br>INHb = high (VDD)...Display On<br>However, serial data transfer is possible when the display is forced off. | L           | I           | VDD                  |
| VDD                  | 56                  | Power supply pin for the logic circuit block.<br>A power voltage of 2.7V to 6.0V must be applied to this pin.  | -           | -           | -                    |
| VSS                  | 59                  | Power supply pin. Must be connected to ground.   | -           | -           | -                    |

IO Equivalence Circuit

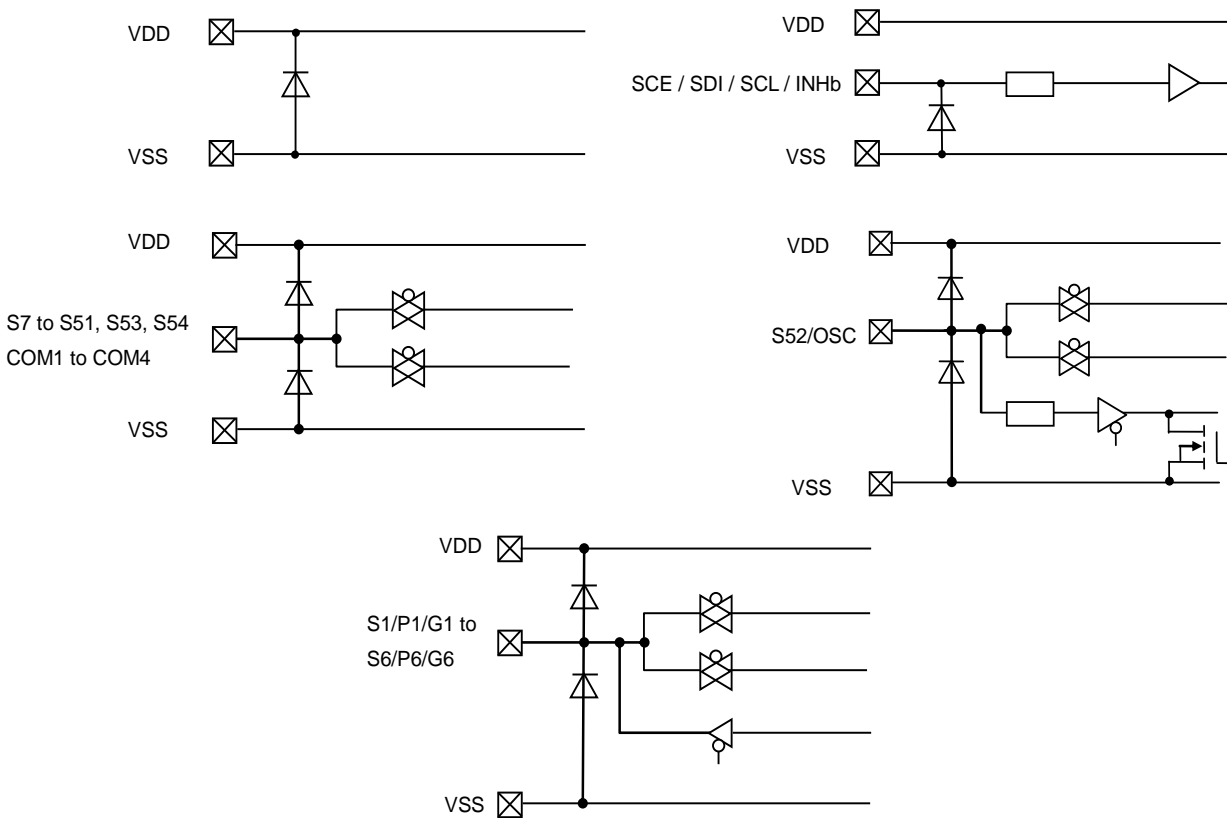


Figure 6. I/O Equivalence Circuit

Serial Data Transfer Formats

1. 1/4 Duty

(1) When SCL is stopped at the low level

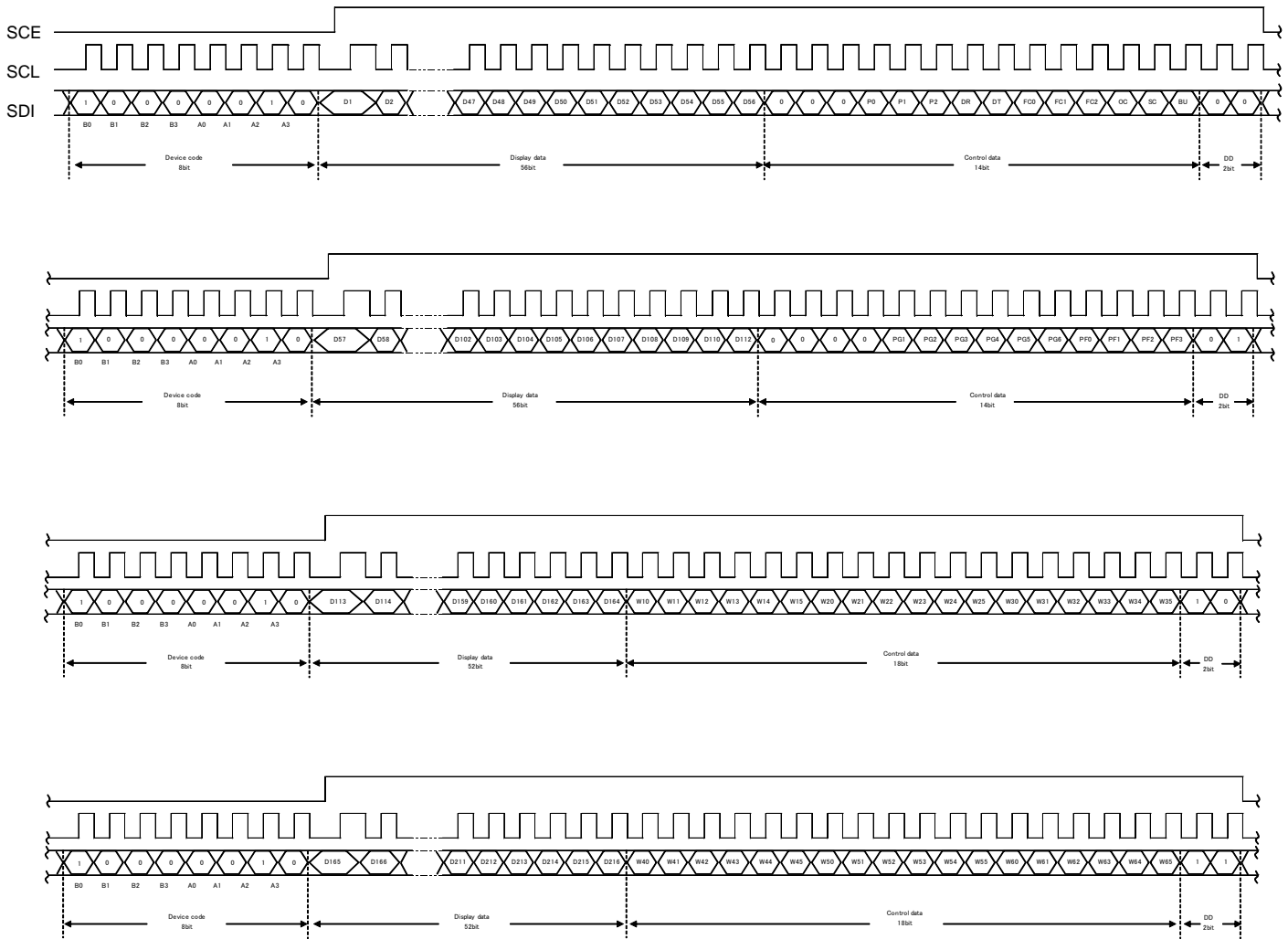


Figure 7. 3-SPI Data Transfer Format

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

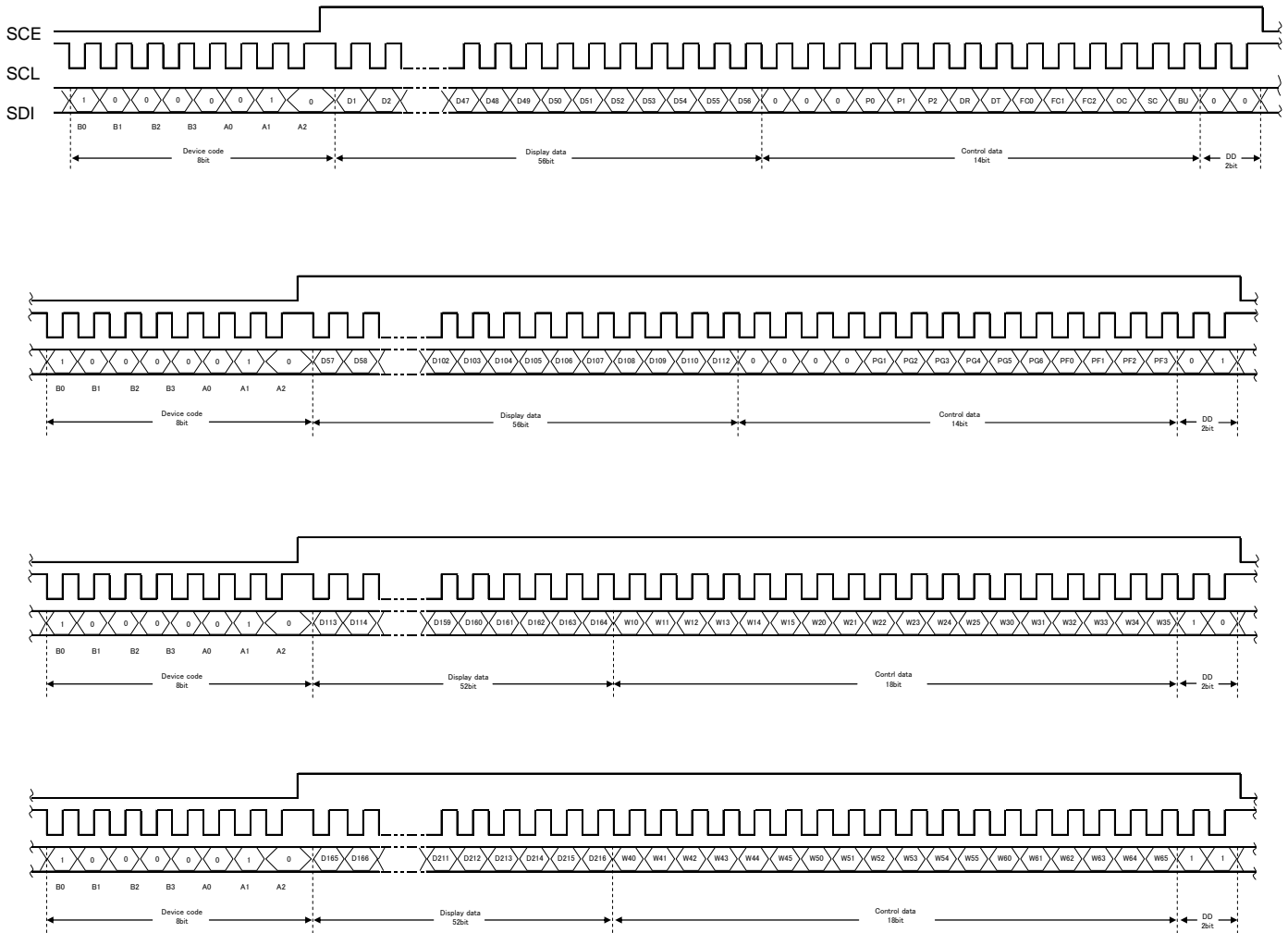


Figure 8. 3-SPI Data Transfer Format

- Device code ..... “41H”
- D1 to D216..... Display Data
- P0 to P2 ..... Segment / PWM / General-purpose output pin switching control data
- DR ..... 1/3 Bias drive or 1/2 Bias drive switching control data
- DT..... 1/4 Duty drive or 1/3 Duty drive switching control data
- FC0 to FC2 ..... Common / Segment output waveform frame frequency switching control data
- OC ..... Internal oscillator operating mode / External clock operating mode switching control data
- SC..... Segment on / off switching control data
- BU..... Normal mode / power-saving mode switching control data
- PG1 to PG6..... PWM / General-purpose output switching control data
- PF0 to PF3..... PWM output frame frequency switching control data
- W10 to W15, W20 to W25, W30 to W35, W40 to W45, W50 to W55, W60 to W65  
..... PWM output duty switching control data
- DD ..... Direction Data



Serial Data Transfer Formats – continued

2. 1/3 Duty

(1) When SCL is stopped at the low level

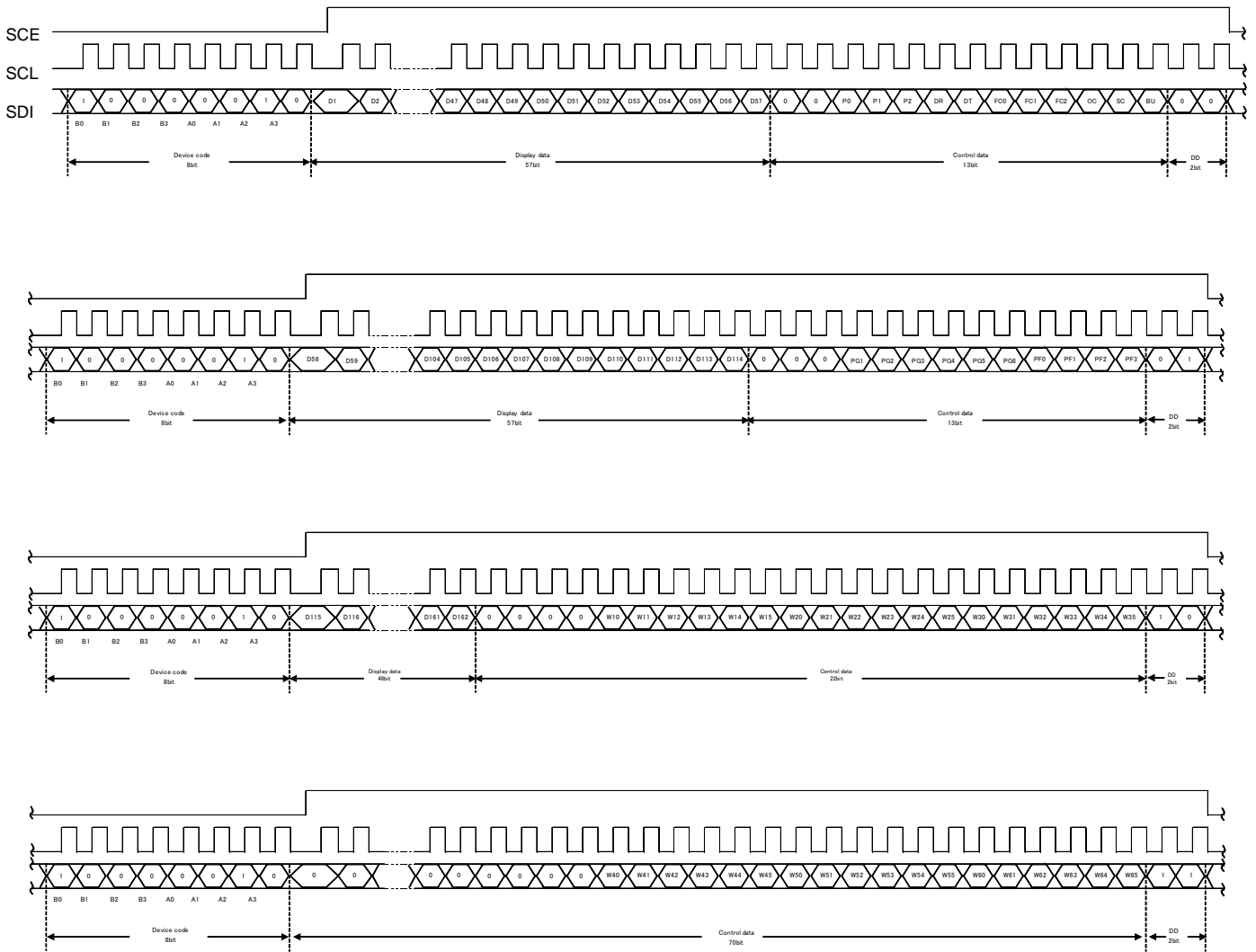


Figure 9. 3-SPI Data Transfer Format

Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level

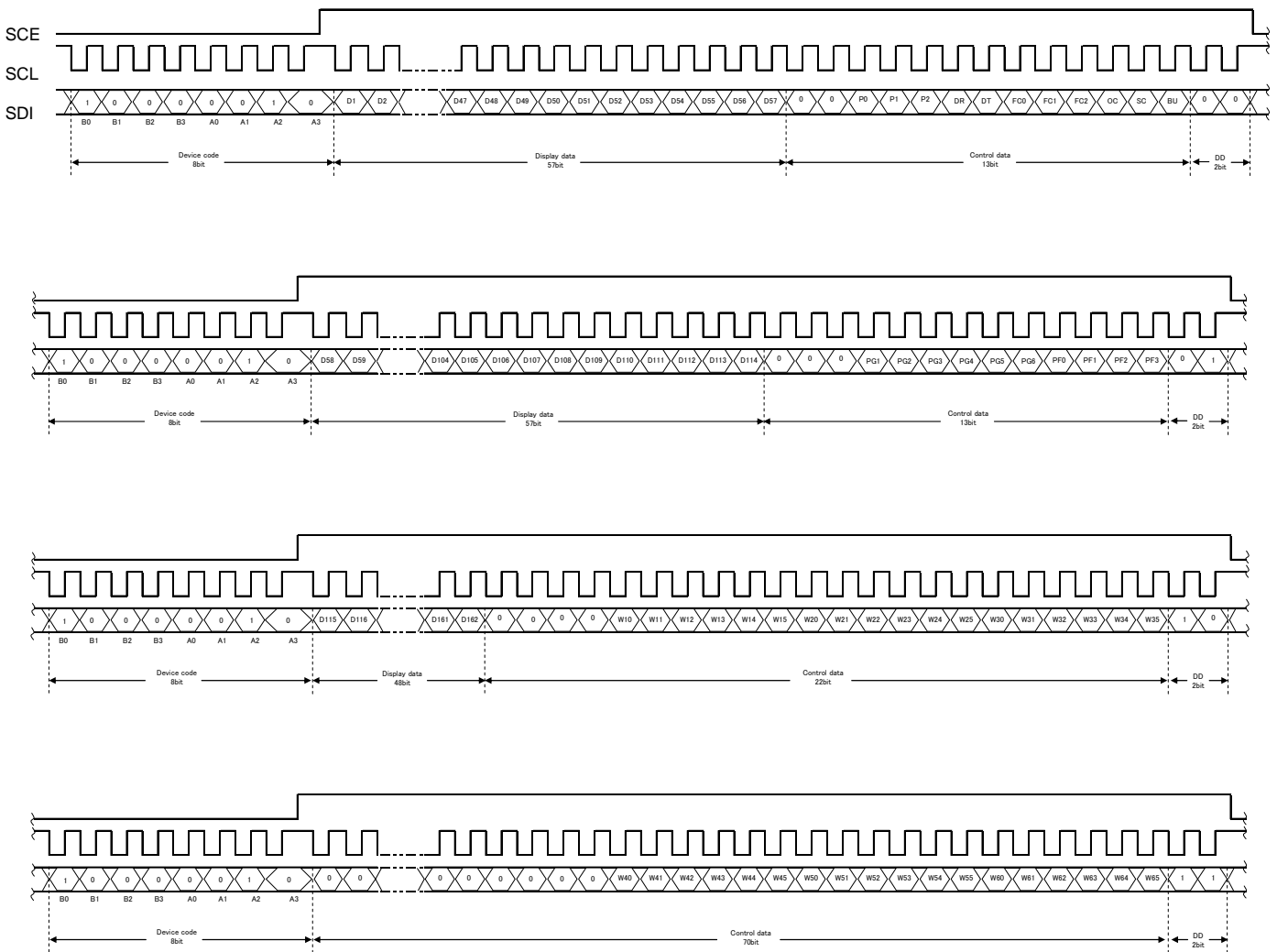


Figure 10. 3-SPI Data Transfer Format

- Device code ..... “41H”
- D1 to D162..... Display Data
- P0 to P2 ..... Segment / PWM / General-purpose output pin switching control data
- DR ..... 1/3 Bias drive or 1/2 Bias drive switching control data
- DT ..... 1/4 Duty drive or 1/3 Duty drive switching control data
- FC0 to FC2 ..... Common / Segment output waveform frame frequency switching control data
- OC ..... Internal oscillator operating mode / External clock operating mode switching control data
- SC..... Segment on / off switching control data
- BU..... Normal mode/power-saving mode switching control data
- PG1 to PG6..... PWM / General-purpose output switching control data
- PF0 to PF3..... PWM output frame frequency switching control data
- W10 to W15, W20 to W25, W30 to W35, W40 to W45, W50 to W55, W60 to W65  
..... PWM output duty switching control data
- DD ..... Direction Data

## Control Data Functions

### 1. P0, P1 and P2: Segment / PWM / General-purpose output pin switching control data

These control bits are used to select the function of the S1/P1/G1 to S6/P6/G6 output pins (Segment Output Pins or PWM Output Pins or General-purpose Output Pins).

Please refer to the table below.

| P0 | P1 | P2 | S1/P1/G1 | S2/P2/G2 | S3/P3/G3 | S4/P4/G4 | S5/P5/G5 | S6/P6/G6 | Reset Condition |
|----|----|----|----------|----------|----------|----------|----------|----------|-----------------|
| 0  | 0  | 0  | S1       | S2       | S3       | S4       | S5       | S6       | ○               |
| 0  | 0  | 1  | P1/G1    | S2       | S3       | S4       | S5       | S6       | -               |
| 0  | 1  | 0  | P1/G1    | P2/G2    | S3       | S4       | S5       | S6       | -               |
| 0  | 1  | 1  | P1/G1    | P2/G2    | P3/G3    | S4       | S5       | S6       | -               |
| 1  | 0  | 0  | P1/G1    | P2/G2    | P3/G3    | P4/G4    | S5       | S6       | -               |
| 1  | 0  | 1  | P1/G1    | P2/G2    | P3/G3    | P4/G4    | P5/G5    | S6       | -               |
| 1  | 1  | 0  | P1/G1    | P2/G2    | P3/G3    | P4/G4    | P5/G5    | P6/G6    | -               |
| 1  | 1  | 1  | S1       | S2       | S3       | S4       | S5       | S6       | -               |

PWM output or General-purpose Output Pin is selected by PGx(x=1 to 6) control data bit.

When the General-purpose Output Pin Function is selected, the correspondence between the output pins and the respective Display Data is given in the table below.

| Output Pins | Corresponding Display Data |               |
|-------------|----------------------------|---------------|
|             | 1/4 Duty Mode              | 1/3 Duty Mode |
| S1/P1/G1    | D1                         | D1            |
| S2/P2/G2    | D5                         | D4            |
| S3/P3/G3    | D9                         | D7            |
| S4/P4/G4    | D13                        | D10           |
| S5/P5/G5    | D17                        | D13           |
| S6/P6/G6    | D21                        | D16           |

When the General-purpose Output Pin Function is selected, the respective output pin outputs a "HIGH" level when its corresponding display data is set to "1". Likewise, it will output a "LOW" level, if its corresponding display data is set to "0". For example, S4/P4/G4 is used as a General-purpose Output Pin in case of 1/4 Duty, if its corresponding Display Data – D13 is set to "1", then S4/P4/G4 will output "HIGH" level. Likewise, if D13 is set to "0", then S4/P4/G4 will output "LOW" level.

### 2. DR: 1/3 Bias drive or 1/2 Bias drive switching control data

This control data bit selects either 1/3 Bias drive or 1/2 Bias drive.

| DR | Bias Drive Scheme | Reset Condition |
|----|-------------------|-----------------|
| 0  | 1/3 Bias drive    | ○               |
| 1  | 1/2 Bias drive    | -               |

### 3. DT: 1/4 Duty drive or 1/3 Duty drive switching control data

This control data bit selects either 1/4 Duty drive or 1/3 Duty drive.

| DT | Duty Drive Scheme | Reset Condition |
|----|-------------------|-----------------|
| 0  | 1/4 Duty drive    | ○               |
| 1  | 1/3 Duty drive    | -               |

### 4. FC0, FC1 and FC2: Frame frequency switching control data

These control data bits set the frame frequency for common and segment output waveforms.

| FC0 | FC1 | FC2 | Frame Frequency fo(Hz) | Reset Condition |
|-----|-----|-----|------------------------|-----------------|
| 0   | 0   | 0   | fosc/6144              | ○               |
| 0   | 0   | 1   | fosc/5376              | -               |
| 0   | 1   | 0   | fosc/4608              | -               |
| 0   | 1   | 1   | fosc/3840              | -               |
| 1   | 0   | 0   | fosc/3072              | -               |
| 1   | 0   | 1   | fosc/2304              | -               |
| 1   | 1   | 0   | fosc/1920              | -               |
| 1   | 1   | 1   | fosc/1536              | -               |

(Note) fosc: Internal oscillation frequency (300kHz Typ)

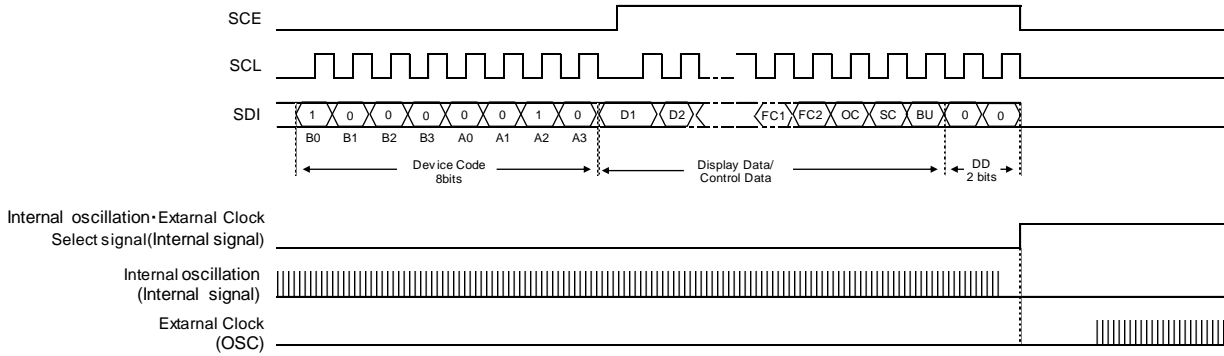
**Control Data Functions – continued**

**5. OC: Internal oscillator operating mode / External clock operating mode switching control data**

| OC | Operating Mode      | In/Out Pin(S52/OSC) Status | Reset Condition |
|----|---------------------|----------------------------|-----------------|
| 0  | Internal oscillator | S52 (segment output)       | ○               |
| 1  | External Clock      | OSC (clock input)          | -               |

<External Clock input timing function>

Internal oscillation / external clock select signal behavior is below.  
Input external clock after serial data sending.



**6. SC: Segment on/off switching control data**

This control data bit controls the on/off state of the segments.

| SC | Display State | Reset Condition |
|----|---------------|-----------------|
| 0  | On            | -               |
| 1  | Off           | ○               |

Note that when the segments are turned off by setting SC to “1”, the segments are turned off by outputting segment off waveforms from the segment output pins.

**7. BU: Normal mode / Power-saving mode switching control data**

This control data bit selects either normal mode or power-saving mode.

| BU | Mode              | Reset Condition |
|----|-------------------|-----------------|
| 0  | Normal Mode       | -               |
| 1  | Power-saving Mode | ○               |

Power-saving mode status: S1/P1/G1 to S6/P6/G6 = active only General-purpose output  
 S7 to S54 = low(VSS)  
 COM1 to COM4 = low(VSS)  
 Shut off current to the LCD drive bias voltage generation circuit  
 Stop the Internal oscillation circuit  
 However, serial data transfer is possible when Power-saving mode.

Control Data Functions – continued

8. PG1, PG2, PG3, PG4, PG5 and PG6: PWM / General-purpose output switching control data

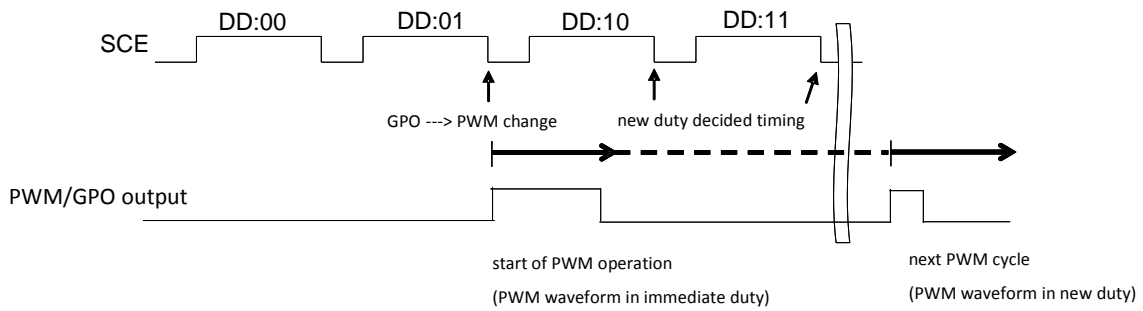
This control data bit select either PWM output or General-purpose output of Sx/Px/Gx pins.(x=1 to 6)

| PGx(x=1 to 6) | Mode                   | Reset Condition |
|---------------|------------------------|-----------------|
| 0             | PWM output             | ○               |
| 1             | General-purpose output | -               |

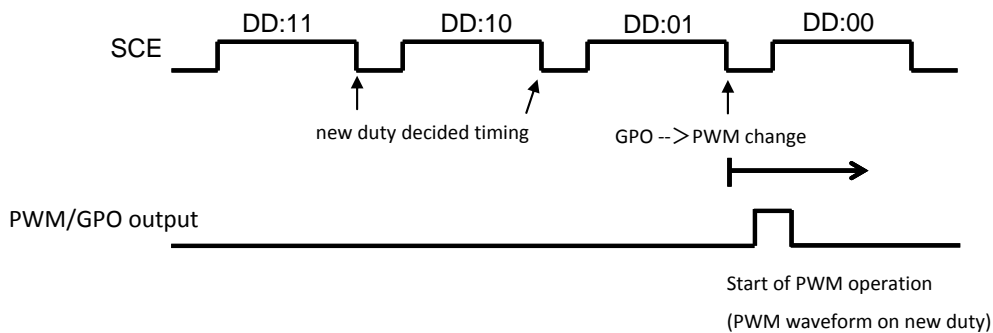
[PWM<->GPO Changing function]

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD:01 during GPO ----> PWM change.
- Please take care of reflect timing of new duty setting of DD:10, DD:11 is from the next PWM.



In order to avoid this operation, please input commands reversely as below.



## Control Data Functions – continued

## 9. PF0, PF1, PF2 and PF3: PWM output frame frequency switching control data

These control data bits set the frame frequency for PWM output.

| PF0 | PF1 | PF2 | PF3 | PWM Output Frame Frequency fp(Hz) | Reset Condition |
|-----|-----|-----|-----|-----------------------------------|-----------------|
| 0   | 0   | 0   | 0   | $f_{osc}/2048$                    | ○               |
| 0   | 0   | 0   | 1   | $f_{osc}/1920$                    | -               |
| 0   | 0   | 1   | 0   | $f_{osc}/1792$                    | -               |
| 0   | 0   | 1   | 1   | $f_{osc}/1664$                    | -               |
| 0   | 1   | 0   | 0   | $f_{osc}/1536$                    | -               |
| 0   | 1   | 0   | 1   | $f_{osc}/1408$                    | -               |
| 0   | 1   | 1   | 0   | $f_{osc}/1280$                    | -               |
| 0   | 1   | 1   | 1   | $f_{osc}/1152$                    | -               |
| 1   | 0   | 0   | 0   | $f_{osc}/1024$                    | -               |
| 1   | 0   | 0   | 1   | $f_{osc}/896$                     | -               |
| 1   | 0   | 1   | 0   | $f_{osc}/768$                     | -               |
| 1   | 0   | 1   | 1   | $f_{osc}/640$                     | -               |
| 1   | 1   | 0   | 0   | $f_{osc}/512$                     | -               |
| 1   | 1   | 0   | 1   | $f_{osc}/384$                     | -               |
| 1   | 1   | 1   | 0   | $f_{osc}/256$                     | -               |
| 1   | 1   | 1   | 1   | $f_{osc}/128$                     | -               |

10. W10 to W15, W20 to W25, W30 to W35, W40 to W45, W50 to W55 and W60 to W65<sup>(Note)</sup>: PWM output duty switching control data

These control data bits set the high level pulse width for PWM output.

| Wn0 | Wn1 | Wn2 | Wn3 | Wn4 | Wn5 | PWM Duty             | Reset Condition |
|-----|-----|-----|-----|-----|-----|----------------------|-----------------|
| 0   | 0   | 0   | 0   | 0   | 0   | $(1/64) \times T_p$  | ○               |
| 1   | 0   | 0   | 0   | 0   | 0   | $(2/64) \times T_p$  | -               |
| 0   | 1   | 0   | 0   | 0   | 0   | $(3/64) \times T_p$  | -               |
| 1   | 1   | 0   | 0   | 0   | 0   | $(4/64) \times T_p$  | -               |
| 0   | 0   | 1   | 0   | 0   | 0   | $(5/64) \times T_p$  | -               |
| 1   | 0   | 1   | 0   | 0   | 0   | $(6/64) \times T_p$  | -               |
| 0   | 1   | 1   | 0   | 0   | 0   | $(7/64) \times T_p$  | -               |
| 1   | 1   | 1   | 0   | 0   | 0   | $(8/64) \times T_p$  | -               |
| 0   | 0   | 0   | 1   | 0   | 0   | $(9/64) \times T_p$  | -               |
| 1   | 0   | 0   | 1   | 0   | 0   | $(10/64) \times T_p$ | -               |
| 0   | 1   | 0   | 1   | 0   | 0   | $(11/64) \times T_p$ | -               |
| 1   | 1   | 0   | 1   | 0   | 0   | $(12/64) \times T_p$ | -               |
| 0   | 0   | 1   | 1   | 0   | 0   | $(13/64) \times T_p$ | -               |
| 1   | 0   | 1   | 1   | 0   | 0   | $(14/64) \times T_p$ | -               |
| 0   | 1   | 1   | 1   | 0   | 0   | $(15/64) \times T_p$ | -               |
| ... | ... | ... | ... | ... | ... | ...                  | -               |
| 1   | 0   | 0   | 0   | 1   | 1   | $(50/64) \times T_p$ | -               |
| 0   | 1   | 0   | 0   | 1   | 1   | $(51/64) \times T_p$ | -               |
| 1   | 1   | 0   | 0   | 1   | 1   | $(52/64) \times T_p$ | -               |
| 0   | 0   | 1   | 0   | 1   | 1   | $(53/64) \times T_p$ | -               |
| 1   | 0   | 1   | 0   | 1   | 1   | $(54/64) \times T_p$ | -               |
| 0   | 1   | 1   | 0   | 1   | 1   | $(55/64) \times T_p$ | -               |
| 1   | 1   | 1   | 0   | 1   | 1   | $(56/64) \times T_p$ | -               |
| 0   | 0   | 0   | 1   | 1   | 1   | $(57/64) \times T_p$ | -               |
| 1   | 0   | 0   | 1   | 1   | 1   | $(58/64) \times T_p$ | -               |
| 0   | 1   | 0   | 1   | 1   | 1   | $(59/64) \times T_p$ | -               |
| 1   | 1   | 0   | 1   | 1   | 1   | $(60/64) \times T_p$ | -               |
| 0   | 0   | 1   | 1   | 1   | 1   | $(61/64) \times T_p$ | -               |
| 1   | 0   | 1   | 1   | 1   | 1   | $(62/64) \times T_p$ | -               |
| 0   | 1   | 1   | 1   | 1   | 1   | $(63/64) \times T_p$ | -               |
| 1   | 1   | 1   | 1   | 1   | 1   | $(64/64) \times T_p$ | -               |

(Note) W10 to W15: S1/P1/G1 PWM duty data  
 W20 to W25: S2/P2/G2 PWM duty data  
 W30 to W35: S3/P3/G3 PWM duty data  
 W40 to W45: S4/P4/G4 PWM duty data  
 W50 to W55: S5/P5/G5 PWM duty data  
 W60 to W65: S6/P6/G6 PWM duty data

n = 1 to 6  
 $T_p = 1/f_p$

## Display Data and Output Pin Correspondence

## 1. 1/4 Duty

| Output Pin <sup>(Note)</sup> | COM1 | COM2 | COM3 | COM4 |
|------------------------------|------|------|------|------|
| S1/P1/G1                     | D1   | D2   | D3   | D4   |
| S2/P2/G2                     | D5   | D6   | D7   | D8   |
| S3/P3/G3                     | D9   | D10  | D11  | D12  |
| S4/P4/G4                     | D13  | D14  | D15  | D16  |
| S5/P5/G5                     | D17  | D18  | D19  | D20  |
| S6/P6/G6                     | D21  | D22  | D23  | D24  |
| S7                           | D25  | D26  | D27  | D28  |
| S8                           | D29  | D30  | D31  | D32  |
| S9                           | D33  | D34  | D35  | D36  |
| S10                          | D37  | D38  | D39  | D40  |
| S11                          | D41  | D42  | D43  | D44  |
| S12                          | D45  | D46  | D47  | D48  |
| S13                          | D49  | D50  | D51  | D52  |
| S14                          | D53  | D54  | D55  | D56  |
| S15                          | D57  | D58  | D59  | D60  |
| S16                          | D61  | D62  | D63  | D64  |
| S17                          | D65  | D66  | D67  | D68  |
| S18                          | D69  | D70  | D71  | D72  |
| S19                          | D73  | D74  | D75  | D76  |
| S20                          | D77  | D78  | D79  | D80  |
| S21                          | D81  | D82  | D83  | D84  |
| S22                          | D85  | D86  | D87  | D88  |
| S23                          | D89  | D90  | D91  | D92  |
| S24                          | D93  | D94  | D95  | D96  |
| S25                          | D97  | D98  | D99  | D100 |
| S26                          | D101 | D102 | D103 | D104 |
| S27                          | D105 | D106 | D107 | D108 |
| S28                          | D109 | D110 | D111 | D112 |
| S29                          | D113 | D114 | D115 | D116 |
| S30                          | D117 | D118 | D119 | D120 |
| S31                          | D121 | D122 | D123 | D124 |
| S32                          | D125 | D126 | D127 | D128 |
| S33                          | D129 | D130 | D131 | D132 |
| S34                          | D133 | D134 | D135 | D136 |
| S35                          | D137 | D138 | D139 | D140 |
| S36                          | D141 | D142 | D143 | D144 |
| S37                          | D145 | D146 | D147 | D148 |
| S38                          | D149 | D150 | D151 | D152 |
| S39                          | D153 | D154 | D155 | D156 |
| S40                          | D157 | D158 | D159 | D160 |
| S41                          | D161 | D162 | D163 | D164 |
| S42                          | D165 | D166 | D167 | D168 |
| S43                          | D169 | D170 | D171 | D172 |
| S44                          | D173 | D174 | D175 | D176 |
| S45                          | D177 | D178 | D179 | D180 |
| S46                          | D181 | D182 | D183 | D184 |
| S47                          | D185 | D186 | D187 | D188 |
| S48                          | D189 | D190 | D191 | D192 |
| S49                          | D193 | D194 | D195 | D196 |
| S50                          | D197 | D198 | D199 | D200 |
| S51                          | D201 | D202 | D203 | D204 |
| S52                          | D205 | D206 | D207 | D208 |
| S53                          | D209 | D210 | D211 | D212 |
| S54                          | D213 | D214 | D215 | D216 |

(Note) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S6/P6/G6.

**Display Data and Output Pin Correspondence – continued**

To illustrate further, the states of the S21 output pin is given in the table below.

| Display Data |     |     |     | State of S21 Output Pin                                    |
|--------------|-----|-----|-----|--|
| D81          | D82 | D83 | D84 |  |
| 0            | 0   | 0   | 0   | LCD Segments corresponding to COM1 to COM4 are OFF.        |
| 0            | 0   | 0   | 1   | LCD Segment corresponding to COM4 is ON.                   |
| 0            | 0   | 1   | 0   | LCD Segment corresponding to COM3 is ON.                   |
| 0            | 0   | 1   | 1   | LCD Segments corresponding to COM3 and COM4 are ON.        |
| 0            | 1   | 0   | 0   | LCD Segment corresponding to COM2 is ON.                   |
| 0            | 1   | 0   | 1   | LCD Segments corresponding to COM2 and COM4 are ON.        |
| 0            | 1   | 1   | 0   | LCD Segments corresponding to COM2 and COM3 are ON.        |
| 0            | 1   | 1   | 1   | LCD Segments corresponding to COM2, COM3 and COM4 are ON.  |
| 1            | 0   | 0   | 0   | LCD Segment corresponding to COM1 is ON.                   |
| 1            | 0   | 0   | 1   | LCD Segments corresponding to COM1 and COM4 are ON.        |
| 1            | 0   | 1   | 0   | LCD Segments corresponding to COM1 and COM3 are ON.        |
| 1            | 0   | 1   | 1   | LCD Segments corresponding to COM1, COM3 and COM4 are ON.  |
| 1            | 1   | 0   | 0   | LCD Segments corresponding to COM1 and COM2 are ON.        |
| 1            | 1   | 0   | 1   | LCD Segments corresponding to COM1, COM2, and COM4 are ON. |
| 1            | 1   | 1   | 0   | LCD Segments corresponding to COM1, COM2, and COM3 are ON. |
| 1            | 1   | 1   | 1   | LCD Segments corresponding to COM1 to COM 4 are ON.        |



## Display Data and Output Pin Correspondence – continued

## 2. 1/3 Duty

| Output Pin <sup>(Note)</sup> | COM1 | COM2 | COM3 |
|------------------------------|------|------|------|
| S1/P1/G1                     | D1   | D2   | D3   |
| S2/P2/G2                     | D4   | D5   | D6   |
| S3/P3/G3                     | D7   | D8   | D9   |
| S4/P4/G4                     | D10  | D11  | D12  |
| S5/P5/G5                     | D13  | D14  | D15  |
| S6/P6/G6                     | D16  | D17  | D18  |
| S7                           | D19  | D20  | D21  |
| S8                           | D22  | D23  | D24  |
| S9                           | D25  | D26  | D27  |
| S10                          | D28  | D29  | D30  |
| S11                          | D31  | D32  | D33  |
| S12                          | D34  | D35  | D36  |
| S13                          | D37  | D38  | D39  |
| S14                          | D40  | D41  | D42  |
| S15                          | D43  | D44  | D45  |
| S16                          | D46  | D47  | D48  |
| S17                          | D49  | D50  | D51  |
| S18                          | D52  | D53  | D54  |
| S19                          | D55  | D56  | D57  |
| S20                          | D58  | D59  | D60  |
| S21                          | D61  | D62  | D63  |
| S22                          | D64  | D65  | D66  |
| S23                          | D67  | D68  | D69  |
| S24                          | D70  | D71  | D72  |
| S25                          | D73  | D74  | D75  |
| S26                          | D76  | D77  | D78  |
| S27                          | D79  | D80  | D81  |
| S28                          | D82  | D83  | D84  |
| S29                          | D85  | D86  | D87  |
| S30                          | D88  | D89  | D90  |
| S31                          | D91  | D92  | D93  |
| S32                          | D94  | D95  | D96  |
| S33                          | D97  | D98  | D99  |
| S34                          | D100 | D101 | D102 |
| S35                          | D103 | D104 | D105 |
| S36                          | D106 | D107 | D108 |
| S37                          | D109 | D110 | D111 |
| S38                          | D112 | D113 | D114 |
| S39                          | D115 | D116 | D117 |
| S40                          | D118 | D119 | D120 |
| S41                          | D121 | D122 | D123 |
| S42                          | D124 | D125 | D126 |
| S43                          | D127 | D128 | D129 |
| S44                          | D130 | D131 | D132 |
| S45                          | D133 | D134 | D135 |
| S46                          | D136 | D137 | D138 |
| S47                          | D139 | D140 | D141 |
| S48                          | D142 | D143 | D144 |
| S49                          | D145 | D146 | D147 |
| S50                          | D148 | D149 | D150 |
| S51                          | D151 | D152 | D153 |
| S52                          | D154 | D155 | D156 |
| S53                          | D157 | D158 | D159 |
| S54                          | D160 | D161 | D162 |

(Note) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S6/P6/G6.

**Display Data and Output Pin Correspondence – continued**

To illustrate further, the states of the S21 output pin is given in the table below.

| Display Data |     |     | State of S21 Output Pin                             |
|--------------|-----|-----|---|
| D61          | D62 | D63 |   |
| 0            | 0   | 0   | LCD Segments corresponding to COM1 to COM3 are OFF. |
| 0            | 0   | 1   | LCD Segment corresponding to COM3 is ON.            |
| 0            | 1   | 0   | LCD Segment corresponding to COM2 is ON.            |
| 0            | 1   | 1   | LCD Segments corresponding to COM2 and COM3 are ON. |
| 1            | 0   | 0   | LCD Segment corresponding to COM1 is ON.            |
| 1            | 0   | 1   | LCD Segments corresponding to COM1 and COM3 are ON. |
| 1            | 1   | 0   | LCD Segments corresponding to COM1 and COM2 are ON. |
| 1            | 1   | 1   | LCD Segments corresponding to COM1 to COM3 are ON.  |

LCD Driving Waveforms  
(1/4 Duty 1/3 Bias Drive Scheme)

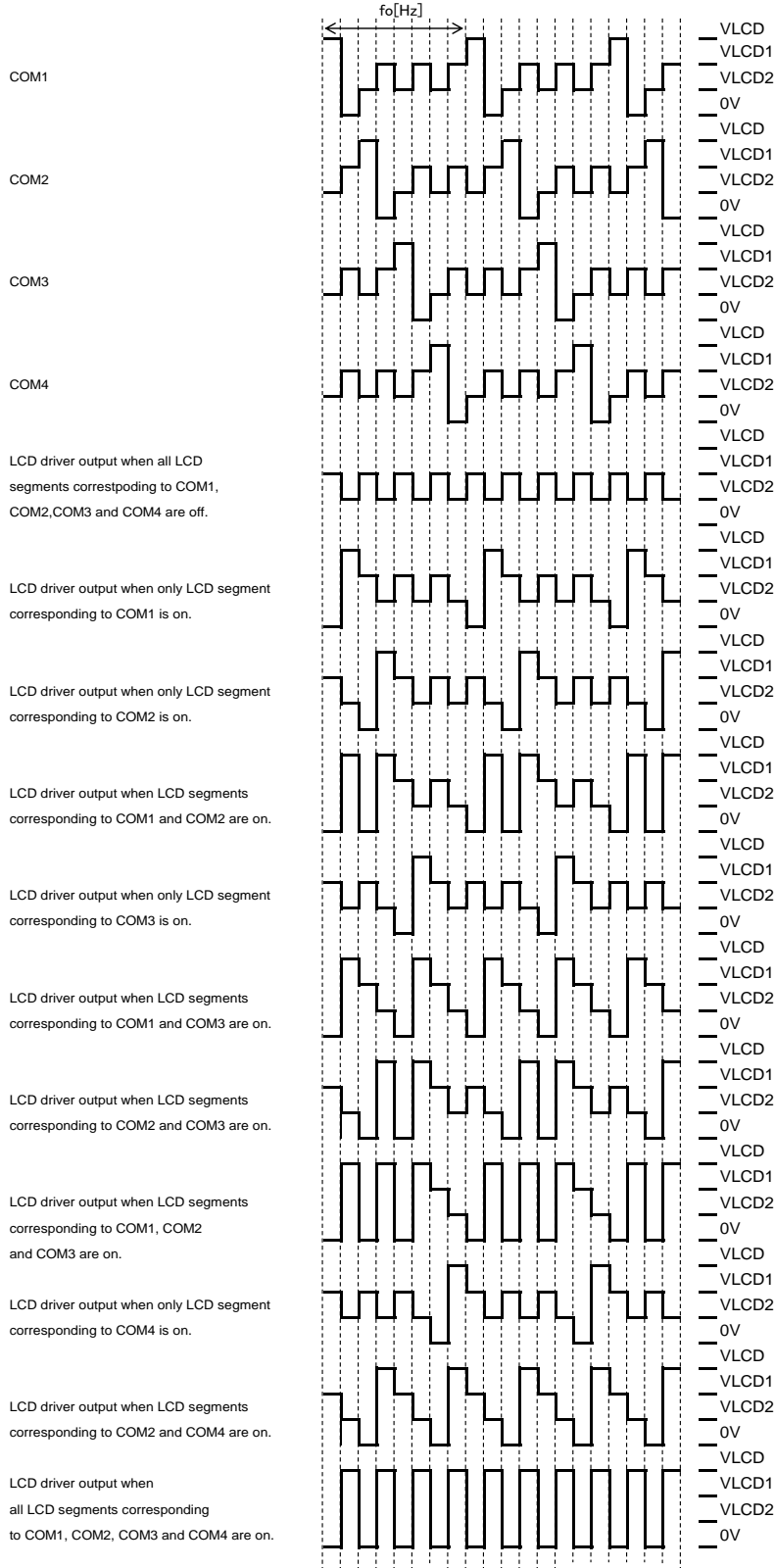


Figure 11. LCD Waveform (1/4 Duty, 1/3 Bias)

**LCD Driving Waveforms– continued**  
**(1/4 Duty 1/2 Bias Drive Scheme)**

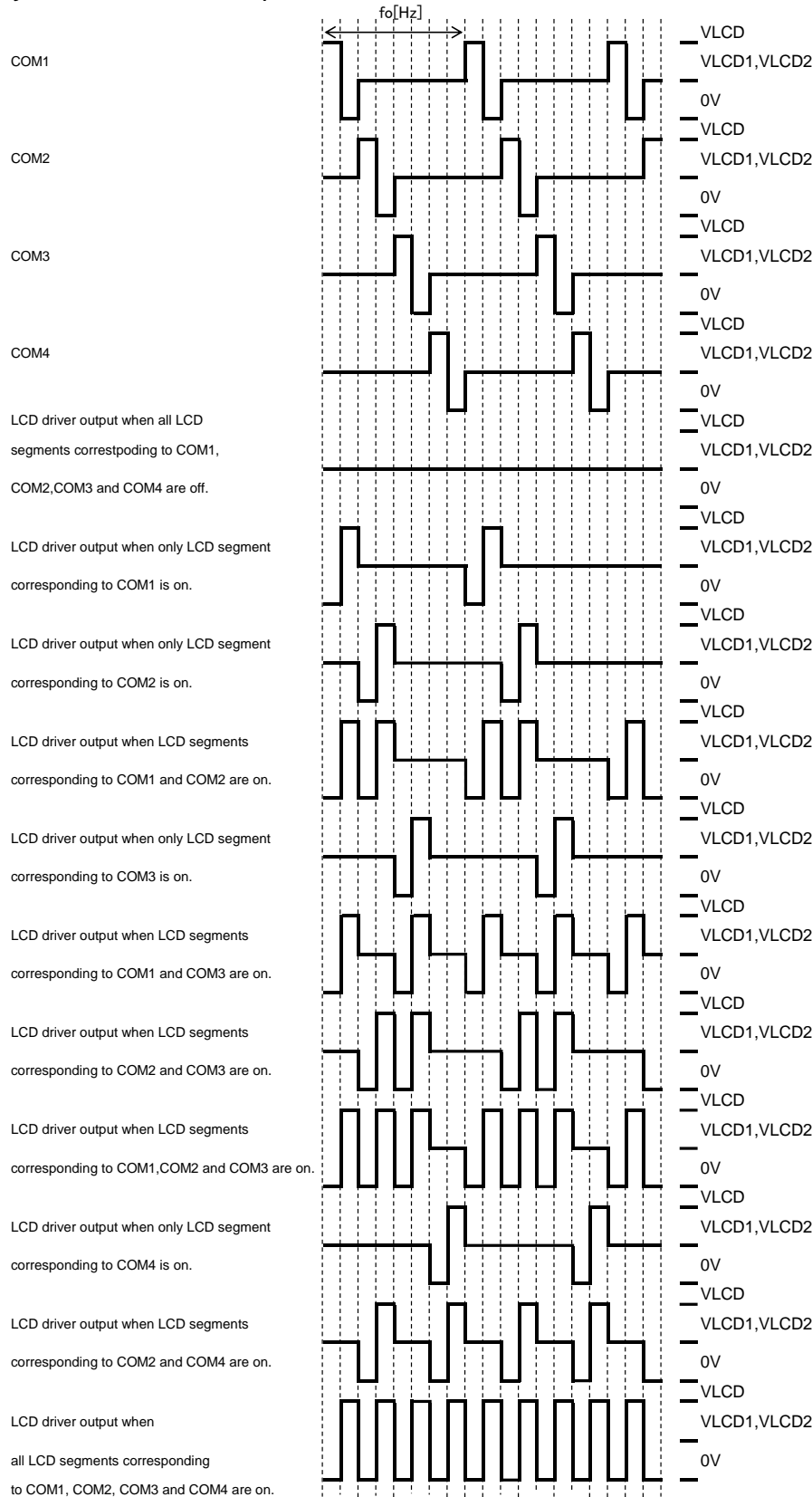


Figure 12. LCD Waveform (1/4 Duty, 1/2 Bias)

LCD Driving Waveforms– continued  
(1/3 Duty 1/3 Bias Drive Scheme)

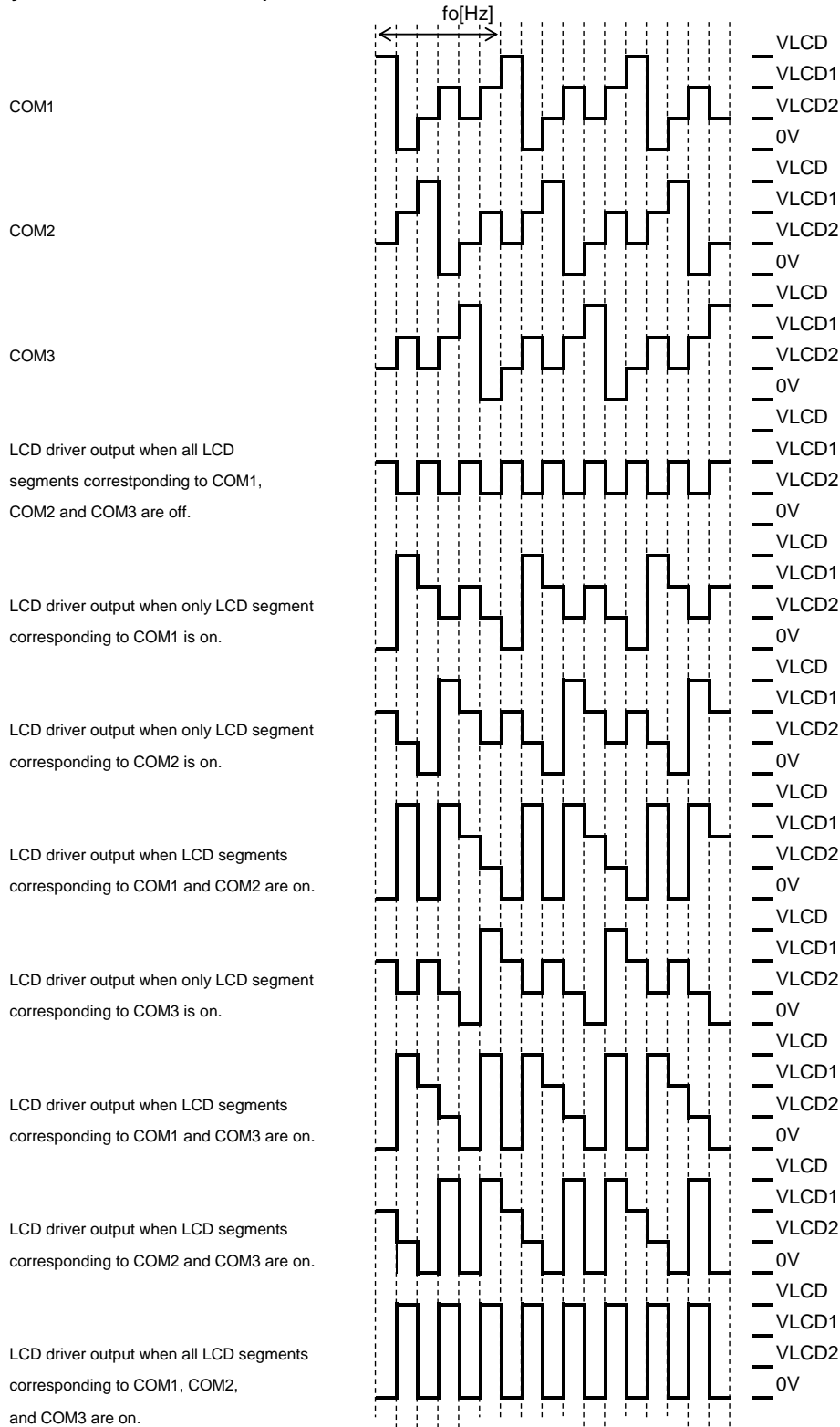


Figure 13. LCD Waveform (1/3 Duty, 1/3 Bias) <sup>(Note)</sup>

(Note) COM4 function is same as COM1 at 1/3 Duty.

LCD Driving Waveforms– continued  
(1/3 Duty 1/2 Bias Drive Scheme)

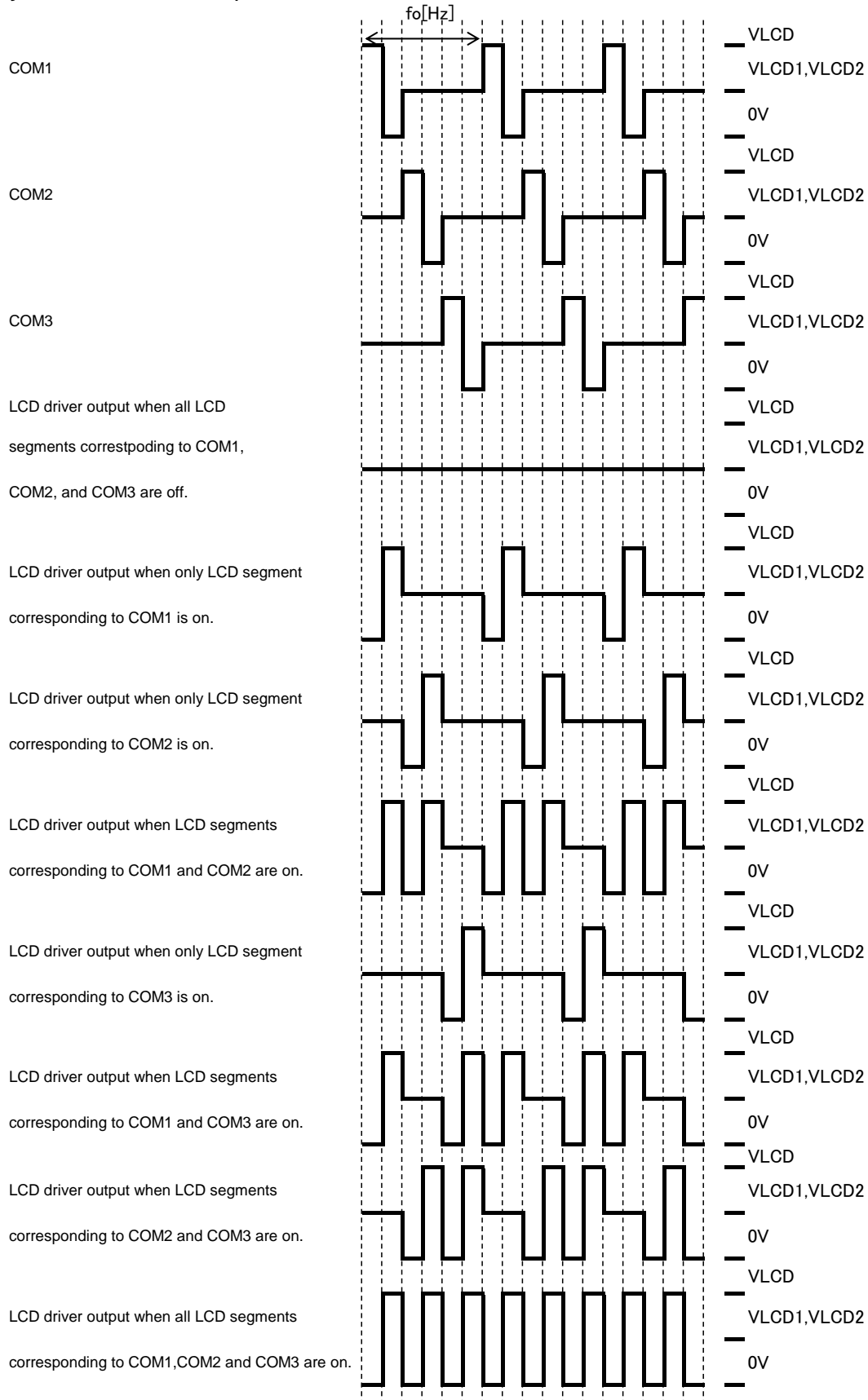


Figure 14. LCD Waveform (1/3 Duty, 1/2 Bias) <sup>(Note)</sup>

(Note) COM4 function is same as COM1 at 1/3 Duty.

**The INHb Pin and Display Control**

Since the IC internal data (the Display Data D1 to D216 and the control data) is undefined when power is first applied, applications should set the INHb pin low at the same time as power is applied to turn off the display (This sets the S1/P1/G1 to S6/P6/G6, S7 to S54, COM1 to COM4 to the VSS level.) and during this period send serial data from the controller. The controller should then set the INHb pin high after the data transfer has completed. This procedure prevents meaningless displays at Power On.

1. 1/4 Duty

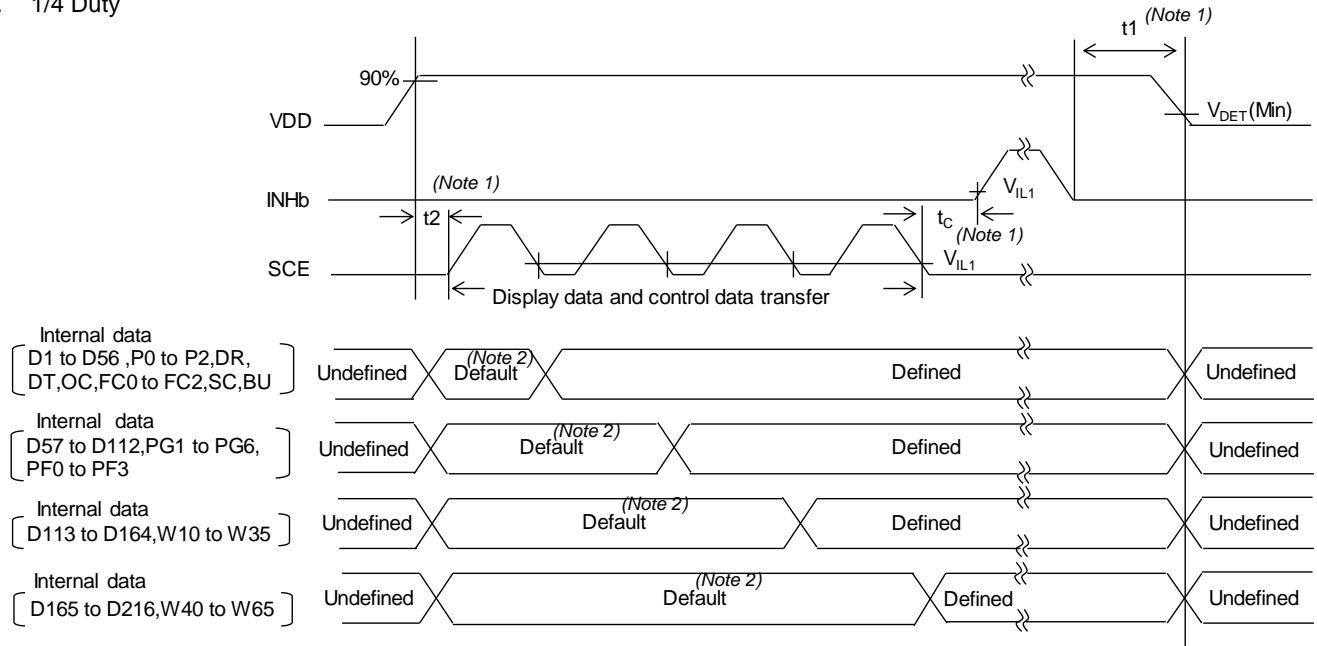


Figure 15. Power On/Off and INHb Control Sequence (1/4 Duty)

(Note 1)  $t1 \geq 0$ ,  $t2 \geq 0$ ,  $t_c$ : (Min) 10 $\mu$ s  
 When VDD level is over 90%, there may be cases where command is not received correctly in unstable VDD.  
 (Note 2) Display Data are undefined. Regarding default value, refer to "Reset Condition"

2. 1/3 Duty

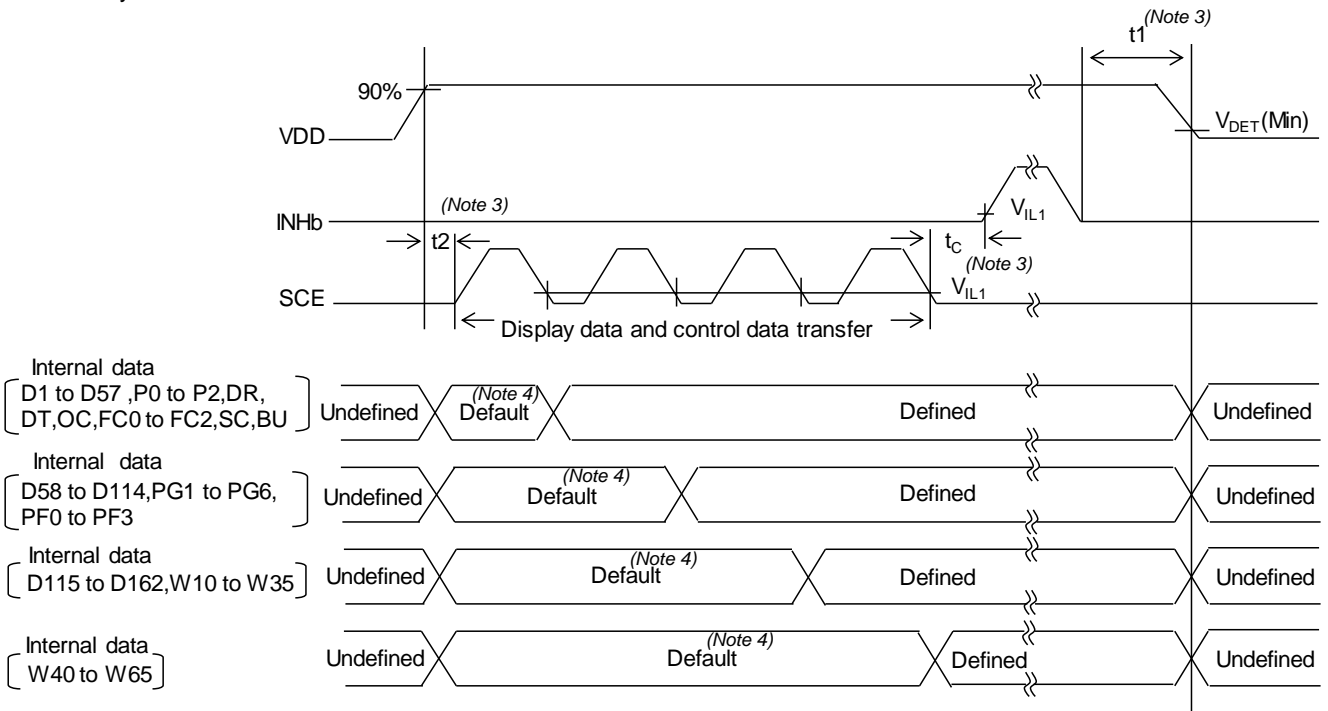


Figure 16. Power On/Off and INHb Control Sequence (1/3 Duty)

(Note 3)  $t1 \geq 0$ ,  $t2 \geq 0$ ,  $t_c$ : (Min) 10 $\mu$ s  
 When VDD level is over 90%, there may be cases where command is not received correctly in unstable VDD.  
 (Note 4) Display Data are undefined. Regarding default value, refer to "Reset Condition".

**Oscillation Stabilization Time of the Internal Oscillation Circuit**

It must be noted that the oscillation of the internal oscillation circuit is unstable for a maximum of 100µs (oscillation stabilization time) after oscillation has started.

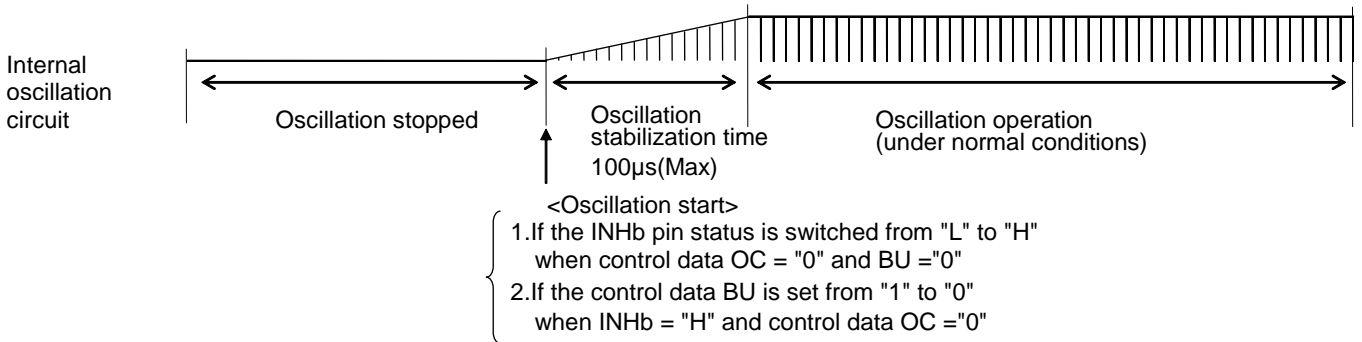


Figure 17. Oscillation Stabilization Time

**Power-saving mode operation in external clock mode**

After receiving [BU]=[1], BU91510KV-M enter to Power-saving mode synchronized with frame then Segment and Common pins output VSS level.

Therefore, in external clock mode, it is necessary to input the external clock based on each frame frequency setting after sending [BU]=[1].

For the required number of clock, refer to Control Data Functions "4. FC0, FC1 and FC2: Frame frequency switching control data".

For example, please input the external clock as below.

[FC0,FC1,FC2]=[0,0,0]: In case of  $f_{osc}/6144$  setting, it needs over 6144clk,

[FC0,FC1,FC2]=[0,1,0]: In case of  $f_{osc}/4608$  setting, it needs over 4608clk,

[FC0,FC1,FC2]=[1,1,1]: In case of  $f_{osc}/1536$  setting, it needs over 1536clk

Please refer to the timing chart below.

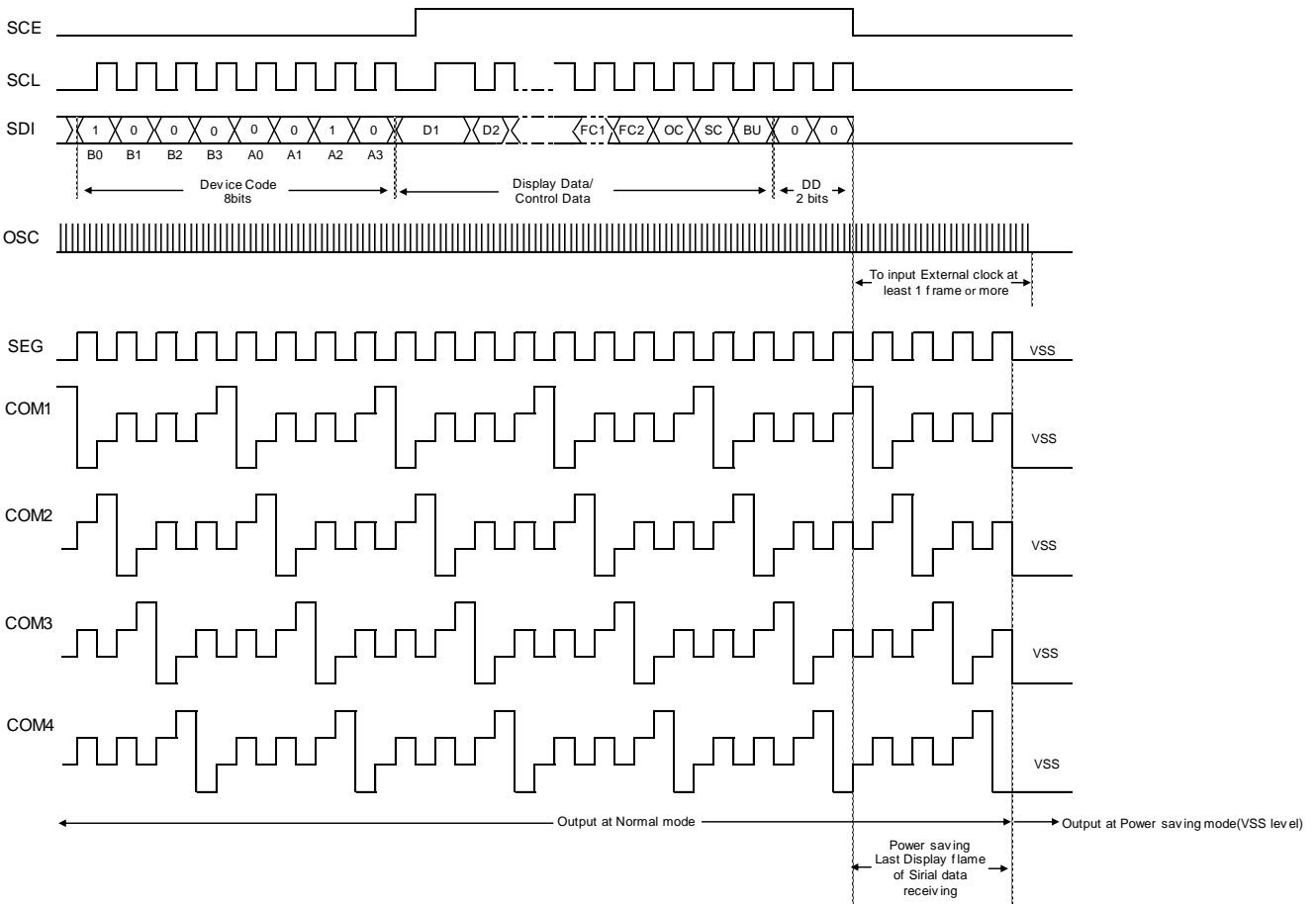


Figure 18. External Stop Timing(1/4 Duty)



**Voltage Detection Type Reset Circuit (VDET)**

The Voltage Detection Type Reset Circuit generates an output signal and resets the system when power is applied for the first time and when voltage drops (that is, for example, the power supply voltage is less than or equal to the power down detection voltage ( $V_{DET} = 1.8V$  Typ) ). To ensure that this reset function works properly, it is recommended that a capacitor must be connected to the power supply line so that both the power supply voltage (VDD) rise time when power is first applied and the power supply voltage (VDD) fall time when the voltage drops are at least 1ms.

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

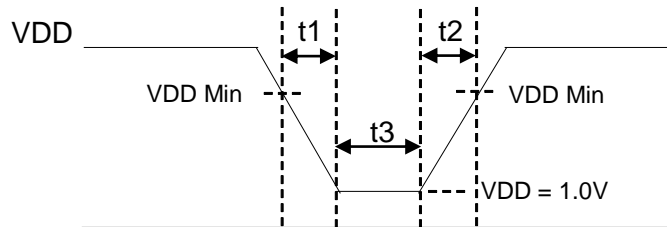


Figure 19. VDET Detection Timing

- Power supply voltage VDD fall time:  $t1 > 1ms$
- Power supply voltage VDD rise time:  $t2 > 1ms$
- Internal reset power supply retain time:  $t3 > 1ms$

If the above conditions cannot be satisfied, the IC may not initialize, so unintended display lighting may occur. In order to reduce this effect, initialize the IC as soon as possible after turning on the power supply. Refer to the IC initialization flow below. But since commands are not received when the power is OFF, the IC initialization flow is not the same function as POR.

Set the BU command to power save mode ([BU] = [1]) and SC command to off (SC = 1) immediately after turning on the power. In BU91510KV-M, command reception is possible (VDD:90%) 0ns after turning on the power. Refer to the timing chart for "The INHb Pin and Display Control".

**Reset Condition**

When BU91510KV-M is initialized, the internal status after power supply has been reset as the following table.

Table 1. control data reset condition

| Instruction              | At Reset Condition  |
|--------------------------|---|
| S1/P1/G1 to S6/P6/G6 Pin | [P0,P1,P2]=[0,0,0]:all segment output                       |
| LCD Bias                 | DR=0: 1/3 Bias  |
| LCD Duty                 | DT=0: 1/4 Duty  |
| Display Frequency        | [FC0,FC1,FC2]=[0,0,0]: $f_{osc}/6144$                       |
| Display Clock Mode       | OC=0:Internal oscillator                                    |
| LCD Display              | SC=1:OFF  |
| Power Mode               | BU=1:Power saving mode                                      |
| PWM / GPO Output         | PGx=0:PWM output(x=1 to 6)                                  |
| PWM Frequency            | [PF0,PF1,PF2,PF3]=[0,0,0,0]: $f_{osc}/2048$                 |
| PWM Duty                 | [Wn0 to Wn5]=[0,0,0,0,0,0]<br>:(1/64)xTp(n=1 to 6, Tp=1/fp) |

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

**Operational Notes – continued****10. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**11. Regarding the Input Pin of the IC**

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

**12. Ceramic Capacitor**

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

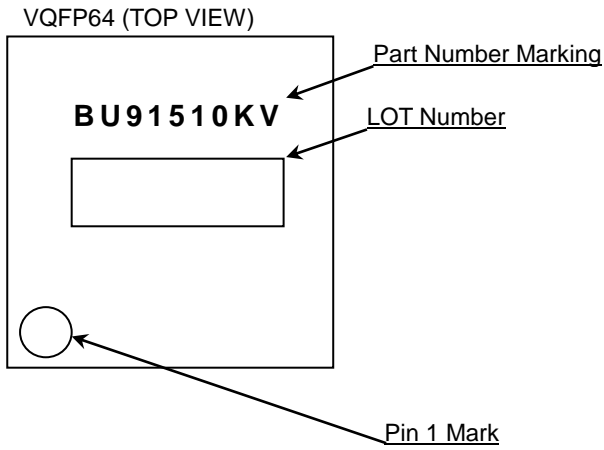
|                   |   |       |
|-------------------|---|-------|
| B U 9 1 5 1 0 K V | - | M E 2 |
|-------------------|---|-------|

Part Number

Package  
KV : VQFP64

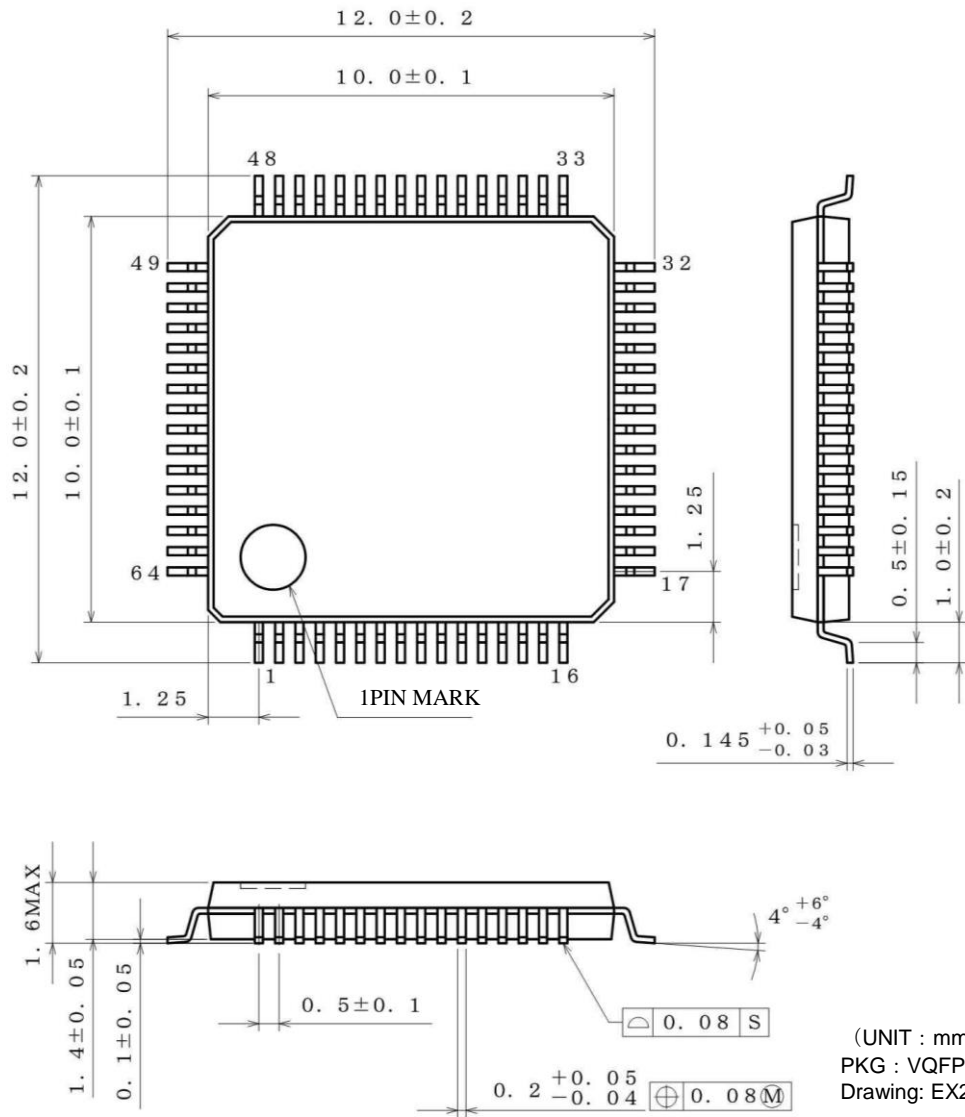
Product Rank  
M: for Automotive  
Packaging Specification  
E2: Embossed tape and reel

Marking Diagram



Physical Dimension, Tape and Reel Information

|              |        |
|--------------|--------|
| Package Name | VQFP64 |
|--------------|--------|



(UNIT : mm)  
 PKG : VQFP64  
 Drawing: EX252-5001-1

<Tape and Reel information>

|                   |   |
|-------------------|---|
| Tape              | Embossed carrier tape (with dry pack)   |
| Quantity          | 1000pcs   |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |

\*Order quantity needs to be multiple of the minimum quantity.

## Revision History

| Version | Date        | Description   |
|---------|-------------|---|
| 001     | 8.July.2015 | New edition   |
| 002     | 29.Jan.2018 | <p>Page 3. Remove temperature condition in Absolute Maximum Ratings. Ta=25°C → Removed</p> <p>Page 3. Modify Maximum Supply Voltage in Absolute Maximum Ratings: -0.3 to +6.5 → -0.3 to +7.0.</p> <p>Page 3. Modify Input Voltage in Absolute Maximum Ratings: -0.3 to +6.5 → -0.3 to +7.0.</p> <p>Page 3. Add OSC in Absolute Maximum Ratings Input Voltage.</p> <p>Add Caution2 in Absolute Maximum Ratings condition. (Moved from Operational Notes)</p> <p>Page 4. Add "External Clock Rise Time", "External Clock Fall Time" and "External Clock Duty" in Oscillation Characteristics.</p> <p>Page.6 Typo Modification in Pin Description in page.6.<br/>S1/P1/G1 to S6/P6/G6, S7 to S54 → S1/P1/G1 to S6/P6/G6, S7 to S51, S53, S54</p> <p>Page.6 Add S52/OSC in Pin Description Function additional explanation</p> <p>Page.6 Add S52/OSC descriptions of "Function", "I/O" and "Handling when unused" of in Pin Description.</p> <p>Page.6 Modify diagram of "Figure 6.I/O Equivalence Circuit".</p> <p>Page 11 to 14. Add "Reset condition" in Control Data Functions.</p> <p>Page 12. Add "External Clock input timing function" in "5.OC: Internal oscillator operating mode/External clock operating mode switching control data".</p> <p>Page 23. Modify diagram of "Figure 15. Power On/Off and INHb Control Sequence (1/4 Duty)".<br/>Modify diagram of "Figure 16. Power On/Off and INHb Control Sequence (1/3 Duty)".</p> <p>Page.23 Add notes for Figure 15 and Figure 16..</p> <p>Page 24. Add "Power-saving mode operation in external clock mode".</p> <p>Page 25. Add explanation in "Voltage Detection Type Reset Circuit (VDET)".</p> <p>Correction of errors</p> |

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| JAPAN     | USA       | EU         | CHINA     |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV  |           | CLASS III  |           |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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  - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
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6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

### Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
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  - [d] the Products are exposed to high Electrostatic
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3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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